北方工业大学
NORTH CHINA UNIVERSITY OF TECHNOLOGY

中国科学院微电子研究所
INSTITUTE OF MICROELECTRONICS OF THE CHINESE ACADEMY OF SCIENCES

《集成电路先进制造工艺技术》 中级培训班

PDK建模与版图设计

2022-04-07

目 录

- **模拟电路版图和PDK建模**
- 数字标准单元版图和库模型建立
- 工艺掩模版优化和监控
- Q&A

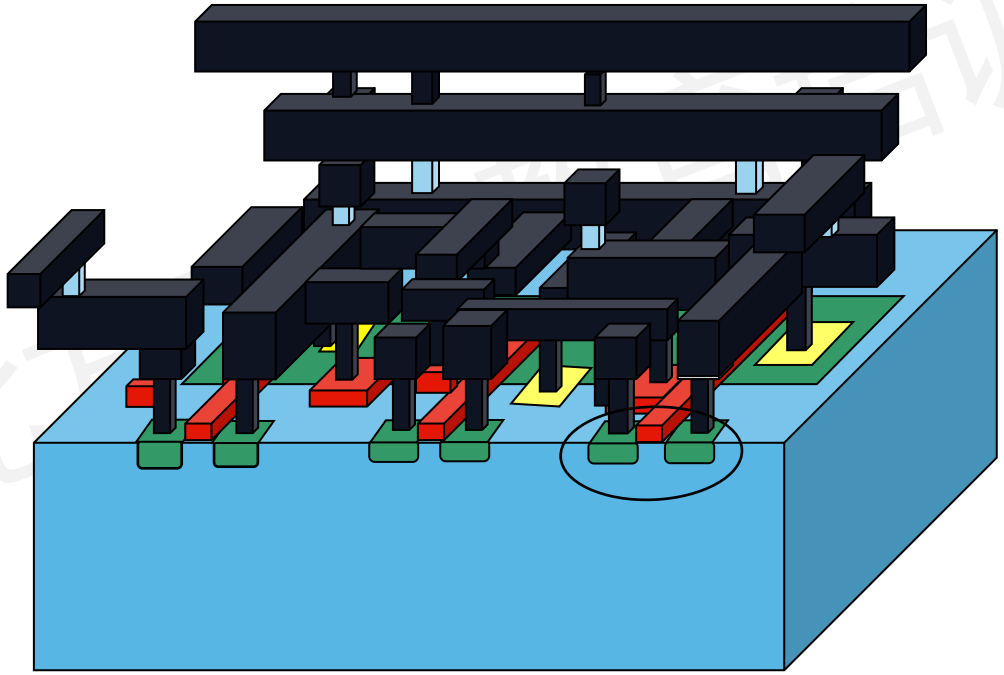
集成电路定义

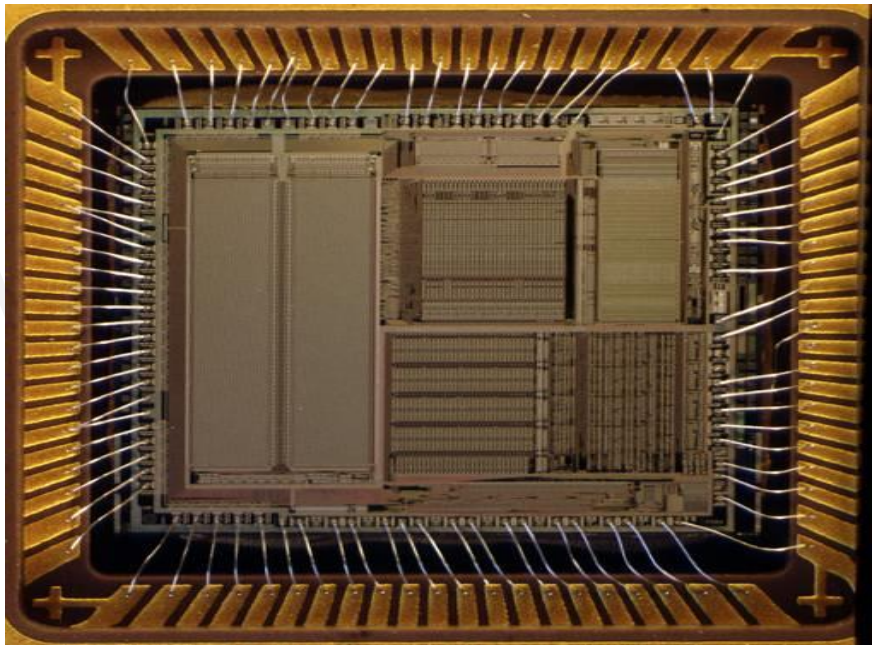
8寸晶圆厚度一般为

725um,直径200mm

通过多层布线把一系列复杂的元器件互

连在一起实现所需电路功能





使用金线或铜线连接

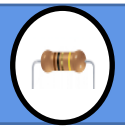
管壳Pin和芯片Pad

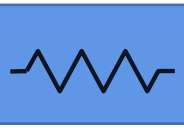
网络公开资料

集成电路分类

Transistor – 开关

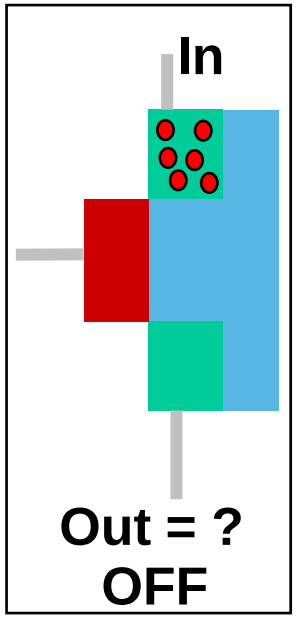
Resistor – 分压，降低电流



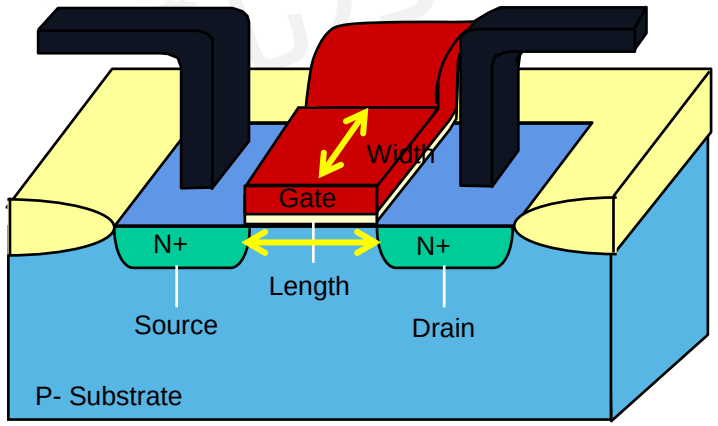


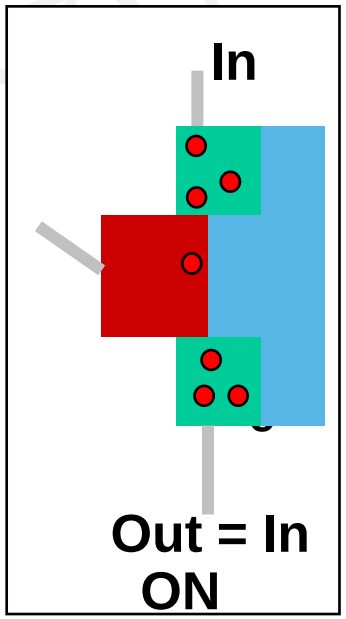
Capacitor – 存储电荷

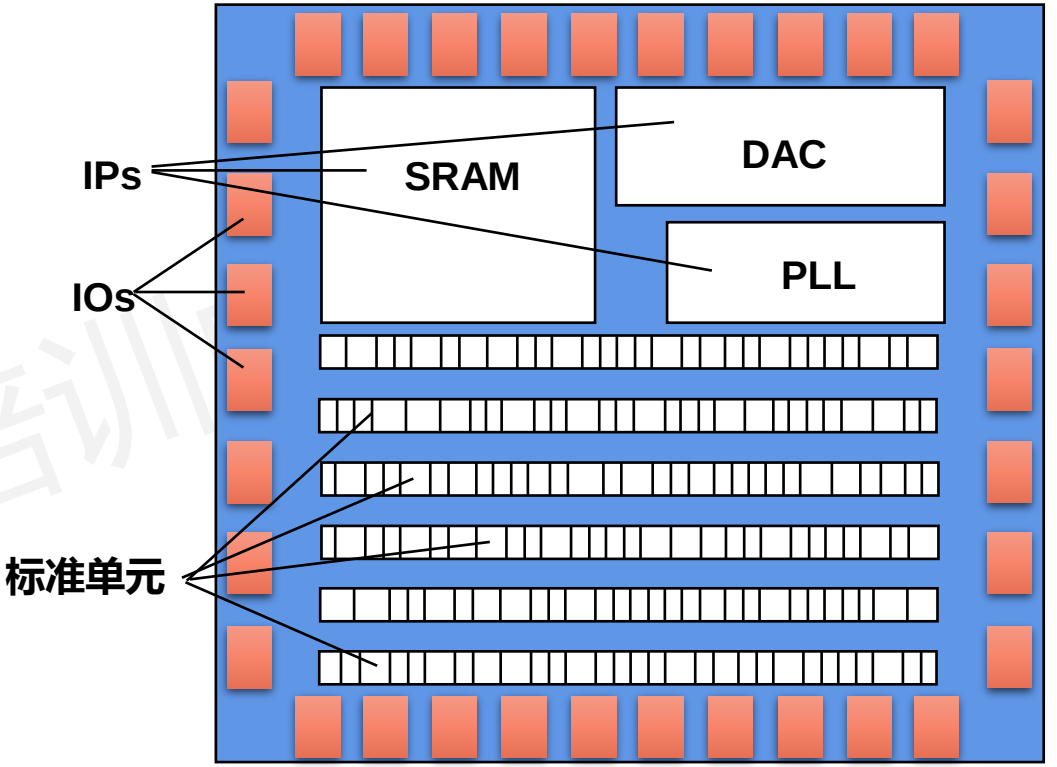
金属互联整合



90nm technology – L_{min}=90nm
45nm technology – L_{min}=45nm
22nm technology – L_{min}=22nm

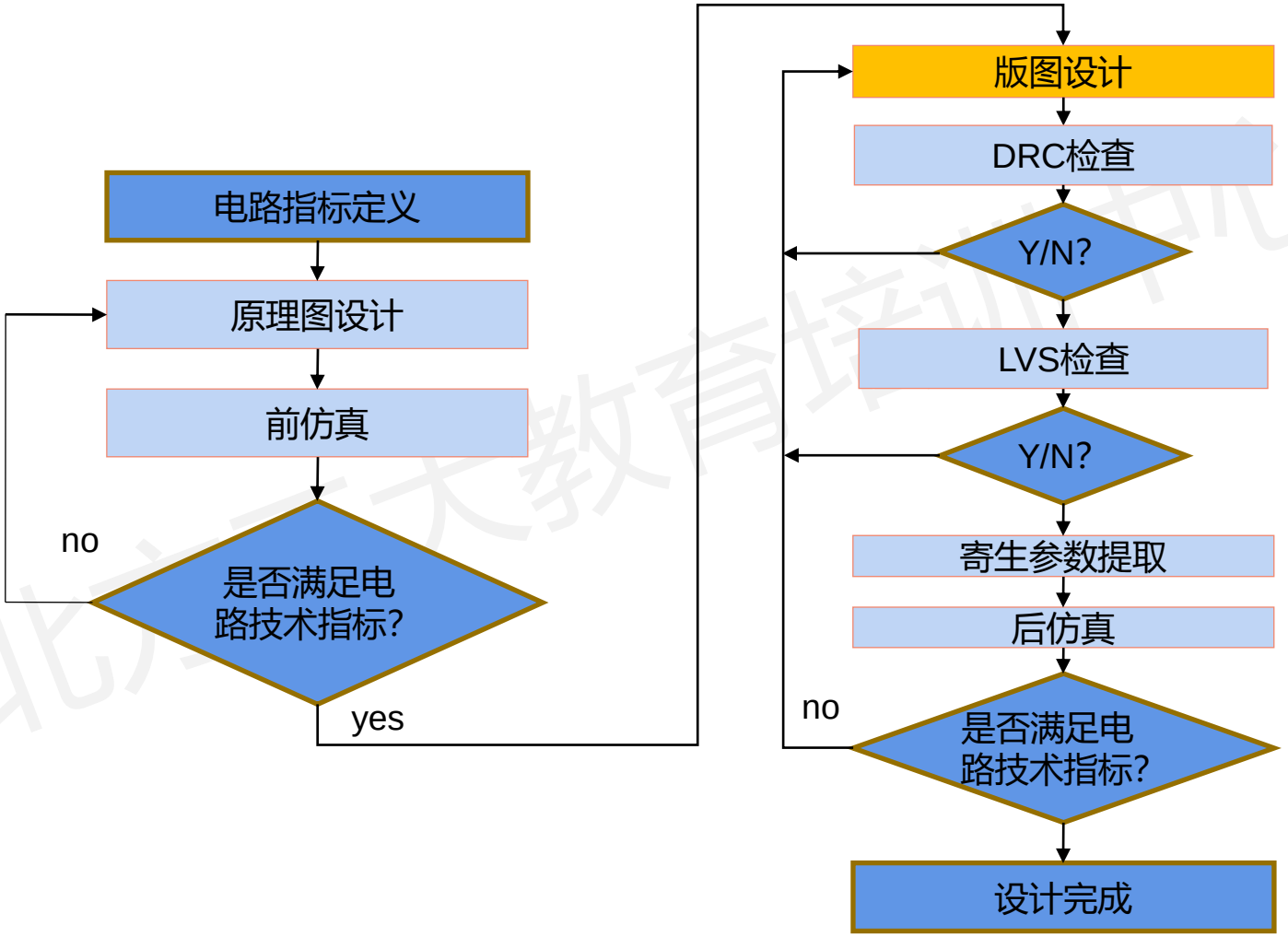






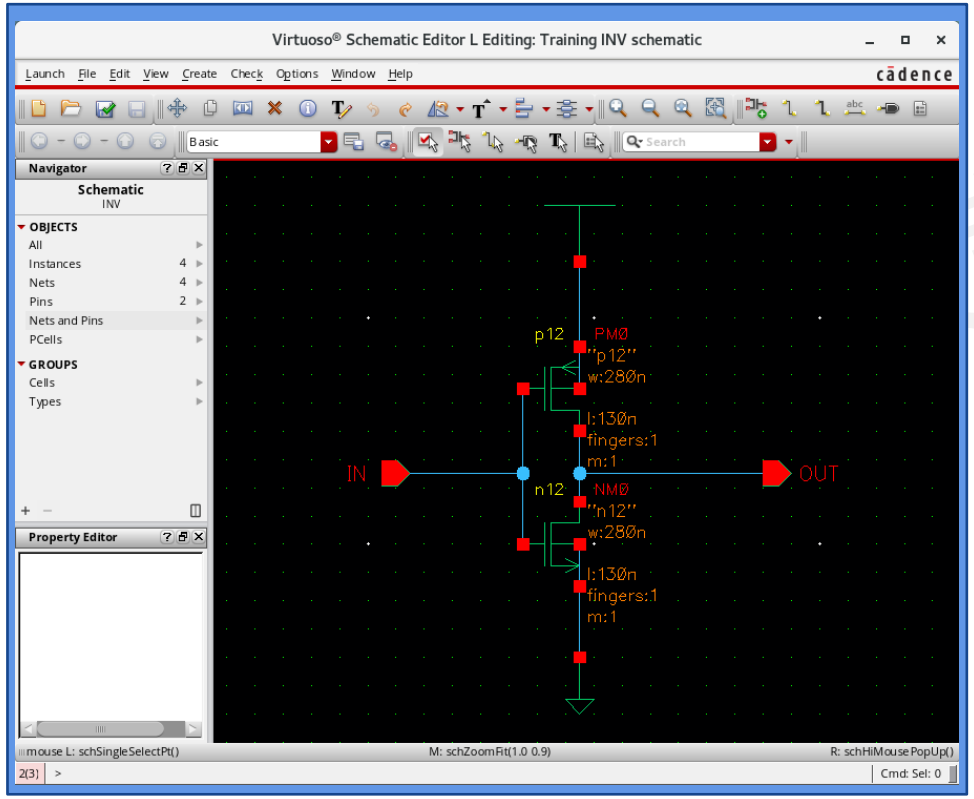
- Intellectual Property (IP)含有某些功能的黑盒子，例如ADC，PLL等；
- Input/Output (IO)连接芯片内部和外围环境的接口
- 具有固定高度但长度不同的数字标准单元

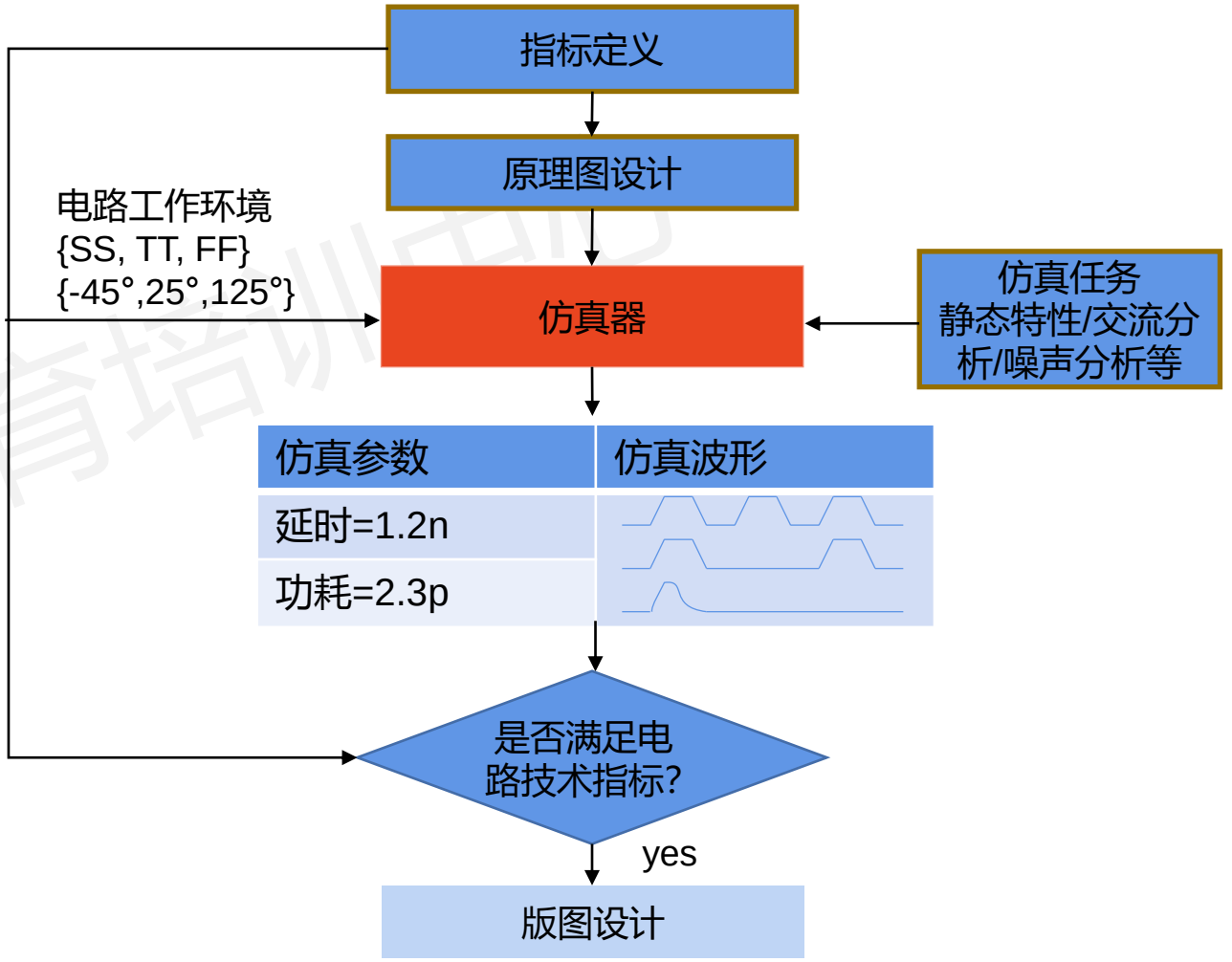
模拟电路设计流程


电路指标定义
原理图设计
前仿真
是否满足电路技术指标?
no
yes
版图设计
DRC检查
Y/N?
LVS检查
Y/N?
寄生参数提取
后仿真
是否满足电路技术指标?
no
设计完成

模拟电路原理图设计

主要目的即是在某种工作条件下，仿真设计出满足产品指标参数要求、且可进行电路器件参数调节的电路功能原理图

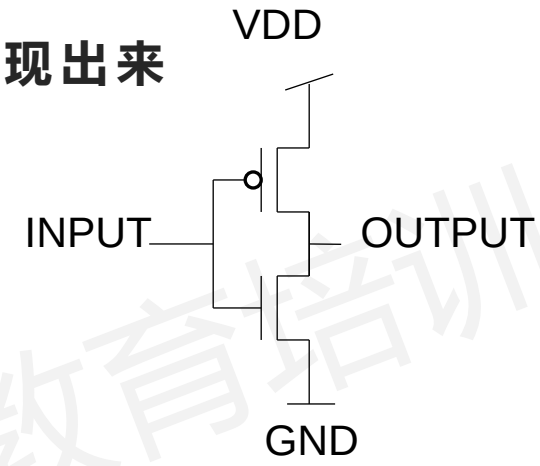


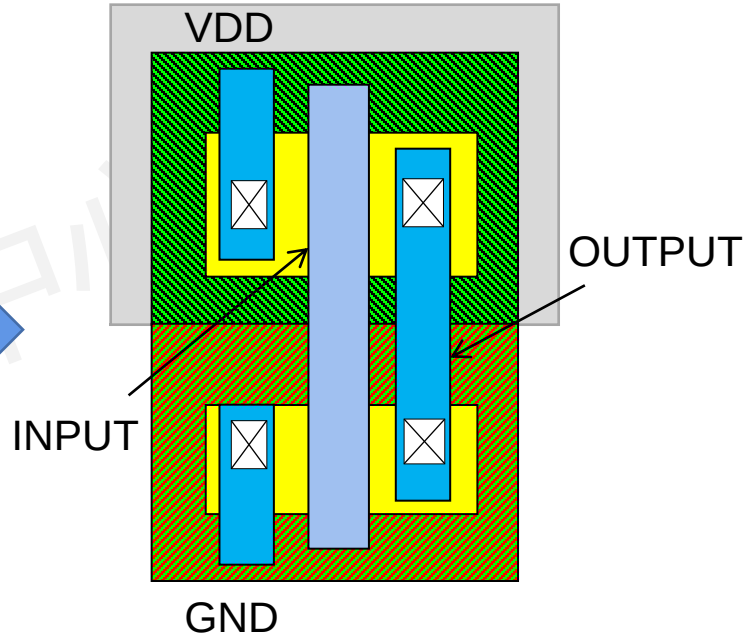


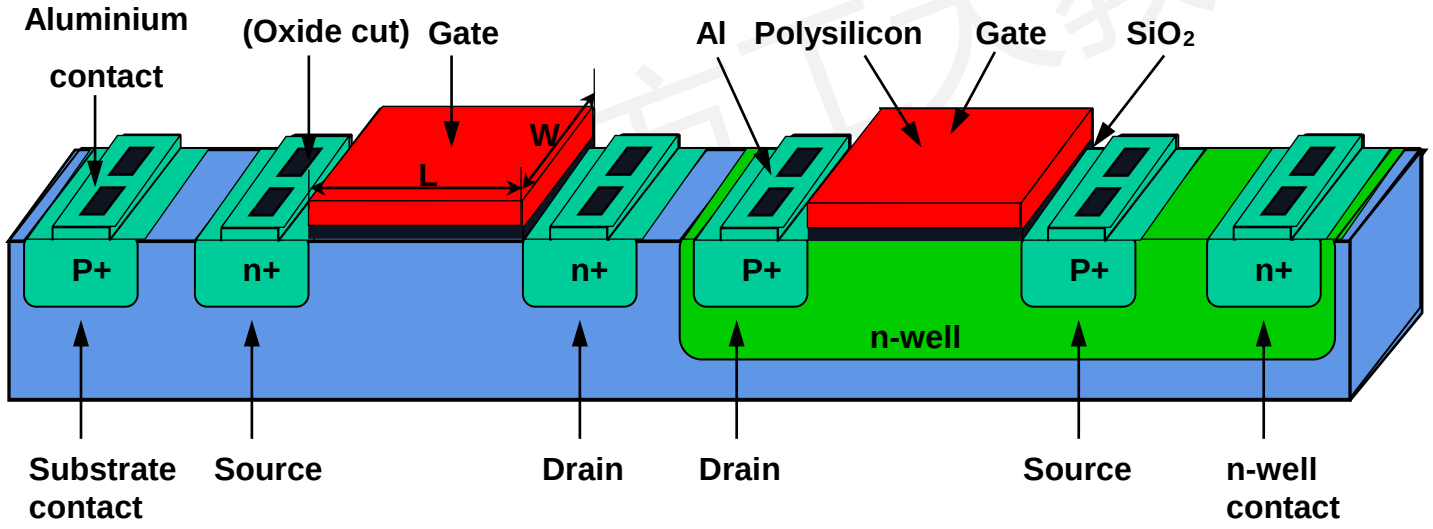
模拟电路版图设计

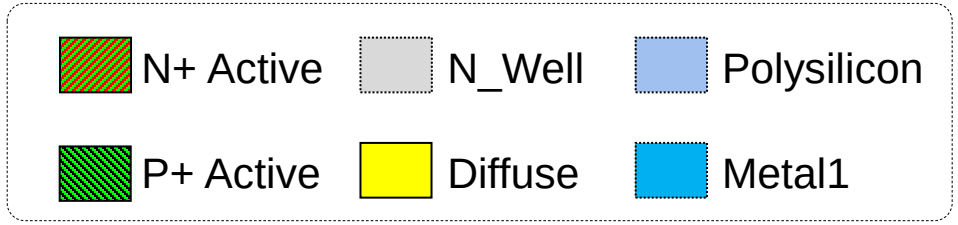
设计目的：

- 把原理图中的器件和连接关系在版图中体现出来
- 保证整体版图功能正常
- 确保不违反工艺制造规则

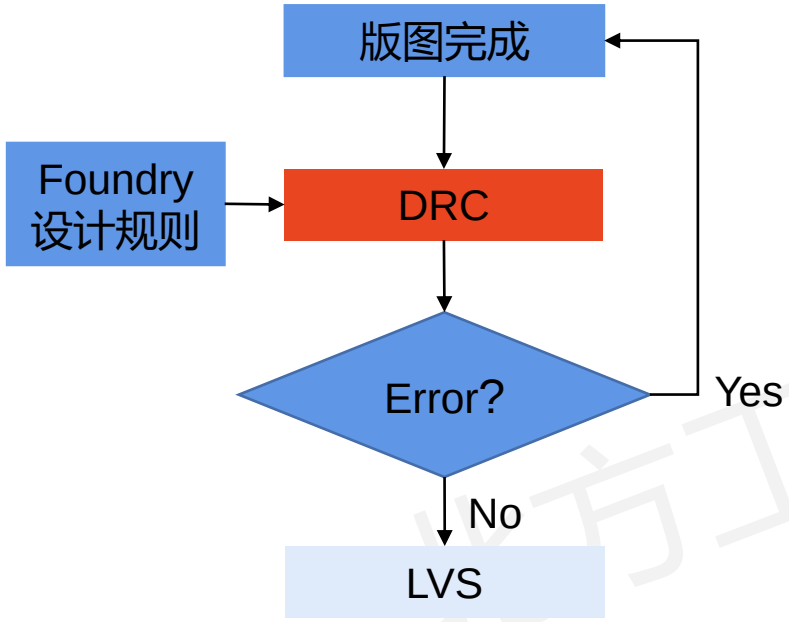


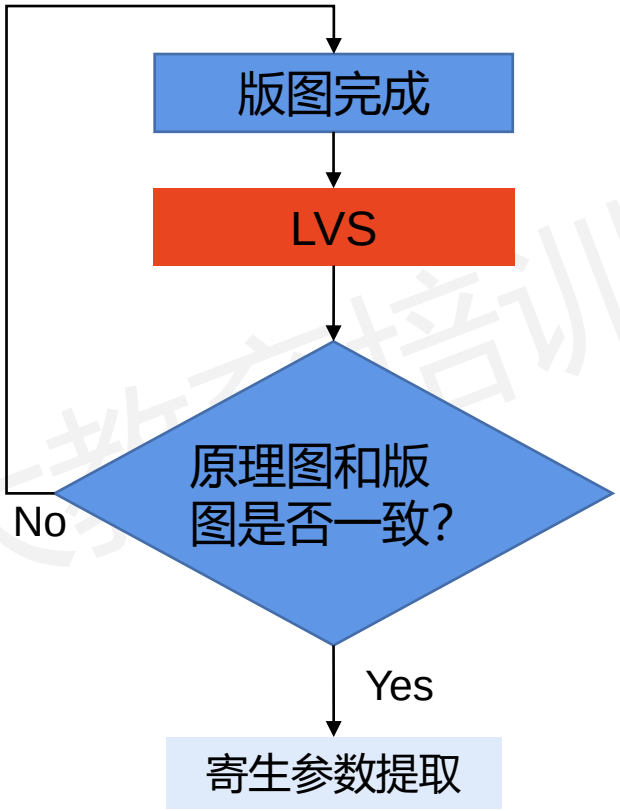




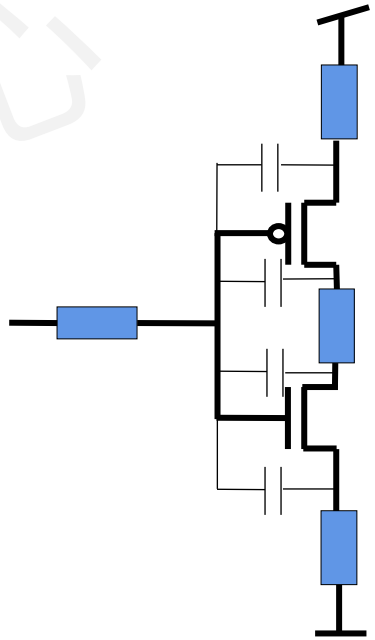


模拟电路物理验证

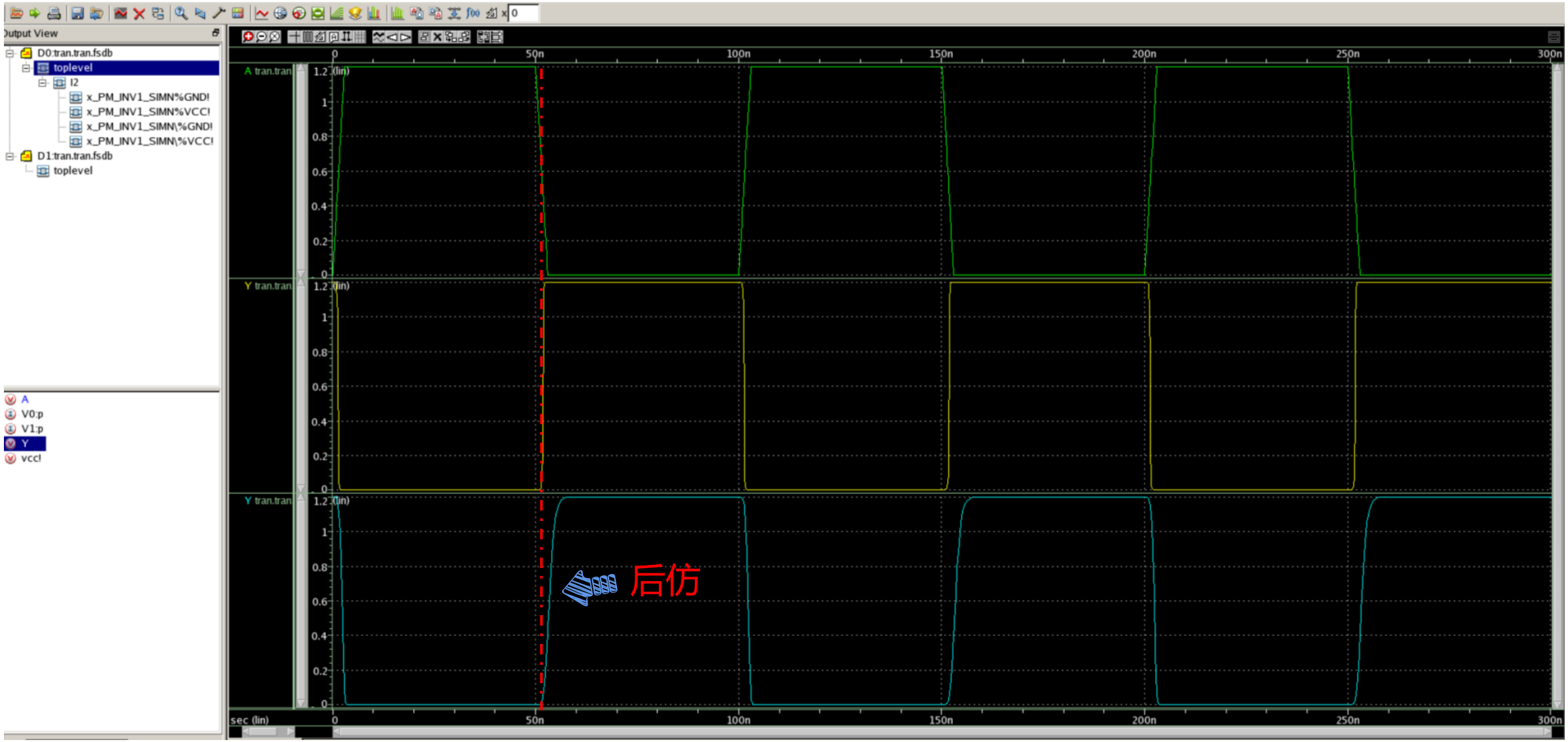




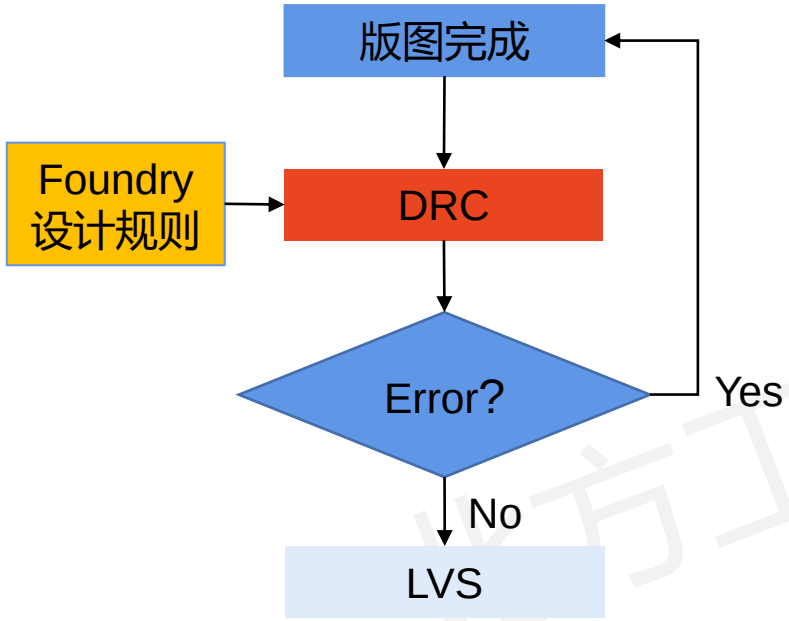
寄生参数提取



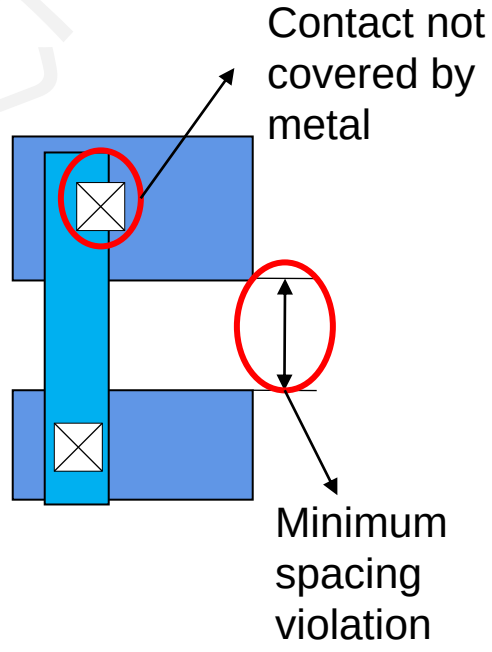
模拟电路仿真


Output View
D0:tran.tran.fsdb
toplevel
I2
x_PM_INV1_SIMN%GND!
x_PM_INV1_SIMN%VCC!
x_PM_INV1_SIMN\%GND!
x_PM_INV1_SIMN\%VCC!
D1:tran.tran.fsdb
toplevel
A
V0:p
V1:p
Y
vcc!
A tran.tran
Y tran.tran
Y tran.tran
0
50n
100n
150n
200n
250n
300n
sec (lin)
后仿

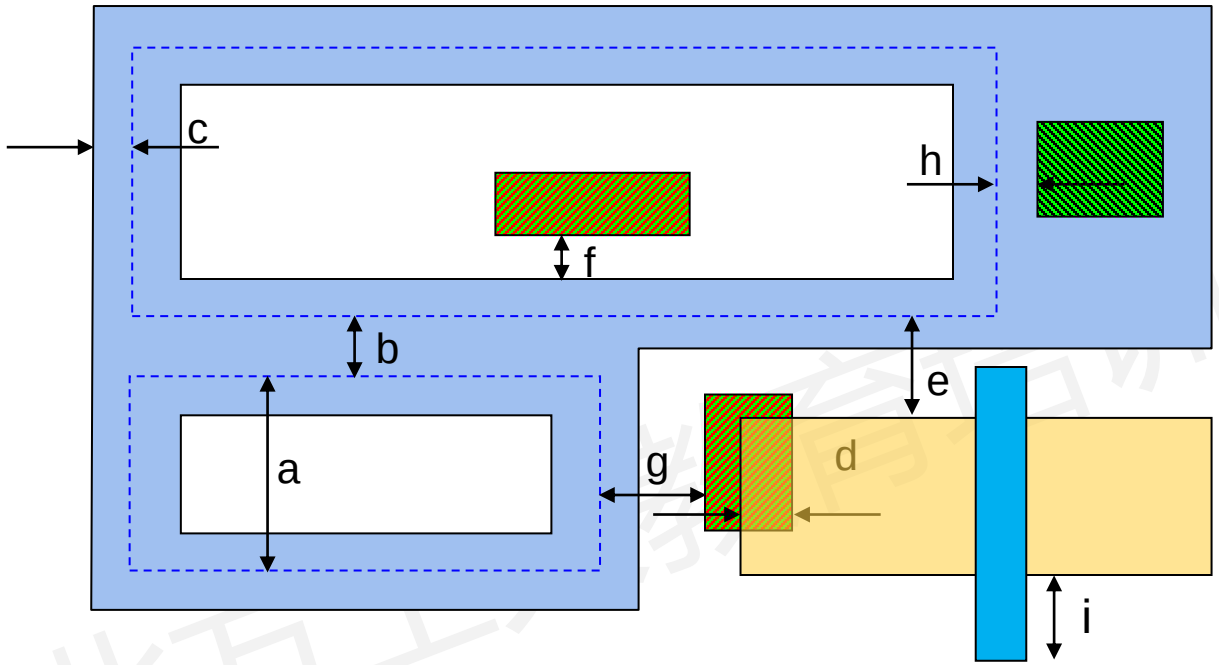
模拟电路设计规则检查

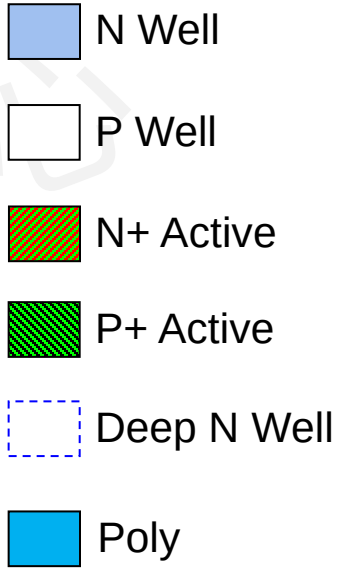



```
INTERNAL m1 {
    COMMENT = "M1.W.1: Minimum width=0.14um "
    SPACING < 0.14
    NON_PARALLEL = TRUE
    POINT_TOUCH = TRUE
} (163)

EXTERNAL m1 {
    COMMENT = "M1.S.1: Minimum spacing=0.14um "
    SPACING < 0.14
    CHECK_SAME_POLYGON = TRUE
    NON_PARALLEL = TRUE
    POINT_TOUCH = TRUE
} (163)

AREA m1 {
    RANGE = [1e-05, 0.07 - 1e-05]
    COMMENT = "M1.A.1  M1 minimum area = 0.07um^2 "
} (163)


SIZE m1 {
    UNDER_OVER=2.5
    LEVEL_NON_ORTHOGONAL = TRUE
} TEMP=m1wide
```



DRC检查种类





a – minimum width

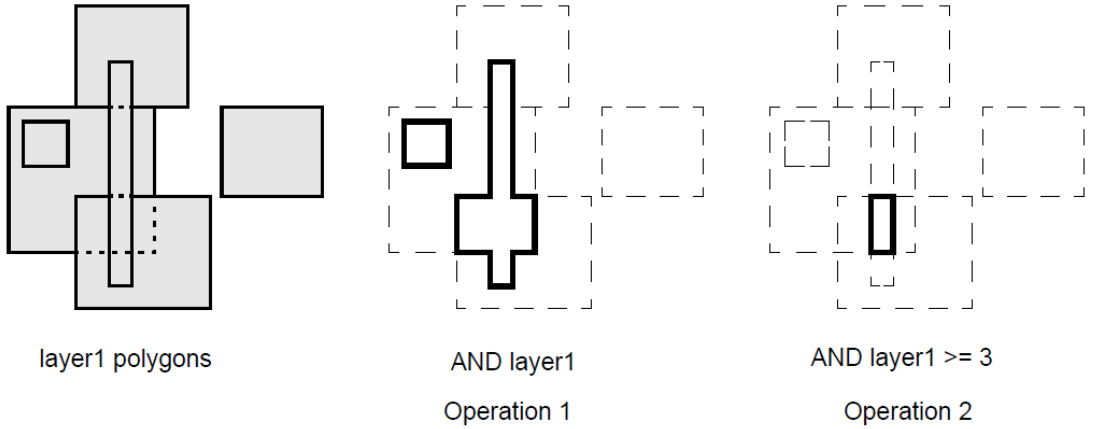
b, e, g, h – minimum spacing

c, f – minimum enclosure

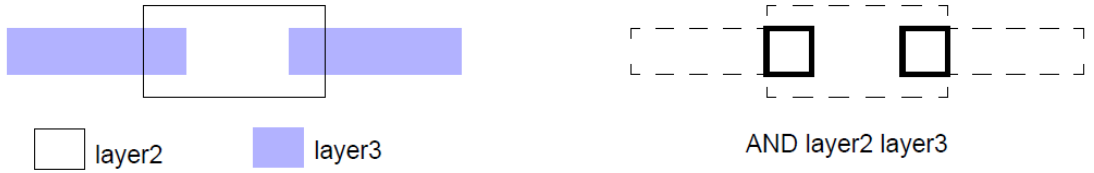
i – minimum extension

d – minimum overlap

布尔运算

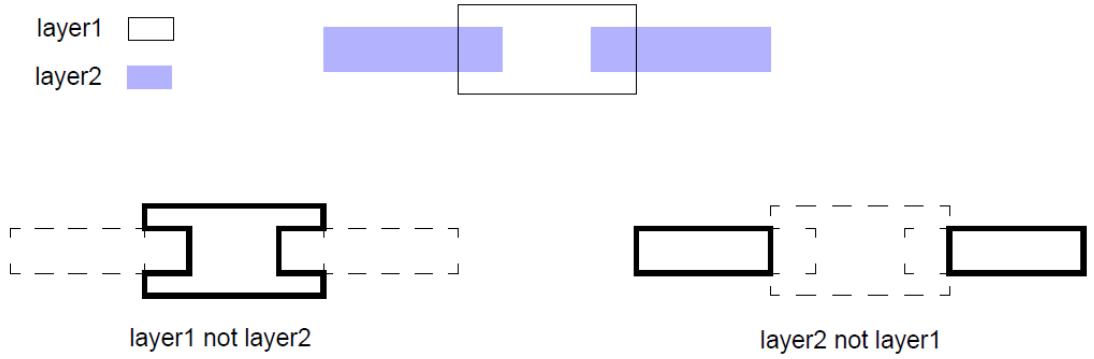


One-layer AND



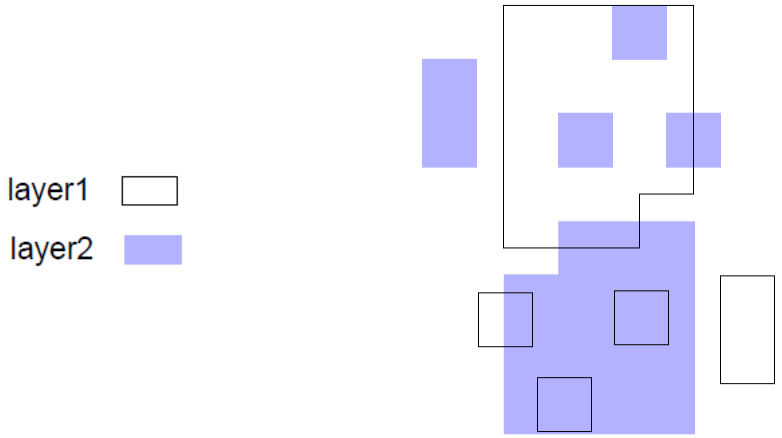
Two-layer AND

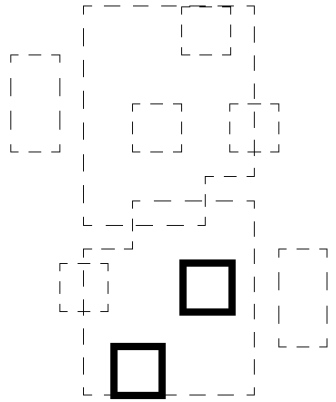
Two-layer OR



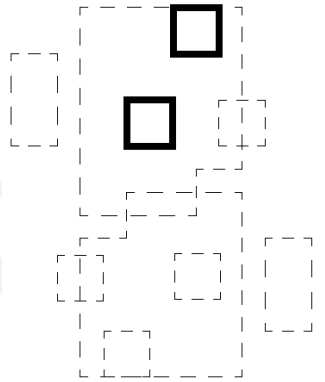
NOT

布尔运算



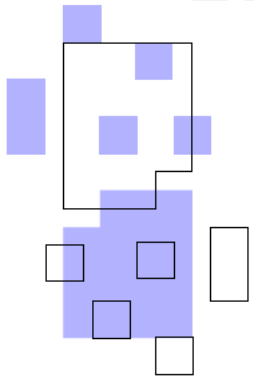


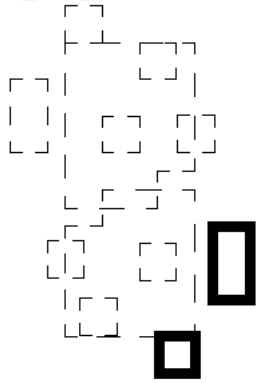
inside layer1 layer2
//also layer1 inside layer2



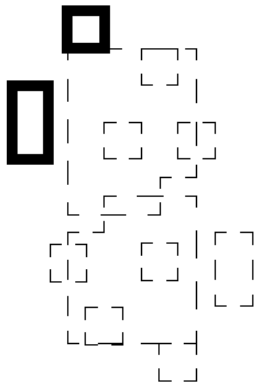
inside layer2 layer1

INSIDE





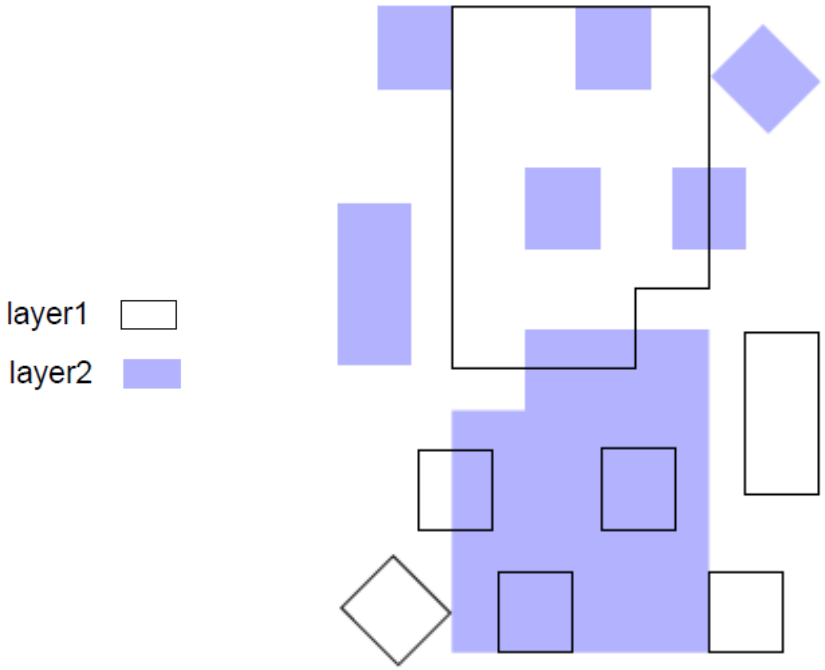
outside layer1 layer2

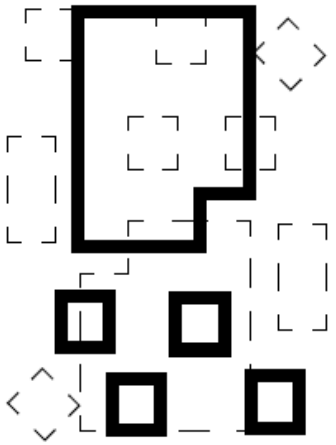


outside layer2 layer1

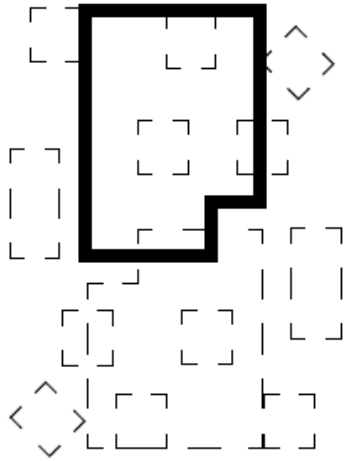
OUTSIDE

布尔运算





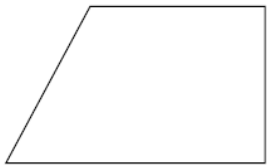
interact layer1 layer2
//also layer1 interact layer2



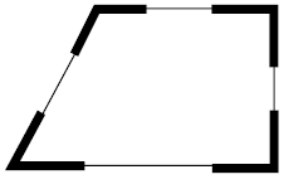
interact layer1 layer2 > 1

INTERACT

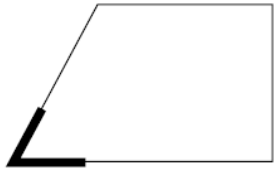
布尔运算 - Options



rule_n {int X < m}
//abutting edges
//not checked
//no other violations



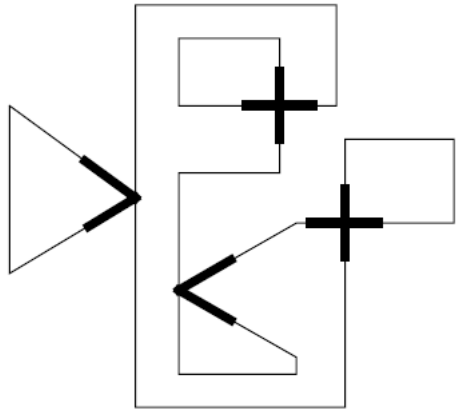
rule_o {int X < m ABUT}
//all abutting edges
//are checked



rule_p {int X < m
ABUT < 90}

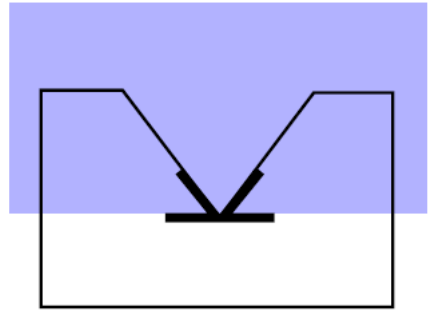
ABUT

Single-layer
Internal SINGULAR



singularities

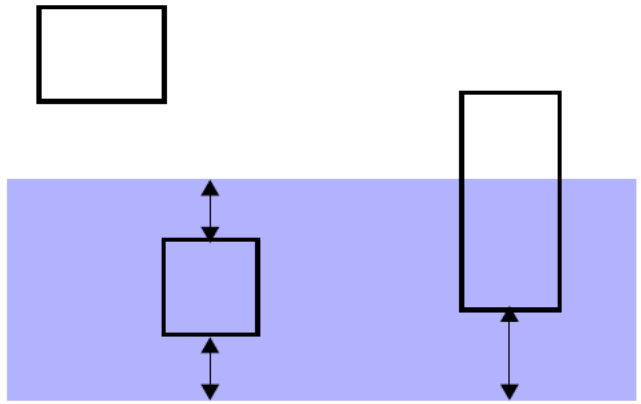
Two layer
INTERNAL SINGULAR



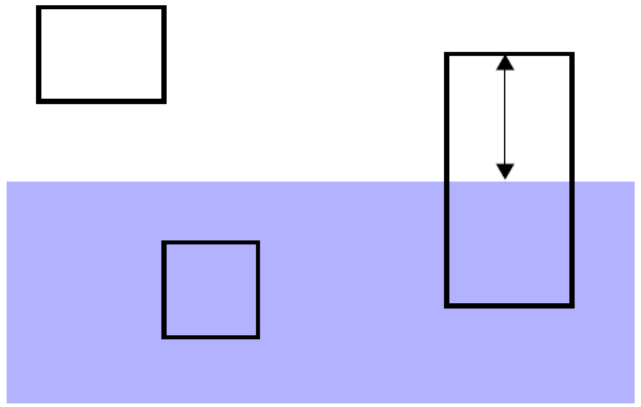
SINGULAR

布尔运算

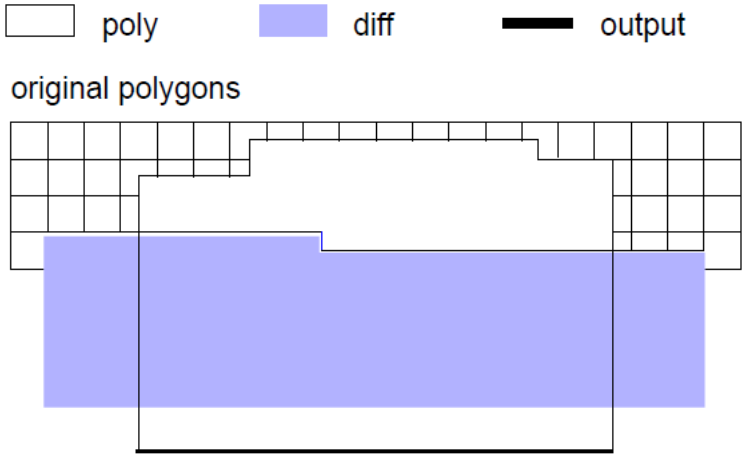
rule_a {ENC layer1 layer2 < m}

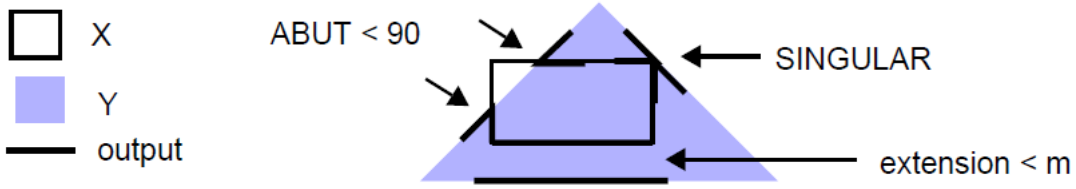


rule_b {ENC layer2 layer1 < m}

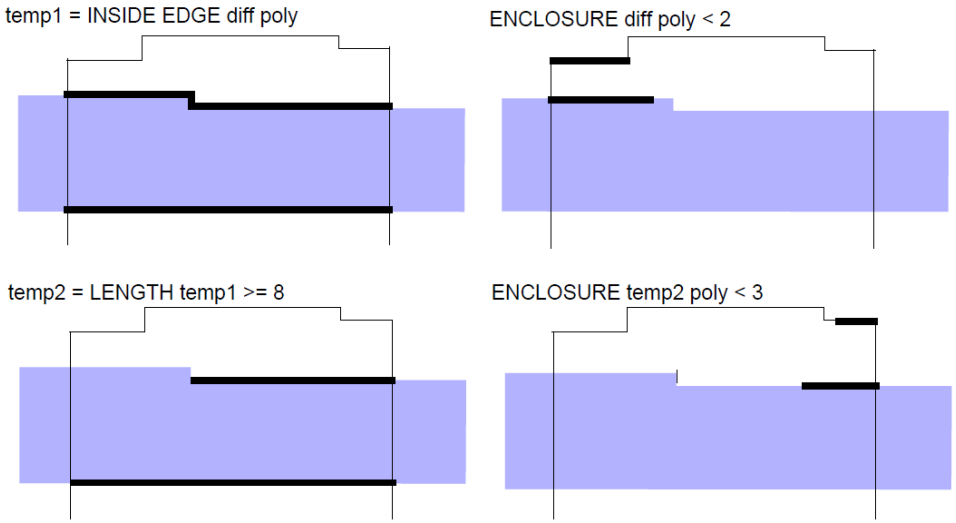


layer1 layer2



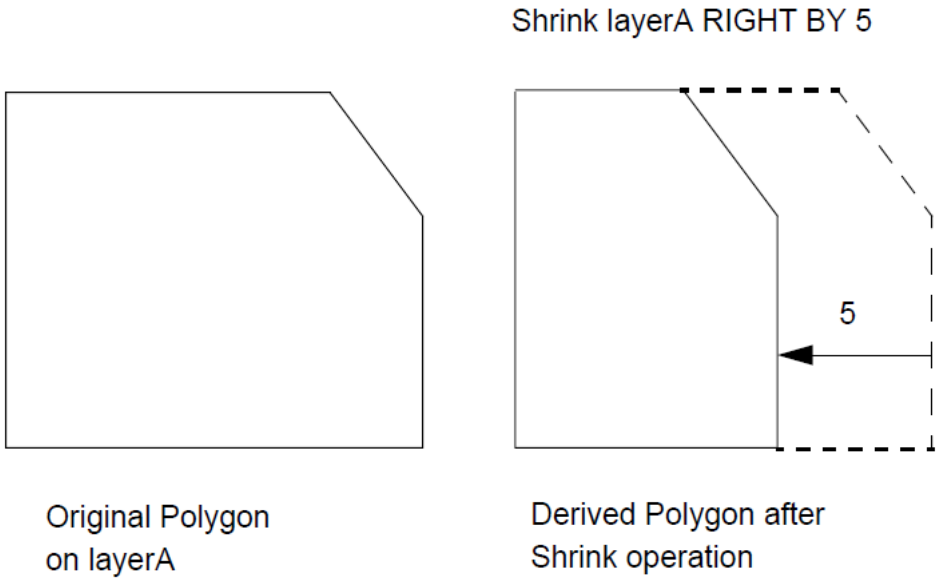


rule_c {ENC X Y < m ABUT < 90 SINGULAR}

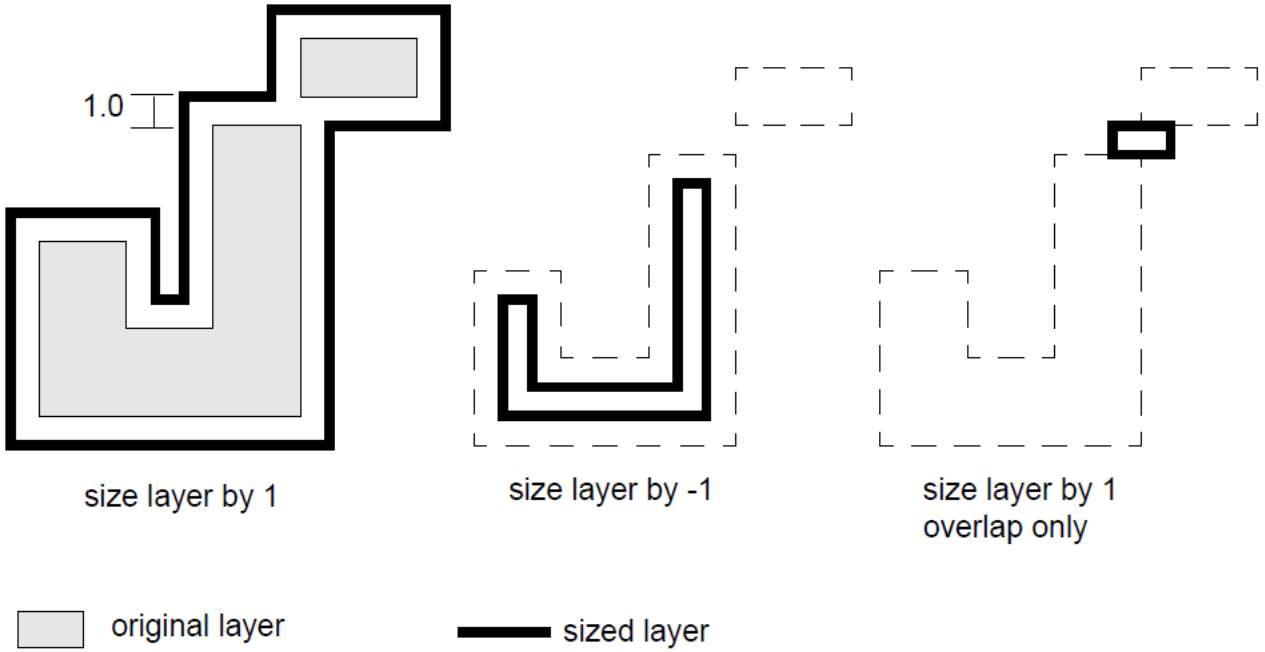


ENCLOSURE

布尔运算

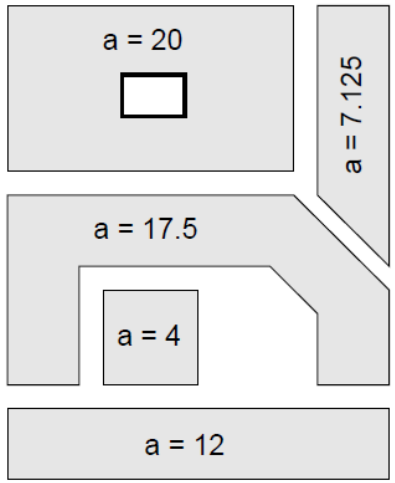


SHRINK

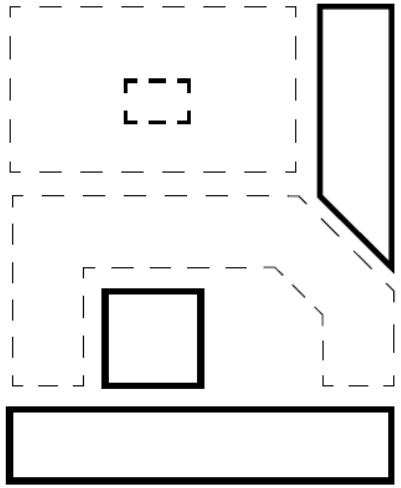


SIZE

布尔运算

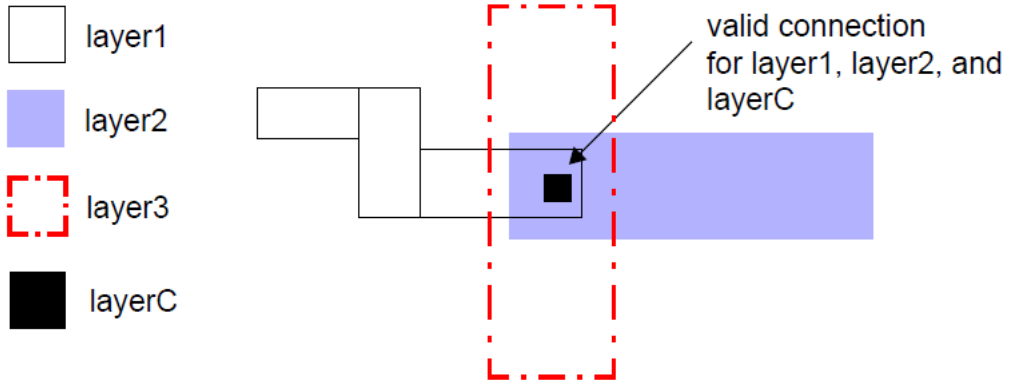


layer1 polygons



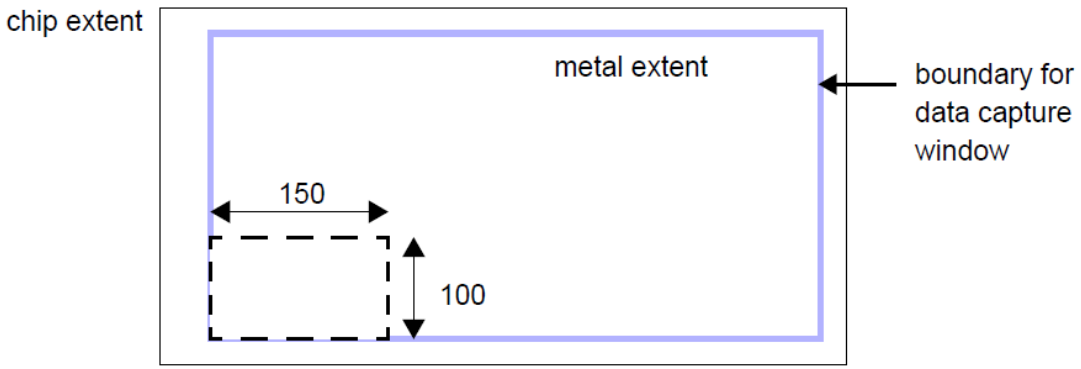
area layer1 < 12.5

AREA

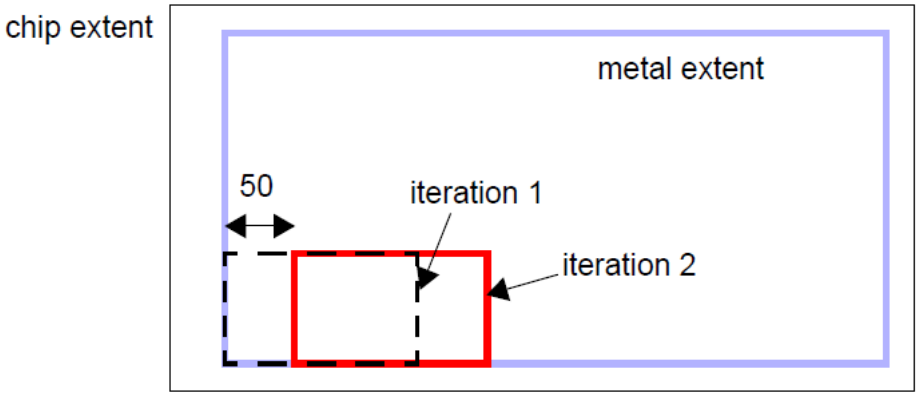


CONNECT layer1 layer2 layer3 BY layerC

CONNECT



rule { DENSITY metal < 25 INSIDE OF EXTENT
WINDOW 150 100}



rule {DENSITY metal < 25 INSIDE OF EXTENT
WINDOW 150 100 STEP 50}

DENSITY

Standard Verification Rule Format Manual

工艺器件定义

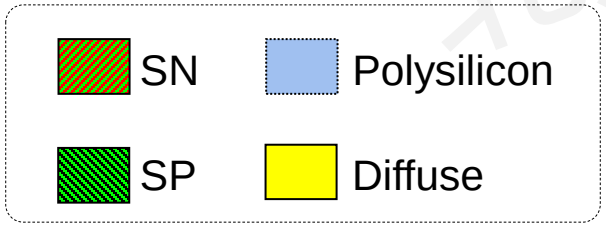
PACT = SP AND AA
NACT = SN AND AA

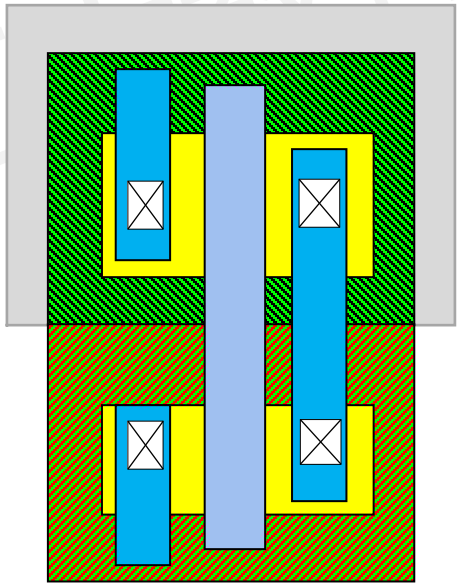
PGATE = PACT AND GT
NGATE = NACT AND GT

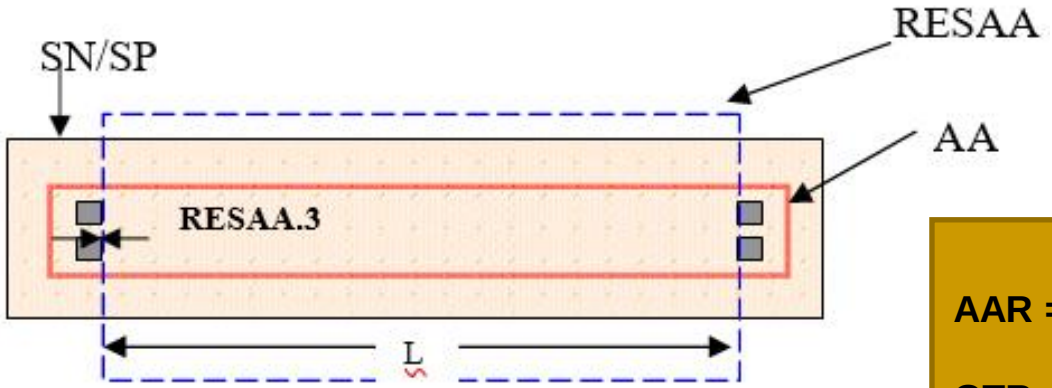
PSD = (PACT NOT PGATE) TOUCH PGATE
NSD = (NACT NOT NGATE) TOUCH NGATE

NMOS = NGATE OR NSD
PMOS = PGATE OR PSD

Transistor







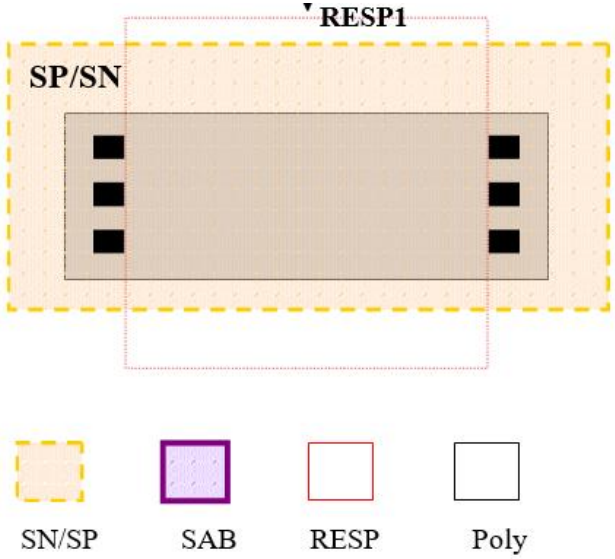
AA Resistor without SAB

AAR = AA INTERACT RESAA

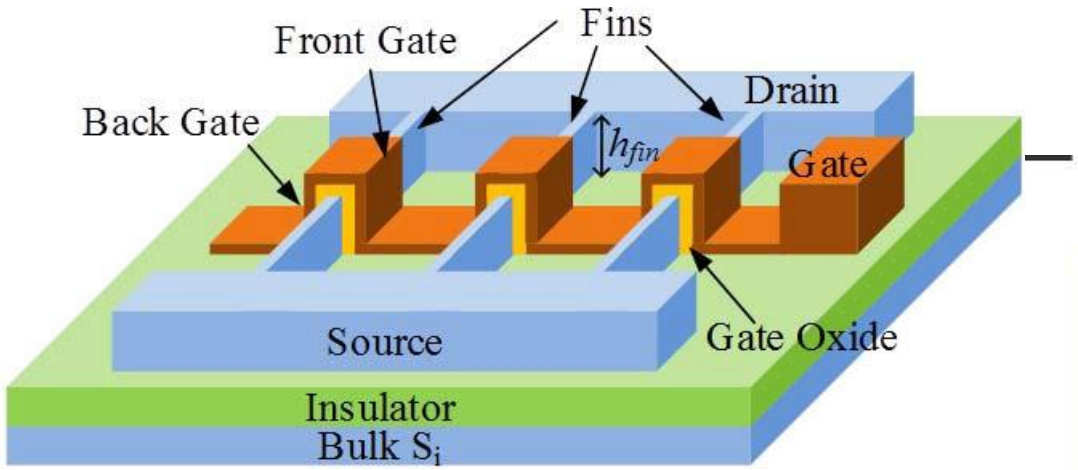
GTR = GT INTERACT RESP1

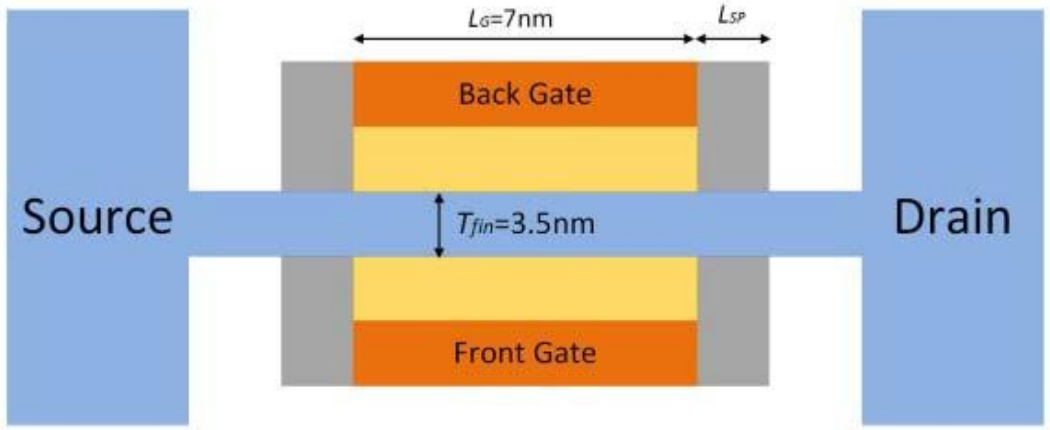
Resistor

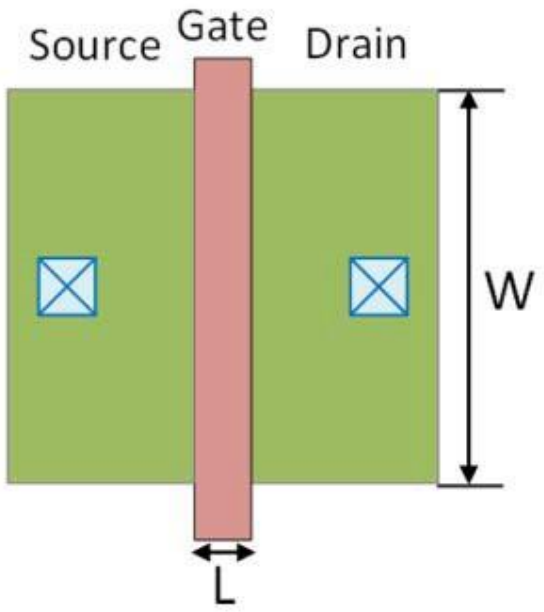
Poly Resistor without SAB



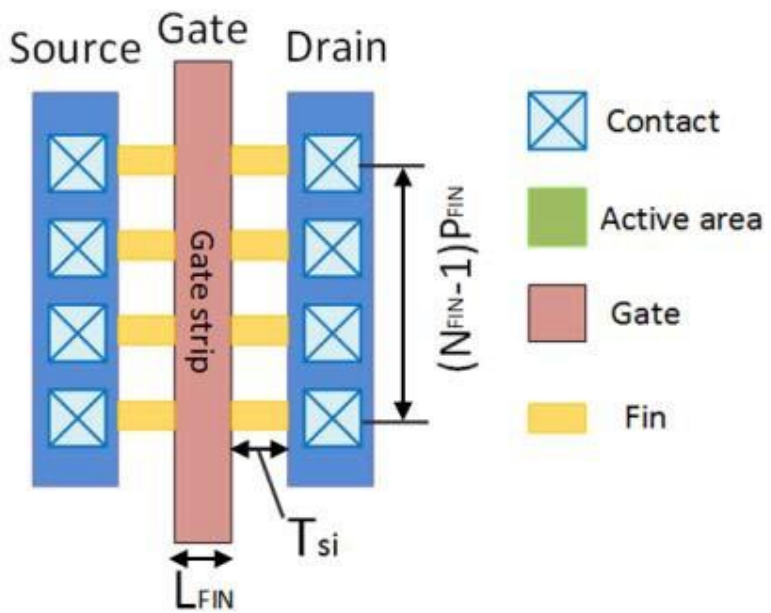
FinFET器件







(a)

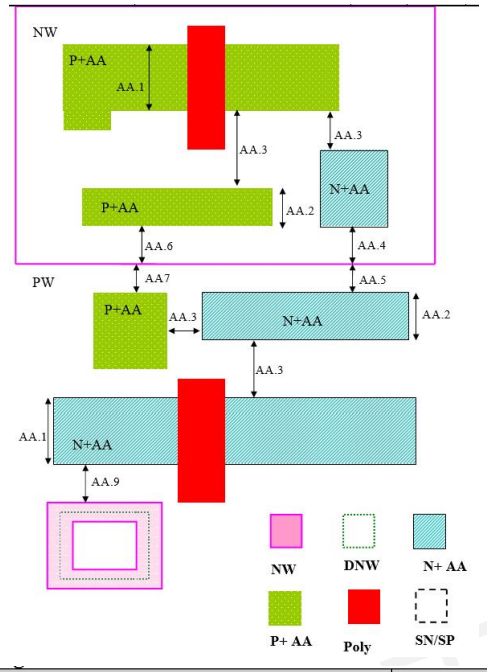


(b)

7nm FinFET Standard Cell Layout

DOI: 10.1109/IGCC.2014.7039170

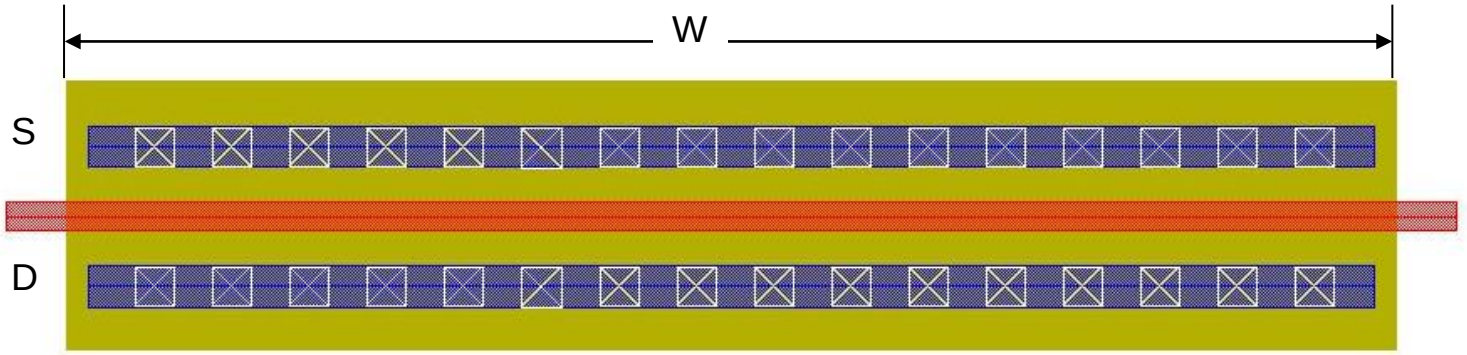
AA Design Rule



Rules number	Description	Operation	Design Value	Unit
AA.1	AA width for NMOS/PMOS transistors	≥	0.15	um
AA.2	AA width for interconnect	≥	0.15	um
AA.3	Space between AAs that are on the same well, INDMY (212;0) covered regions are excluded for this rule check.	≥	0.21	um
AA.4	N+AA enclosure by NW except NW resistor region.	≥	0.23	um
AA.5	Space between NW and N+AA	≥	0.30	um
AA.6	P+AA enclosure by NW	≥	0.30	um
AA.7	Space between NW to P+AA inside PW	≥	0.23	um
AA.8	AA area (in um^2)	≥	0.10	um^2

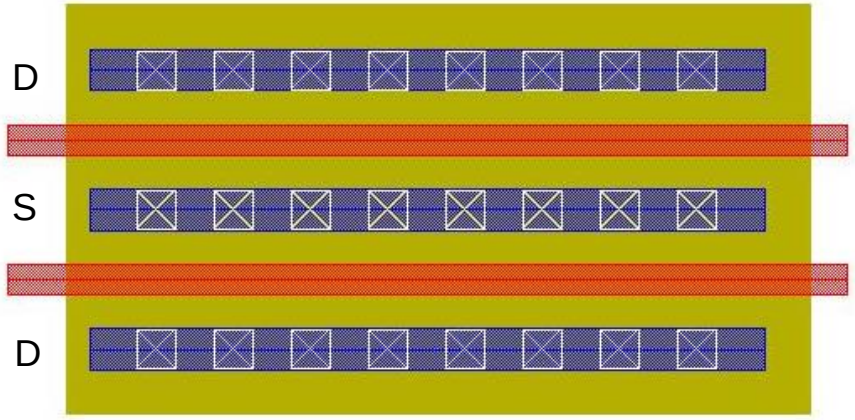
```
AA_1_2 {
@ AA width MOS transistors is 0.15
@ AA width for interconnect is 0.15
        (INT AA < 0.15 ABUT<90 SINGULAR REGION) NOT INSIDE OPCBA
}
AA_3 {
@ Space between AAs that are on the same well is 0.21 (exclude INDMY region).
X = EXT AA < 0.21 ABUT<90 SINGULAR REGION
(X NOT INSIDE OPCBA) NOT INDMY
}
AA_4 {
@ N+ AA enclosure by NW except NW resistor region is >= 0.23
ENC NACT (NW NOT NWR) < 0.23 ABUT<90 SINGULAR REGION
}
AA_5 {
@ Space between NW and N+ AA is 0.30
EXT NW NACT < 0.30 ABUT<90 SINGULAR REGION
}
AA_6 {
@ P+ AA enclosure by NW is 0.30
ENC PACT NW < 0.30 ABUT<90 SINGULAR REGION
}
AA_7 {
@ Space between NW to P+AA inside PW is 0.23
EXT (PACT AND PW) NW < 0.23 ABUT<90 SINGULAR REGION
}
AA_8 {
@ AA area is 0.1 (in um2)  AREA AA < 0.1
}
```

版图基本设计要点



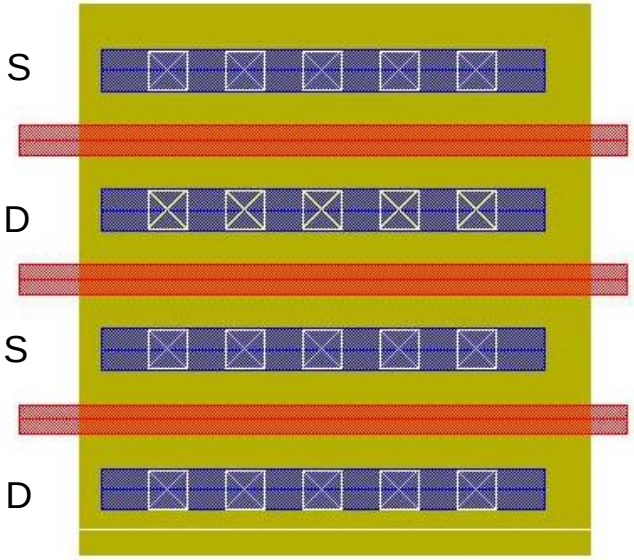
$C'_{SB}; C'_{DB}$

W/2



$$C_{SB} = \frac{1}{2} C_{DB}; C_{DB} = C'_{DB}$$

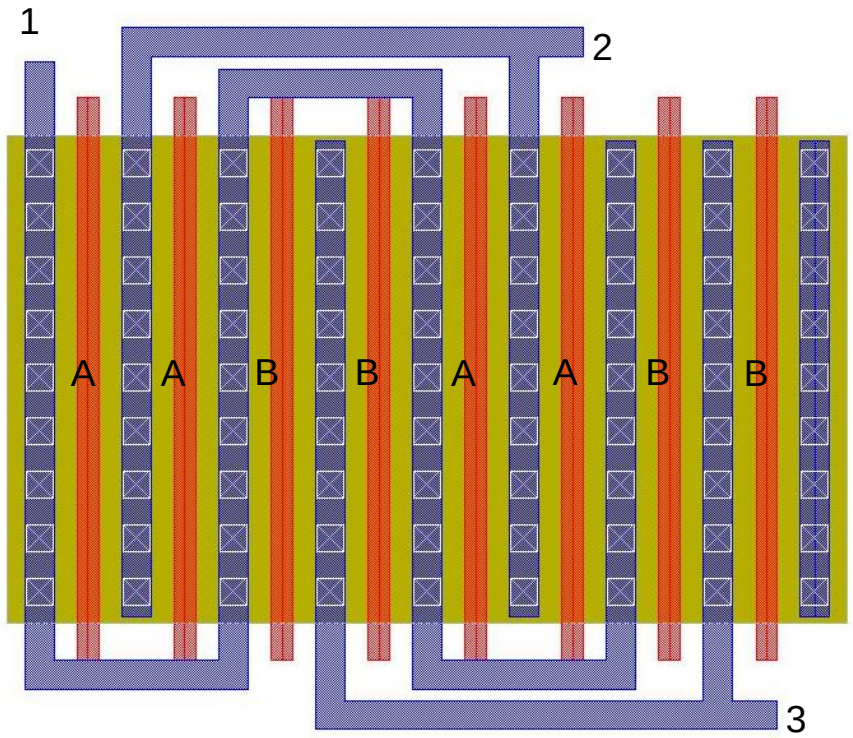
W/3

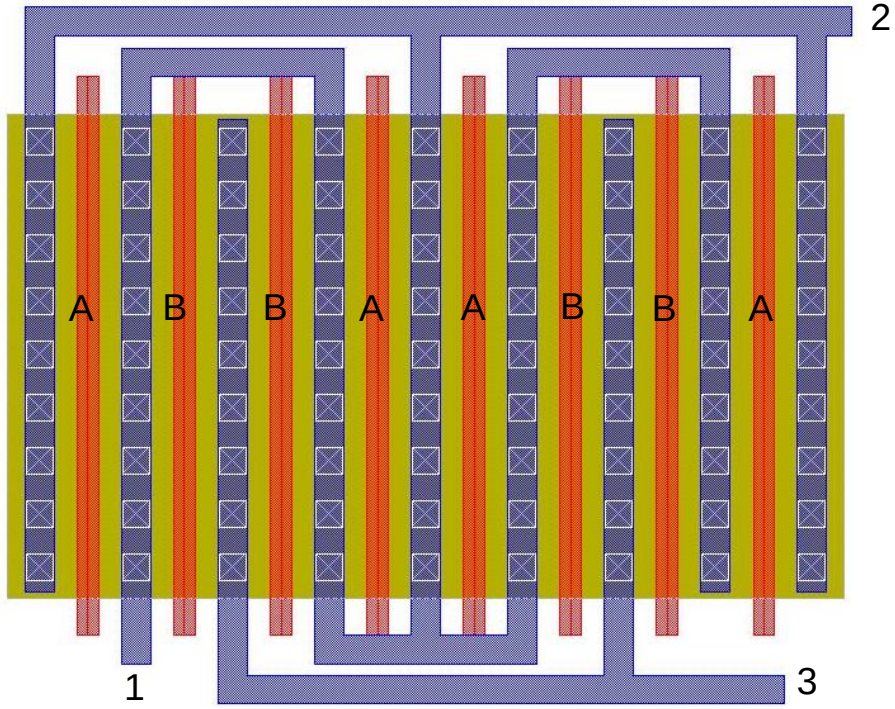


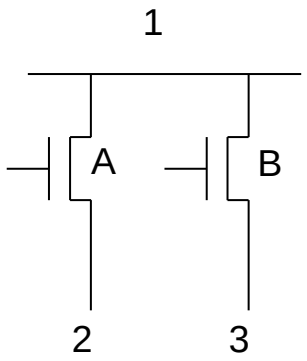
$$C_{SB} = \frac{2}{3} C'_{SB}$$

$$C_{DB} = \frac{2}{3} C'_{DB}$$

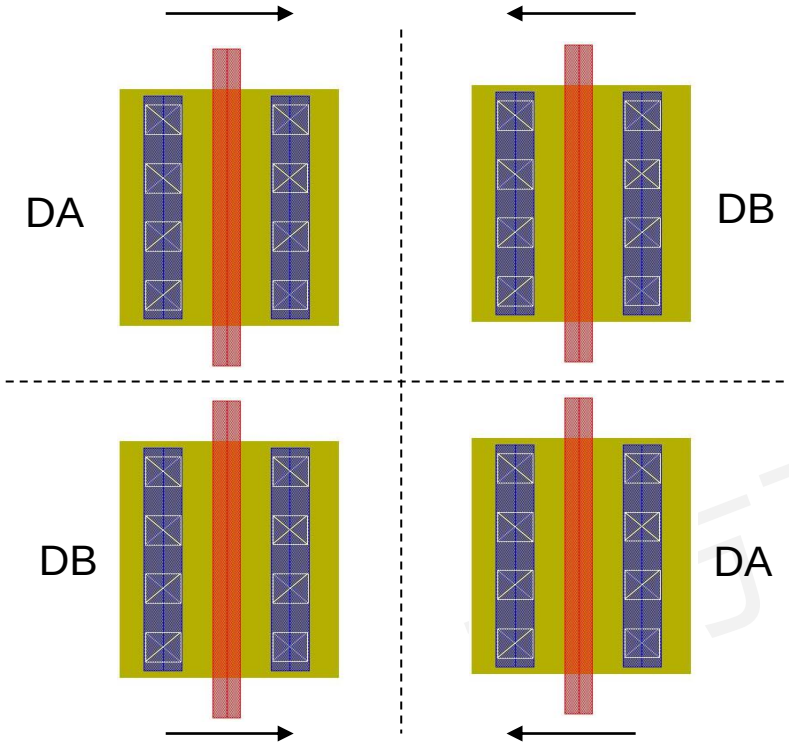
版图基本设计要点

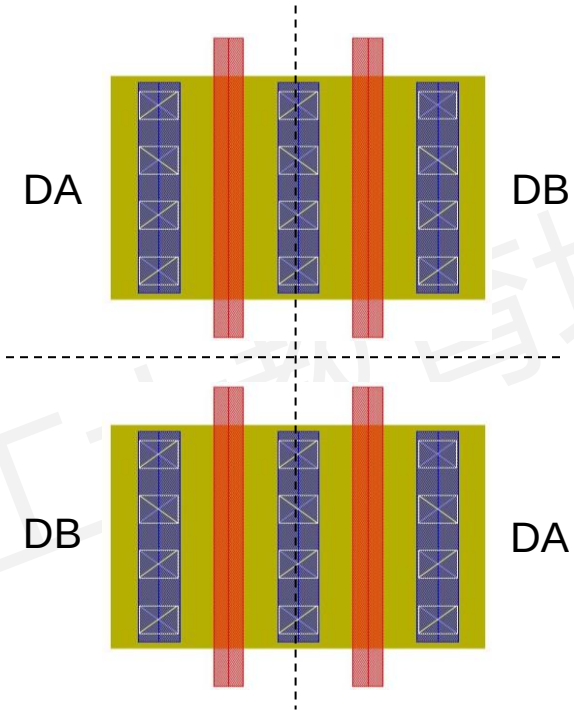


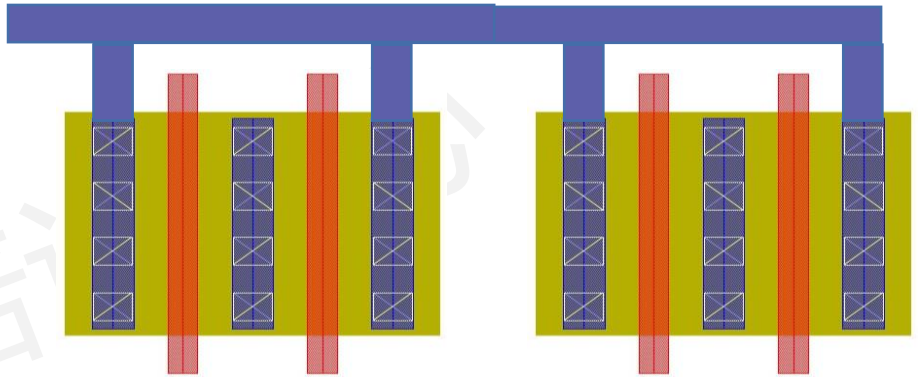


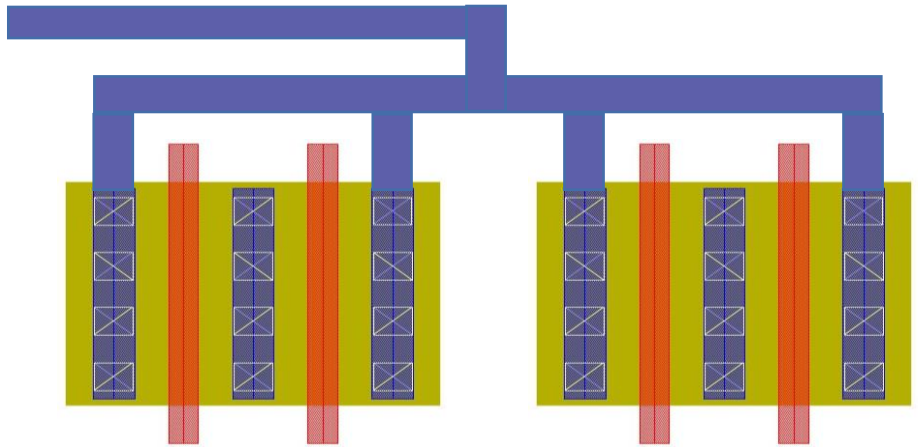


版图基本设计要点









PDK

- Process Design Kit工艺设计开发包，基于Cadence设计环境的一套模拟/混合信号设计数据包。
- PDK数据包主要内容包括technology files, device symbols, CDF, callbacks, Pcells, PV rule files, etc.

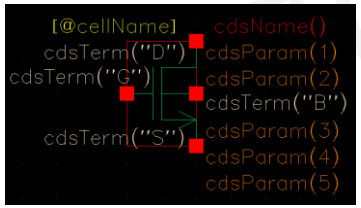
Schematic Symbols & CDF

Analog Simulation (Spectre) Models & callbacks

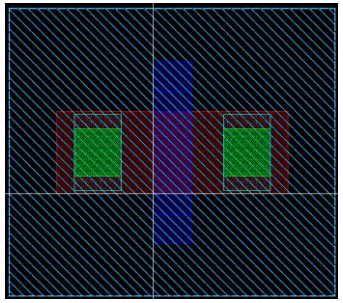
Physical Layout Parameterized Cells

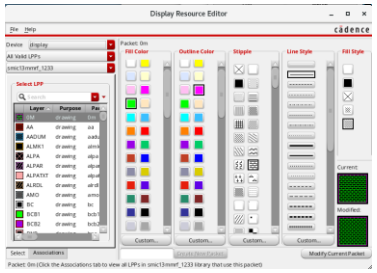
Techfile:
- Layer maps
- Layer props
- Display

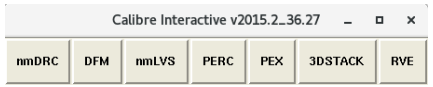
Verification Rules
- DRC
- LVS
- PEX



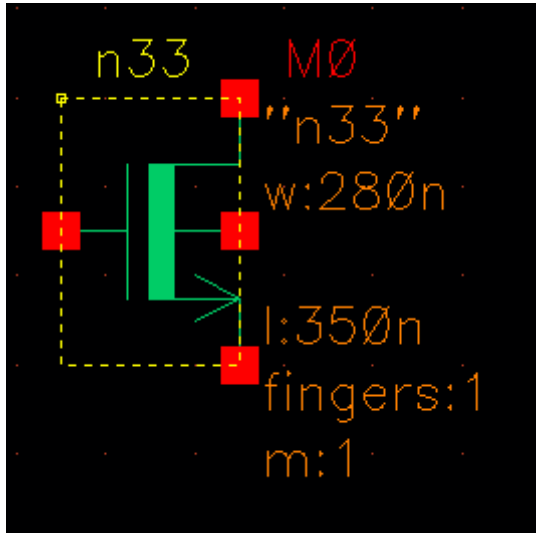
GENERAL MODEL PARAMETERS
+tnom = 25 tox =(2.58e-009+dtox_n12_rf_mismatch)
toxm = 2.58e-009 +wint = -1.25e-008 lint = 2.25e-008 dlc = 1.75e-008 +dwc = -7.5e-009
hdif = 1.25e-007 ……



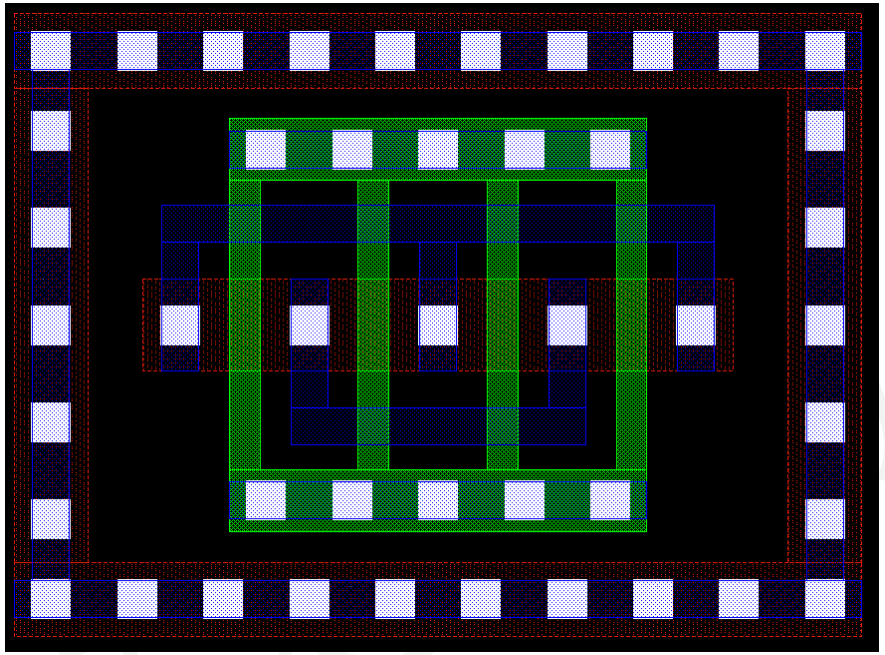




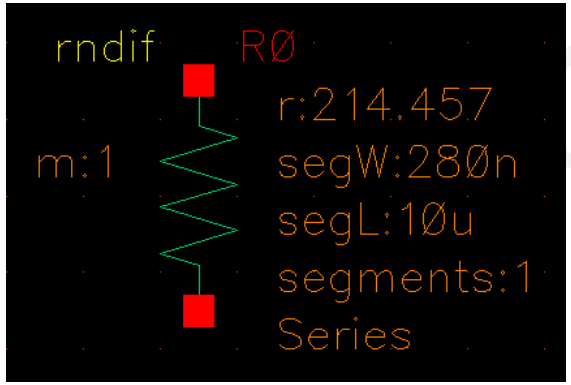
Schematic & Layout Pcells



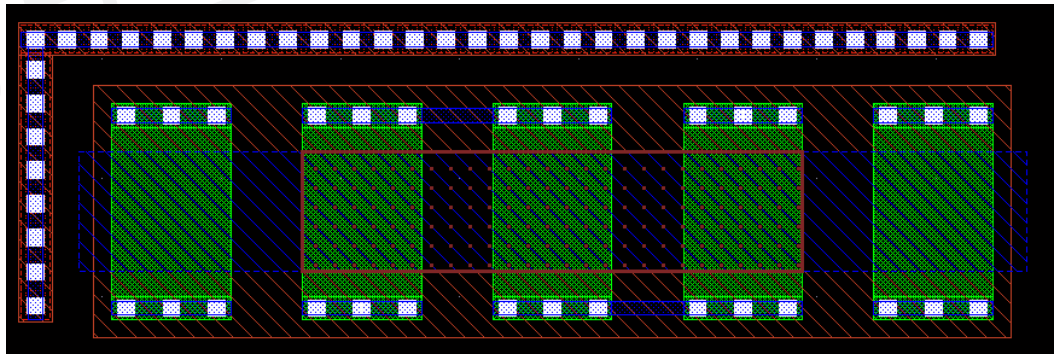
Thick Oxide NMOS



4-Fingered Mos Device with Gate Connections, S/D Connections, all Detached Body ties

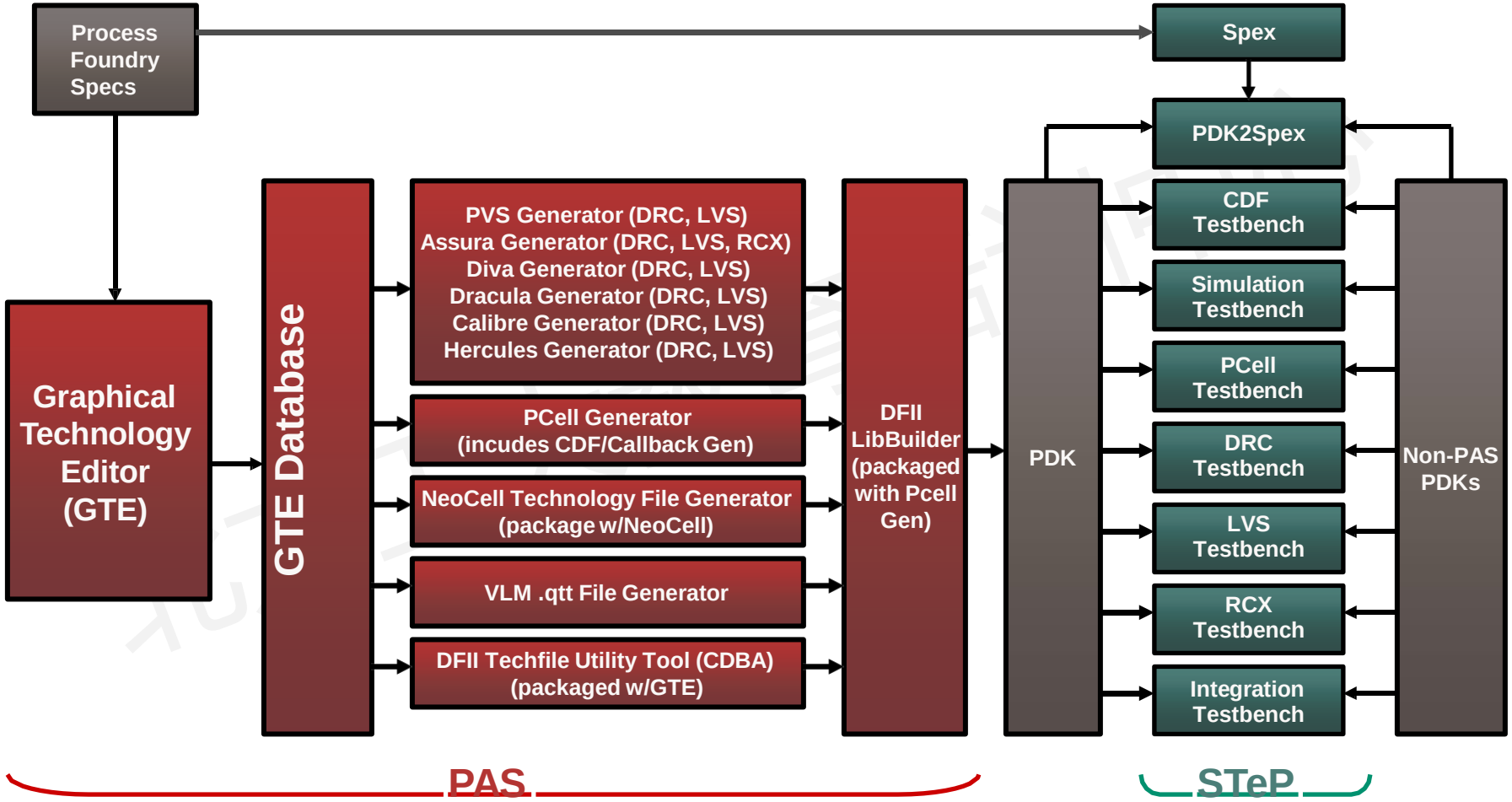


Rndif resistor



3-Segment Resistor in Series with Left & Right Dummies and Left/top body ties

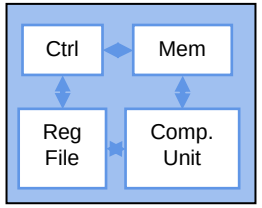
PASGTE


Process Foundry Specs
Graphical Technology Editor (GTE)
GTE Database
PVS Generator (DRC, LVS)
Assura Generator (DRC, LVS, RCX)
Diva Generator (DRC, LVS)
Dracula Generator (DRC, LVS)
Calibre Generator (DRC, LVS)
Hercules Generator (DRC, LVS)
PCell Generator (incudes CDF/Callback Gen)
NeoCell Technology File Generator (package w/NeoCell)
VLM .qtt File Generator
DFII Techfile Utility Tool (CDBA) (packaged w/GTE)
DFII LibBuilder (packaged with Pcell Gen)
PDK
Spex
PDK2Spex
CDF Testbench
Simulation Testbench
PCell Testbench
DRC Testbench
LVS Testbench
RCX Testbench
Integration Testbench
Non-PAS PDKs
PAS
STeP

- 模拟电路版图和PDK建模
- **数字标准单元版图和库模型建立**
- 工艺掩模版优化和监控
- Q&A

数字电路设计流程

Structural Description

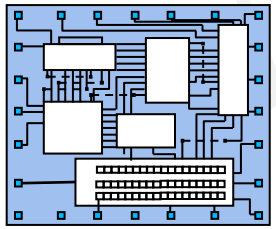


HDL Programming

Logic Synthesis

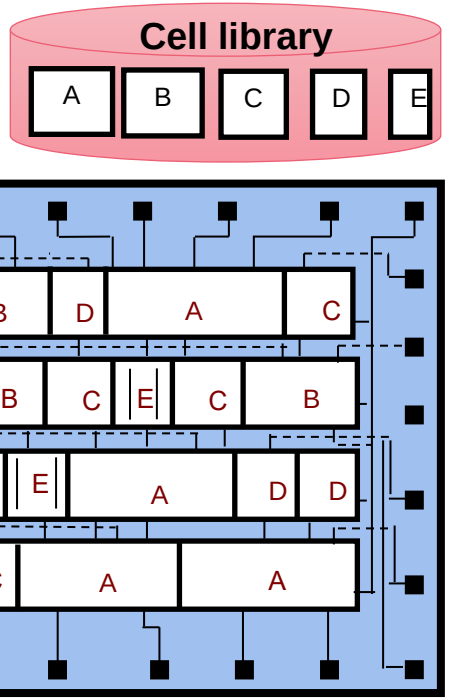
Component Design

Place & Route



Fabrication

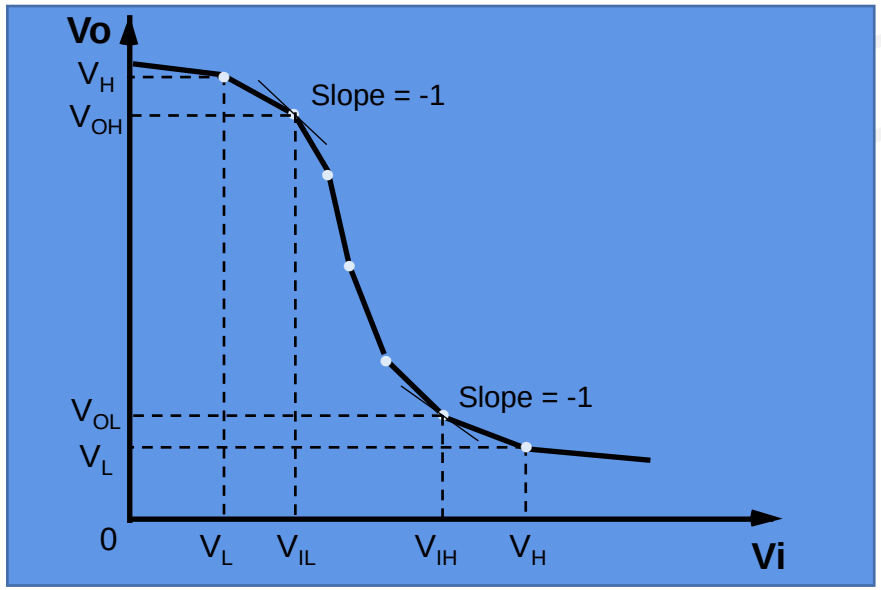
- 标准单元库，包括版图库、符号库、电路逻辑库等。包含了组合逻辑、时序逻辑、功能单元和特殊类型单元。是数字电路后端设计过程中的基础部分。
- 标准单元包括反相器、与门、寄存器、选择器、全加器等多种基本单元，每一个标准单元对应着多个不同尺寸(W/L)、不同驱动能力的单元电路，而且不同驱动强度电路都是基本尺寸或最小尺寸的整倍数。
- 模块单元(block)包括各种规模的数字模块:RAM、ROM、COT、IP、电压比较器等，也包括模拟模块:运算放大器、ADC/DAC、锁相环、振荡器等
- 芯片与PCB通信的接口电路统称为 I/O 电路。它作为芯片与外界通信的接口必须具有较大的驱动能力，抵御静电放电的能力，抗噪声干扰的能力以及足够的带宽和过电保护功能。

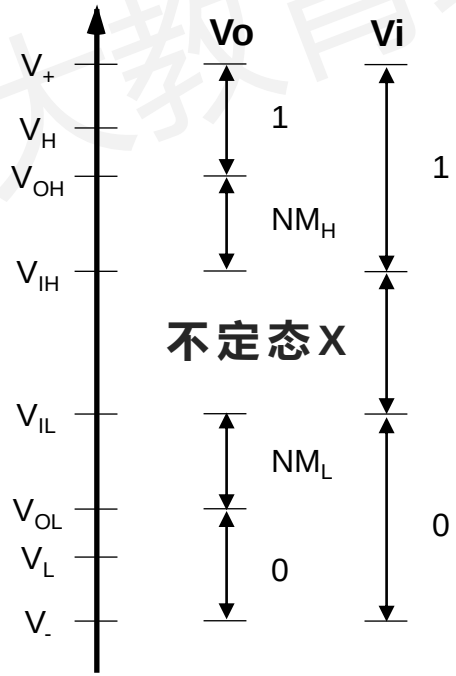


逻辑门的电平定义及噪声容限

数字逻辑电路即二值逻辑，只有两个分立的状态，正逻辑的高电平对应逻辑1，低电平对应逻辑0。理想逻辑门的输出只有两种可能的电压电平：V_H对应逻辑1状态，V_L对应逻辑0状态。当理想逻辑门的输入超过规定参考电压V_{ref}时，输出将立即改变状态，然而实际中的逻辑状态并没有界定精确的参考电压。V_{IL}和V_{IH}有电压传输特性曲线上斜率等于-1的点对应的输入电压进行定义，这些电压定义了逻辑1和逻辑0之间转换区域的边界。

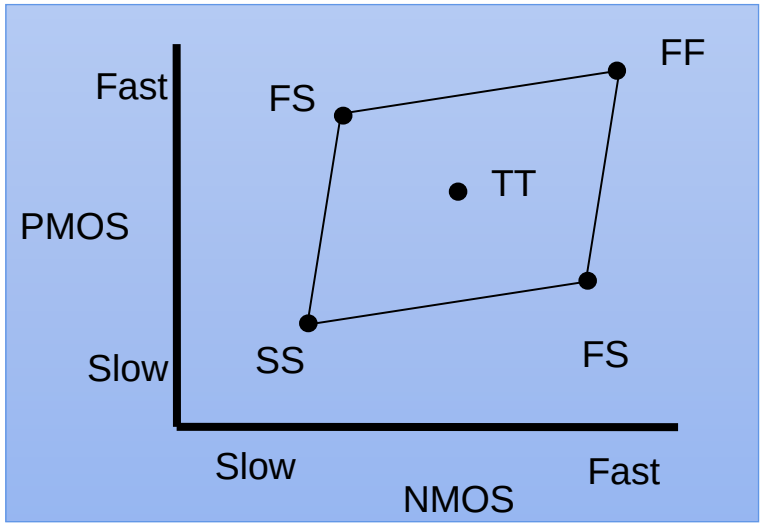
噪声容限表示逻辑门抑制外来信号的能力，对于逻辑门而言非常重要。高电平状态和低电平状态的噪声容限分别被定义为$NM_H=V_{OH}-V_{IH}$和$NM_L=V_{IL}-V_{OL}$。电压V_{OL}和V_{OH}代表的是在斜率为-1处的逻辑门输出电压，对应的输入电平分别为V_{IL}和V_{IH}。





SYMBOL	PARAMETER	CONDITION	MINIMUM	MAXIMUM	UNIT
V_{IH}	High-level input voltage	(TTL)	2.4		V
V_{IL}	Low-level input voltage	(TTL)		0.8	V
V_{OL1}	Low-level output voltage	I_{OL} = 4.0mA, V_{DD} = 4.5V (TTL)		0.4	V
V_{OL2}	Low-level output voltage	I_{OL} = 200μA, V_{DD} = 4.5V (CMOS)		V_{SS} + 0.10	V
V_{OH1}	High-level output voltage	I_{OH} = -200μA, V_{DD} = 4.5V (CMOS)	V_{DD} -0.1		V
V_{OH2}	High-level output voltage	I_{OH} = -2.0mA, V_{DD} = 4.5V (TTL)	2.4		V

基本单元INVX1电路设计



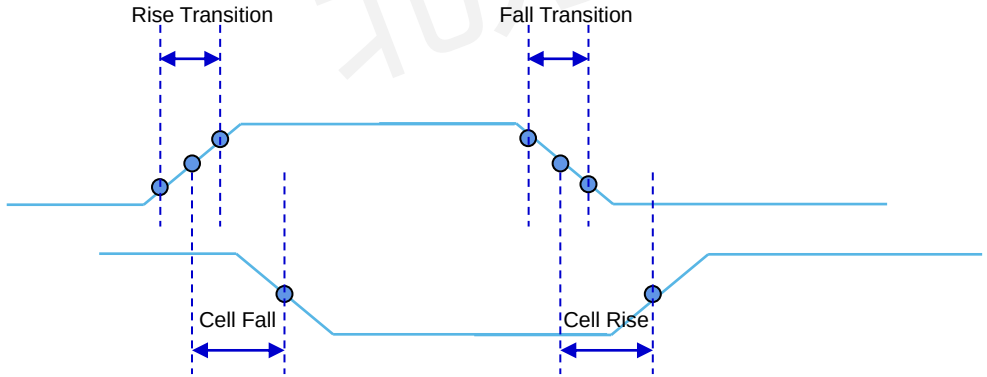
Process: Fast
Temp: 125°
Voltage: 1.32v

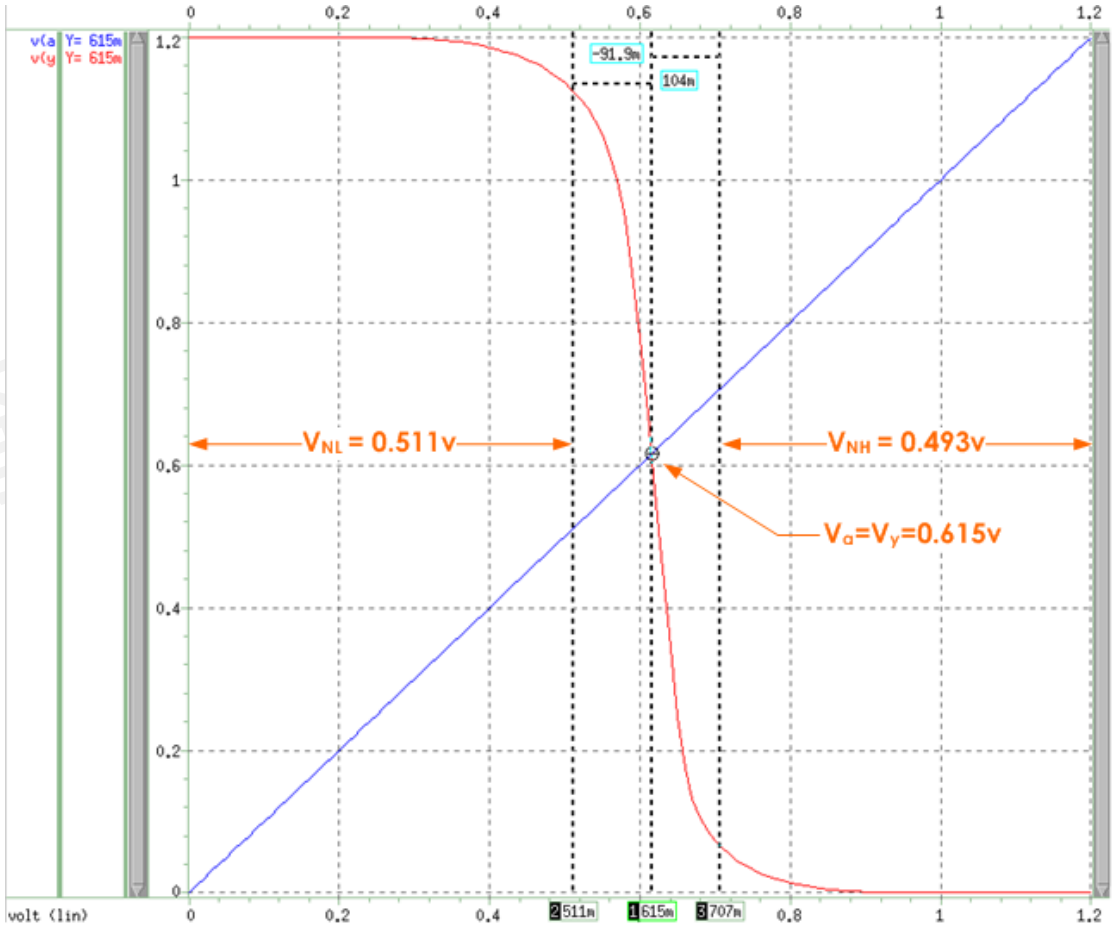
Process: Slow
Temp: -40°
Voltage: 1.08v

Process: Typical
Temp: 25°
Voltage: 1.2v

一个好的反相器设计需要考虑两个方面：

- **均衡的上升和下降渡越时间；**
- **均衡的上升和下降传播延时时间**

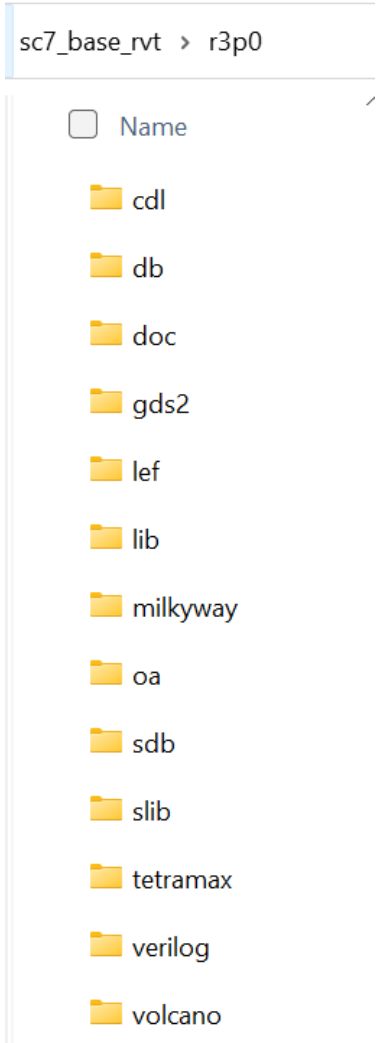




直流特性仿真，噪声容限

V_{NL}=0.511V，V_{NH}=0.493V

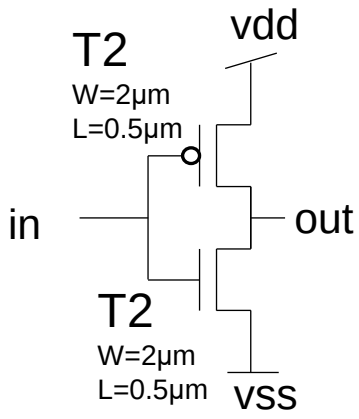
数字标准单元库



- CDL：网表信息文件，主要用于LVS检查和转换回原理图
- DB：用于Synopsys Design Compiler工具的综合时序库，由.lib文件转换而成
- DOC：单元库说明文档
- GDS2：单元库中所有单元的版图文件
- LEF：主要分为Tech LEF和Cell LEF，Tech LEF主要定义的是布局布线的设计规则和晶圆厂的工艺信息，Cell LEF主要用于定义标准单元的物理信息。定义单元的放置区域，对称性，面积大小，单元输入输出端口的布线层、几何形状、不可布线区域以及天线效应参数供布线使用。主要用于Cadence Encounter后端布局布线工具
- LIB：主要包含Cell时序，延时和功耗等信息
- MILKYMAY：包含CEL、FRAM两种数据格式，其中CEL中包含单元版图中所有层的信息，FRAM中是各个单元版图的抽象信息，包括单元的放置区、pin的位置、布线层的信息。Milkyway格式是Synopsys专用的物理库格式，用于ICC后端工具
- VERILOG：提供verilog模型，行为级网表，用于verilog网表仿真

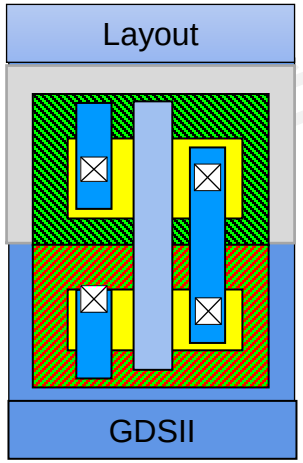
。。。。。。

CDL & GDSII



Inverter.sp

```
.subckt inverter
        mt1 out in vdd nmos l = 0.5u w = 2u
        mt2 out in vdd pmos l = 0.5u w = 2u
.ends
```



Inverter.gds

```
02000200 60000201 1C000300 02000600 .........`.... 000000
01000E00 02000200 60002500 01000E00 .....%.`........ 000010
42494C45 4C504D41 58450602 12002500 .%....EXAMPLELIB 000020
413E0503 14000300 02220600 59524152 RARY.."......>A 000030
1C00545A 9BA02FB8 4439EFA7 C64B3789 .7K...9D./..ZT.. 00004
60000000 01000E00 02000200 60000205 ...`.........` 000050
58450606 0C001100 01000E00 02000200 .............EX 000060
0100020D 06000008 04000045 4C504D41 AMPLE..... 000070
0000F0D8 FFFF0310 2C000000 020E0600 .....,..... 000080
FFFF204E 00001027 0000204E 00001027 '...N ..'...N .. 000090
0000F0D8 FFFFF0D8 FFFFF0D8 FFFFF0D8 ..... 0000A0
00000004 04000007 04000011 04001027 '..... 0000B0
00000000 00000000 00000000 00000000 ..... 0000C0
```

LIB & DB

Liberty (*.lib) format

```
cell ( OR2_4x ) {
    area : 8.000 ;
    pin ( Y ) {
        direction : 2;
        timing ( ) {
            related_pin : "A" ;
            timing_sense : positive_unate ;
            rise_propagation (drive_3_table_1) {
                values ("0.2616, 0.2711, 0.2831,..)
            }
            rise_transition (drive_3_table_2) {
              values ("0.0223, 0.0254, ...)
                    . . . .
        function : "(A | B)";
        max_capacitance :  1.14810 ;
        min_capacitance :  0.00220 ;
   }
    pin ( A ) {
        direction : 1;
        capacitance : 0.012000;
                    . . . .
```

Cell name

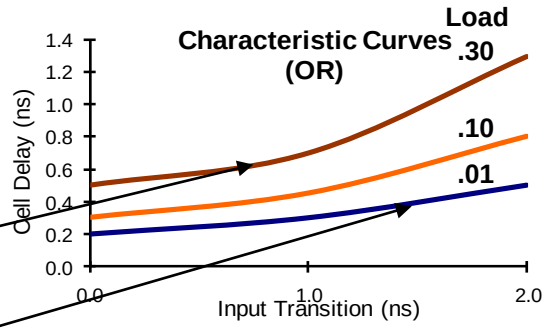
Cell Area

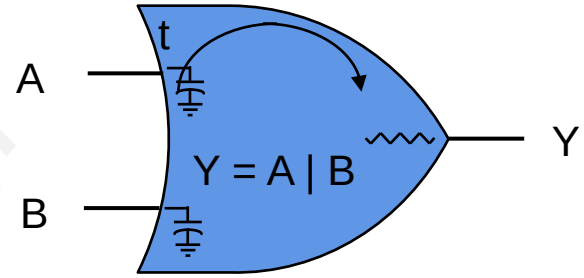
2 = Output; 1 = Input

Pin Y Functionality

Design Rules for Pin Y

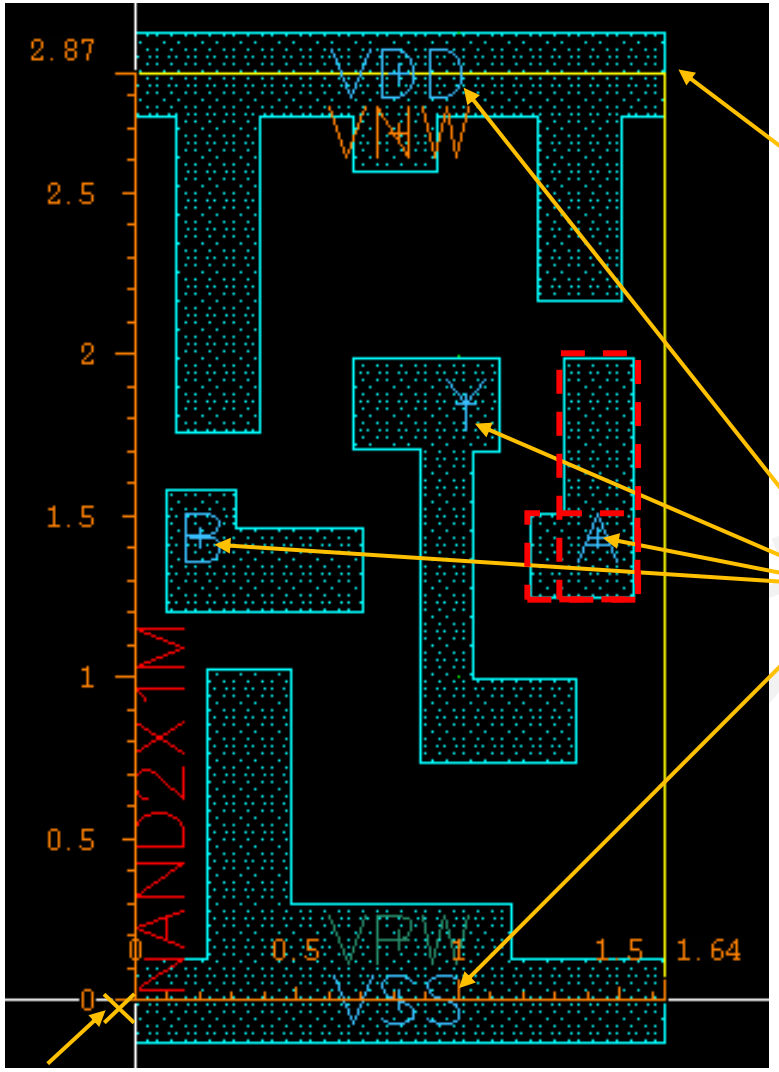
Electrical Characteristics of Pin A





Corner Name	Process (NMOS proc. – PMOS proc.)	Temperature (T)	Power Supply (V)	Notes
TTNT1p20v	Typical - Typical	25	1.2	Typical corner
SSHT1p08v	Slow - Slow	125	1.08	Slow corner
FFLT1p32v	Fast - Fast	-40	1.32	Fast corner
FFHT1p32v	Fast - Fast	125	1.32	High leakage corner
SSLT1p32v	Slow - Slow	-40	1.32	Low temperature corners
SSLT1p08v	Slow - Slow	-40	1.08	
Low Voltage Operating Conditions				
TTNT0p80v	Typical - Typical	25	0.80	Typical corner
SSHT0p70v	Slow - Slow	125	0.70	Slow corner
FFLT0p90v	Fast - Fast	-40	0.90	Fast corner
FFHT0p90v	Fast - Fast	125	0.90	High leakage corner
SSLT0p90v	Slow - Slow	-40	0.90	Low temperature corners
SSLT0p70v	Slow - Slow	-40	0.70	

MILKYWAY & LEF



Dimension
“bounding box”

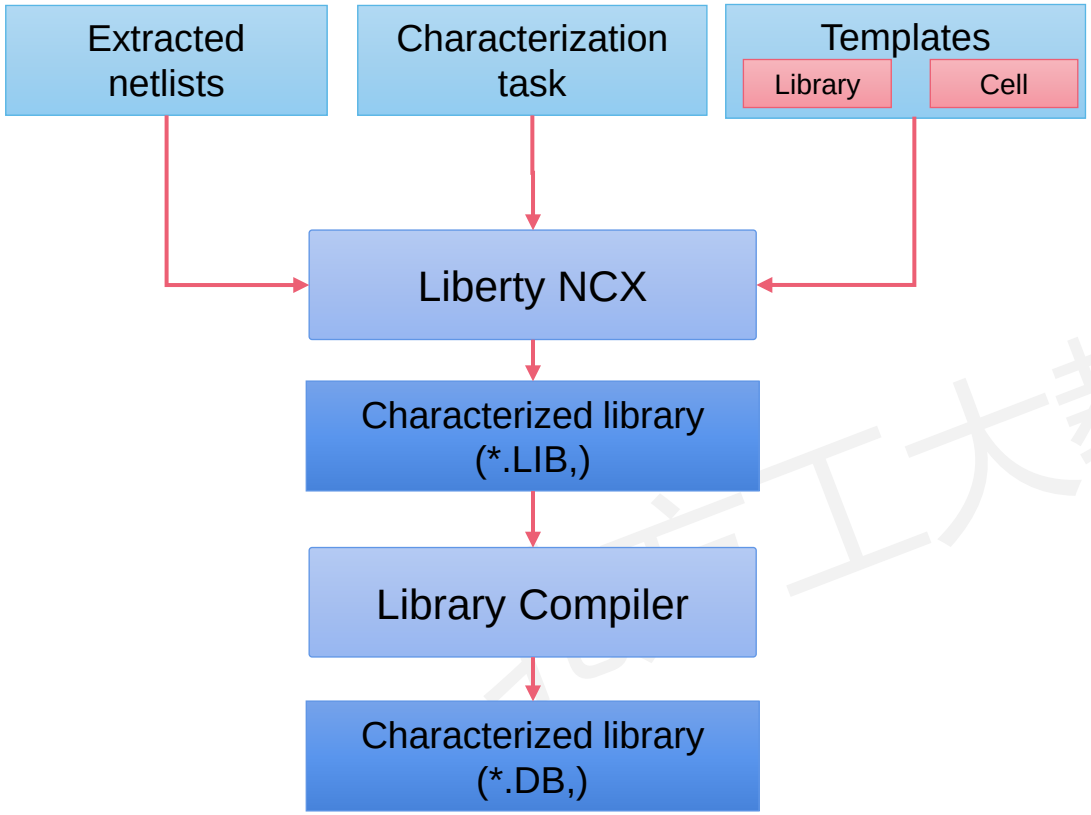
Pins
(direction, layer
and shape)

reference point
(typically 0,0)

NAND2X1

```
MACRO NAND2X1M
  CLASS CORE ;
  ORIGIN 0 0 ;
  FOREIGN NAND2X1M 0 0 ;
  SIZE 1.64 BY 2.87 ;
  SYMMETRY X Y ;
  SITE sc7_logic013 ;
  PIN A
    DIRECTION INPUT ;
    USE SIGNAL ;
    ANTENNAMODEL OXIDE1 ;
     ANTENNAGATEAREA 0.1274 LAYER METAL1 ;
    PORT     LAYER METAL1 ;
      RECT 1.225 1.25 1.54 1.51 ;
      RECT 1.33 1.25 1.54 1.99 ;
    END  END A
  PIN B
……
  PIN Y
    DIRECTION OUTPUT ;
    USE SIGNAL ;
    ANTENNADIFFAREA 0.3611 LAYER METAL1 ;
    PORT
      LAYER METAL1 ;
        RECT 0.885 0.735 1.045 1.99 ;
        RECT 0.885 1.7 1.13 1.99 ;
        RECT 0.675 1.71 1.13 1.99 ;
        RECT 0.885 0.735 1.365 0.995 ;
    END
  END Y
END NAND2X1M
```

数字标准单元库模型建立



Library Template

```
ncx_input_transition_time_index : 0.016 0.032 0.064… ;
ncx_constrained_pin_transition_index : 0.016 0.032 0.064…;
ncx_input_net_transition_index : 0.016 0.032 0.064… ;
ncx_related_pin_transition_index : 0.016 0.032 0.064… ;\
ncx_total_output_net_capacitance_index :0.1  0.25 0.5… ;
 …
technology : cmos ;
delay_model : table_lookup ;
capacitive_load_unit : 1.0000000 ff ;
default_leakage_power_density : 0.0;
input_threshold_pct_rise : 50.0000000 ;
slew_lower_threshold_pct_rise : 20.0000000 ;
default_fanout_load : 1.0000000 ;
library_features : report_power_calculation ;
…
normalized_driver_waveform driver_waveform_template {
  driver_waveform_name : preDrv ;
  index_1 : index list
  index_2 :  index list
  values : value array
}
```

Indexes

Lib information

Attribute data for characterization

数字标准单元库模型建立

Cell Template

```
pg_pin VDD {
  voltage_name : VDD ;
  pg_type : primary_power ;
}
pg_pin VSS {
….
}
```

Power/Ground Pins

```
pin <input_pin_name> {
  related_power_pin : VDD ;
  related_ground_pin : VSS ;
  direction : input ;
}
pin <output_pin_name> {
  related_power_pin : VDD ;
  related_ground_pin : VSS ;
  direction : output ;
  function : A*B ;
}
```

Pins

Function

```
 sensitization {
   <input_pin_name> : <output_pin_name> ;
   01 : r ;
   10 : f ;
}
```

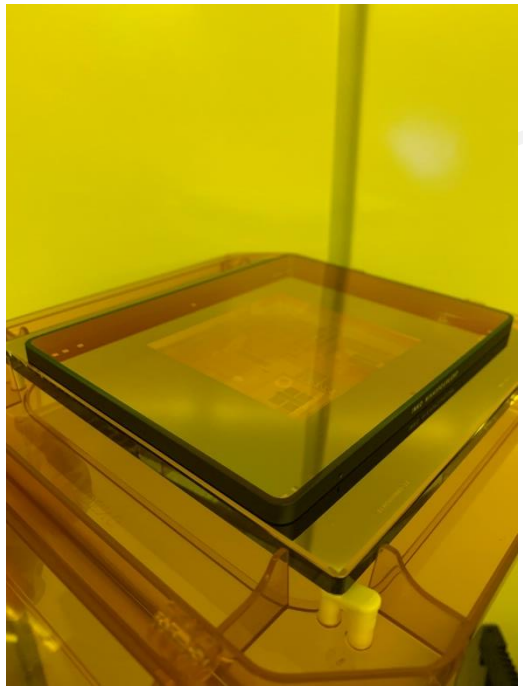
Sensitization

```
cell(NAND2X1M) {
    area : 4.7068 ;
    cell_footprint : nand2 ;
……
 timing() {
       related_pin : "A" ;
       sdf_cond : "B==1'b1" ;
       timing_sense : negative_unate ;
       timing_type : combinational ;
       when : "B" ;

       cell_fall(tmg_ntin_oload_7x7) {
         index_1("0.00476, 0.0398954, 0.163228, 0.39875, 0.765682, \
                  1.28053, 1.958");
        index_2("0.0001, 0.00387505, 0.0171263, 0.0424315, \
                  0.0818558, 0.137173, 0.209962");
        values("0.0214293, 0.0411068, 0.108922, 0.2381, 0.439198, 0.721519, 1.09312",\
               "0.0290418, 0.0494663, 0.117826, 0.247197, 0.448512, 0.73079, 1.10237",\
               "0.0400375, 0.0730273, 0.150395, 0.279832, 0.481246, 0.76363, 1.13518",\
               "0.0468113, 0.0922862, 0.199736, 0.343575, 0.544587, 0.826751, 1.19781",\
               "0.0484177, 0.10635, 0.242618, 0.425859, 0.644428, 0.926106, 1.29705",\
               "0.0439357, 0.114558, 0.279035, 0.500766, 0.765143, 1.06676, 1.43691",\
               "0.0329601, 0.115944, 0.309036, 0.567546, 0.877771, 1.2304, 1.62232");
       }

       cell_rise(tmg_ntin_oload_7x7) {
         index_1("0.00476, 0.0398954, 0.163228, 0.39875, 0.765682, \
                  1.28053, 1.958");
        index_2("0.0001, 0.00387505, 0.0171263, 0.0424315, \
                  0.0818558, 0.137173, 0.209962");
        values("0.0186953, 0.0370294, 0.0993295, 0.218022, 0.402689, 0.661781, 1.00272",\
               "0.0292974, 0.048193, 0.111194, 0.23013, 0.414712, 0.67374, 1.01504",\
               "0.0501557, 0.0818763, 0.153179, 0.272181, 0.457162, 0.716396, 1.05709",\
               "0.074659, 0.11943, 0.222188, 0.354017, 0.538452, 0.797871, 1.13885",\
               "0.103369, 0.161006, 0.294239, 0.467099, 0.666825, 0.925234, 1.26544",\
               "0.136302, 0.207152, 0.369761, 0.583757, 0.830982, 1.10604, 1.44624",\
               "0.173792, 0.258353, 0.450101, 0.703022, 0.999281, 1.32618, 1.68349");
       }
       fall_transition(tmg_ntin_oload_7x7) {
……
       }
       rise_transition(tmg_ntin_oload_7x7) {
……..
       }
```

- 模拟电路版图和PDK建模
- 数字标准单元版图和库模型建立
- **工艺掩模版优化和监控**
- Q&A

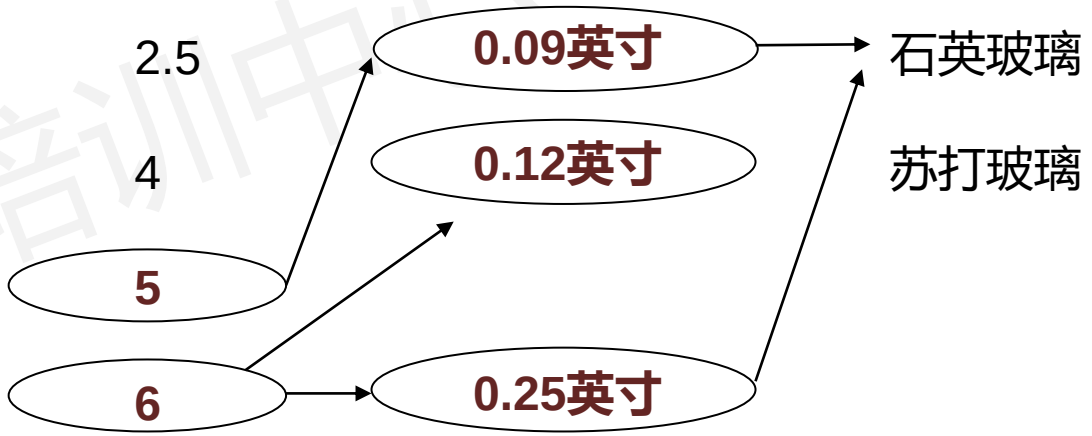
光刻掩模版

- 掩模是一种统称，又名光掩模或是光罩(Mask，PhotoMask，Reticle)
- 掩模是一个在石英/苏打基板上以铬膜所构成之集成电路(IC)设计图案
- 其目的是为了将设计出的集成电路图案利用掩模投影微缩转移至晶圆上



图形对比　尺寸大小　玻璃厚度　玻璃材质

Mask-->Wafer	Inch	Mil
1 X	2.5	
2.5X	4	
4 X	5	
5 X	6	

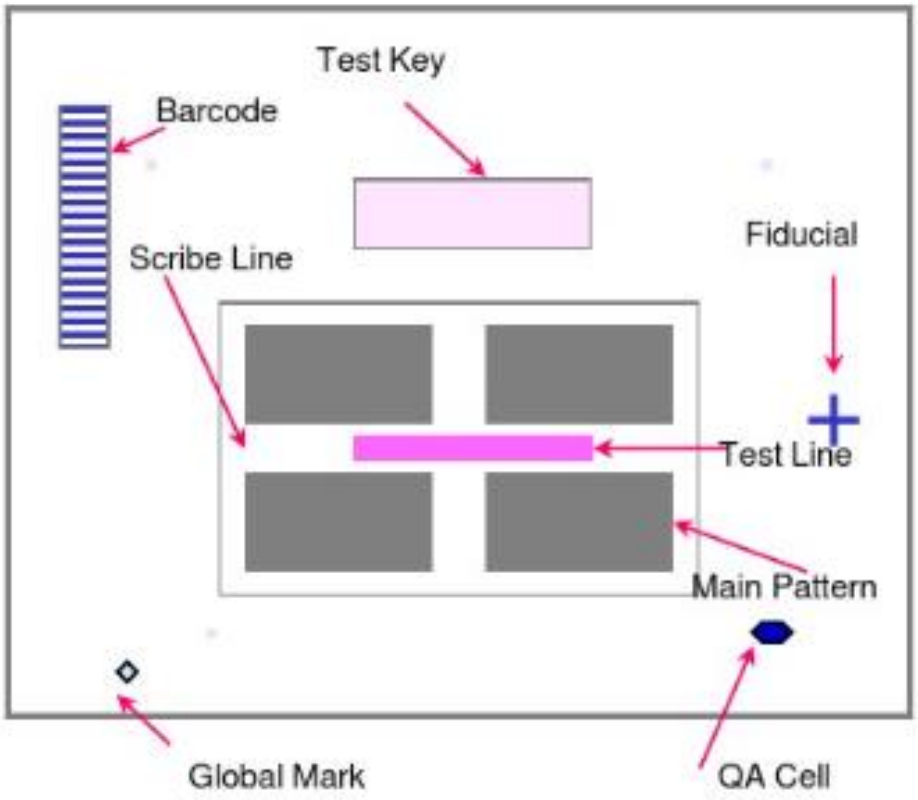


Size of 8inch Wafer Mask

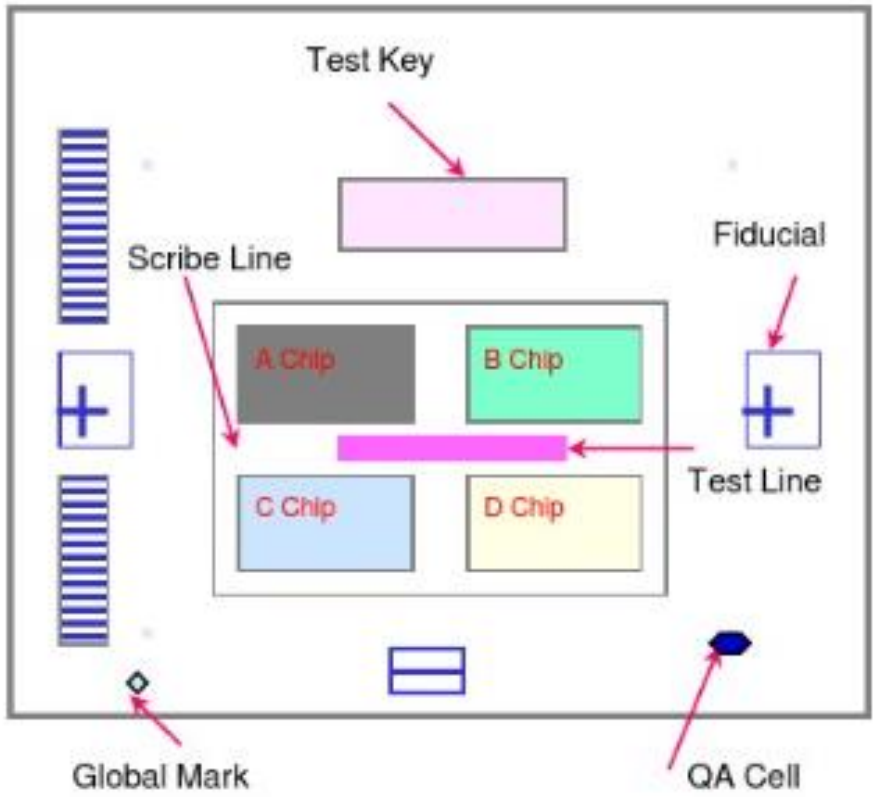
5inch 90mil(5009)	5inch 180mil(5018)
6inch 120mil(6012)	6inch 250mil(6025)
7inch 250mil(7015)	

光刻掩模版布局

Normal



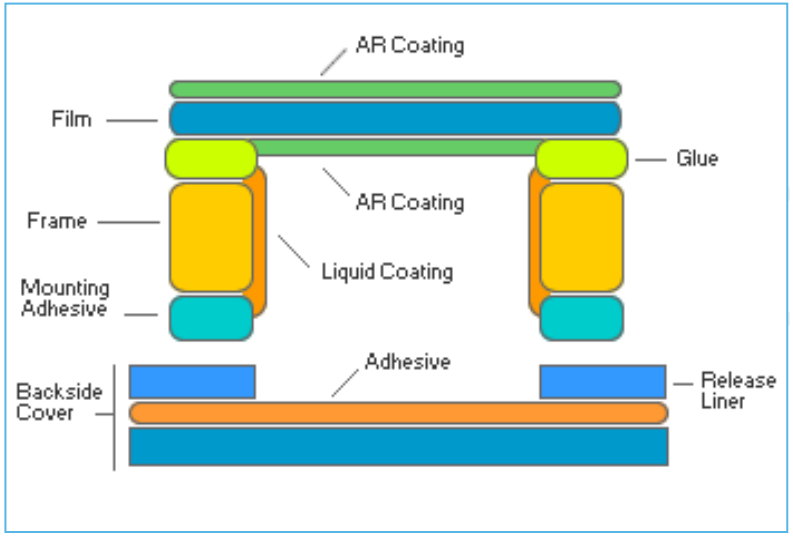
Multi-Chip

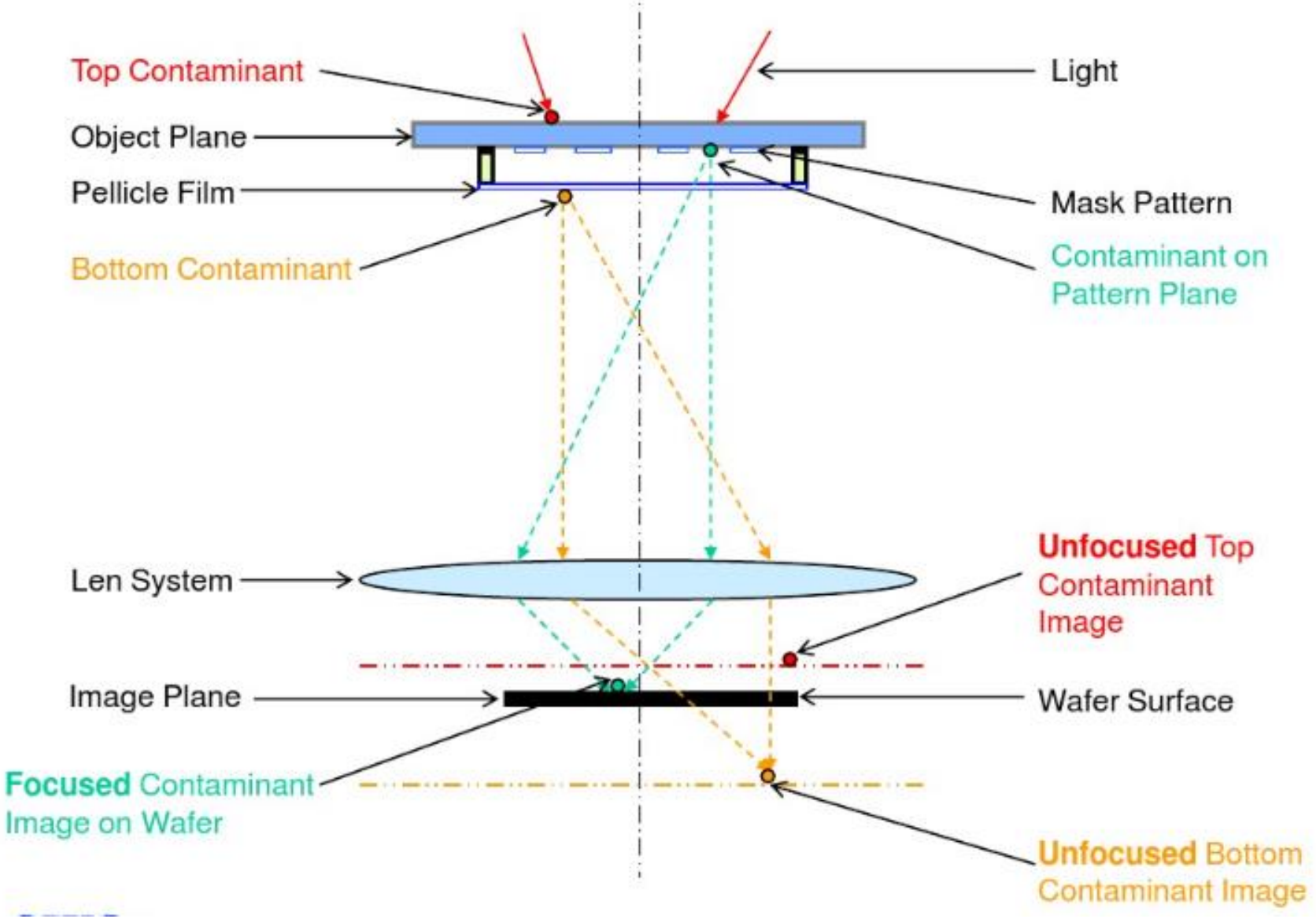


光刻掩模版薄膜

Membrane

Material	Wave Length
N.C.	365nm (I-line)
C.E.	365, 248nm (I-line, DUV)
F.C.	193nm (ArF)





光刻掩模版制造

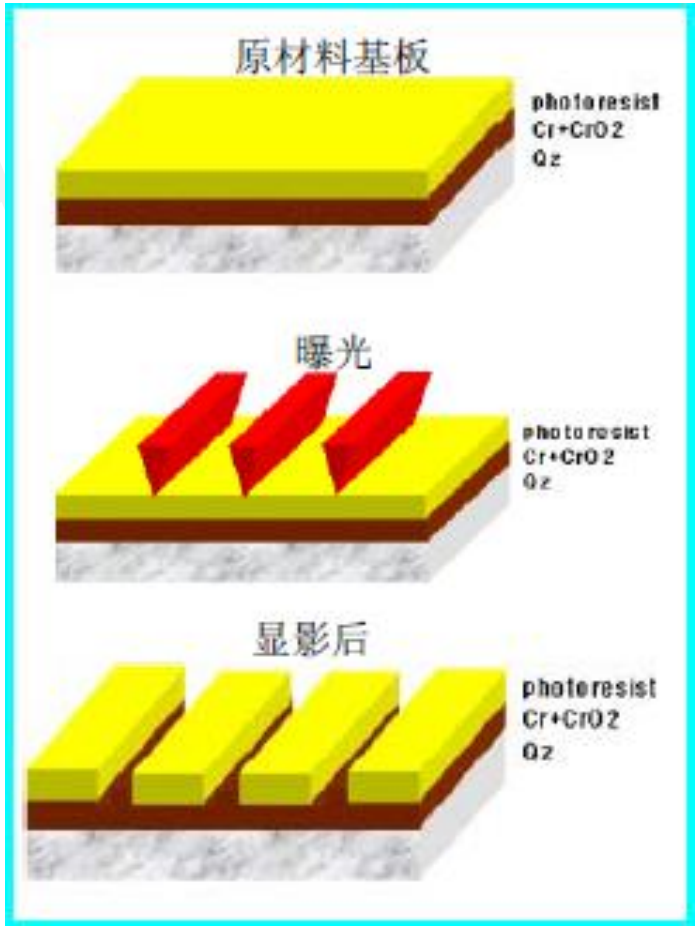
曝光 → 显影 → 刻蚀 → 去胶

Front -End

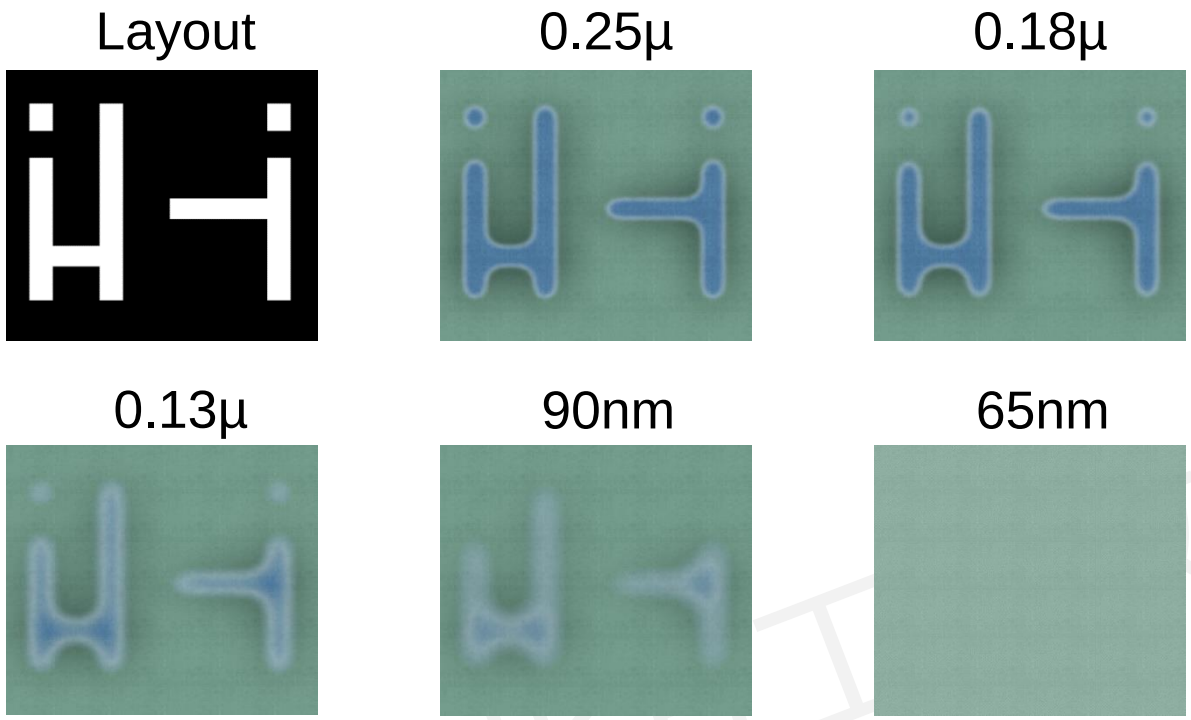
Back- End

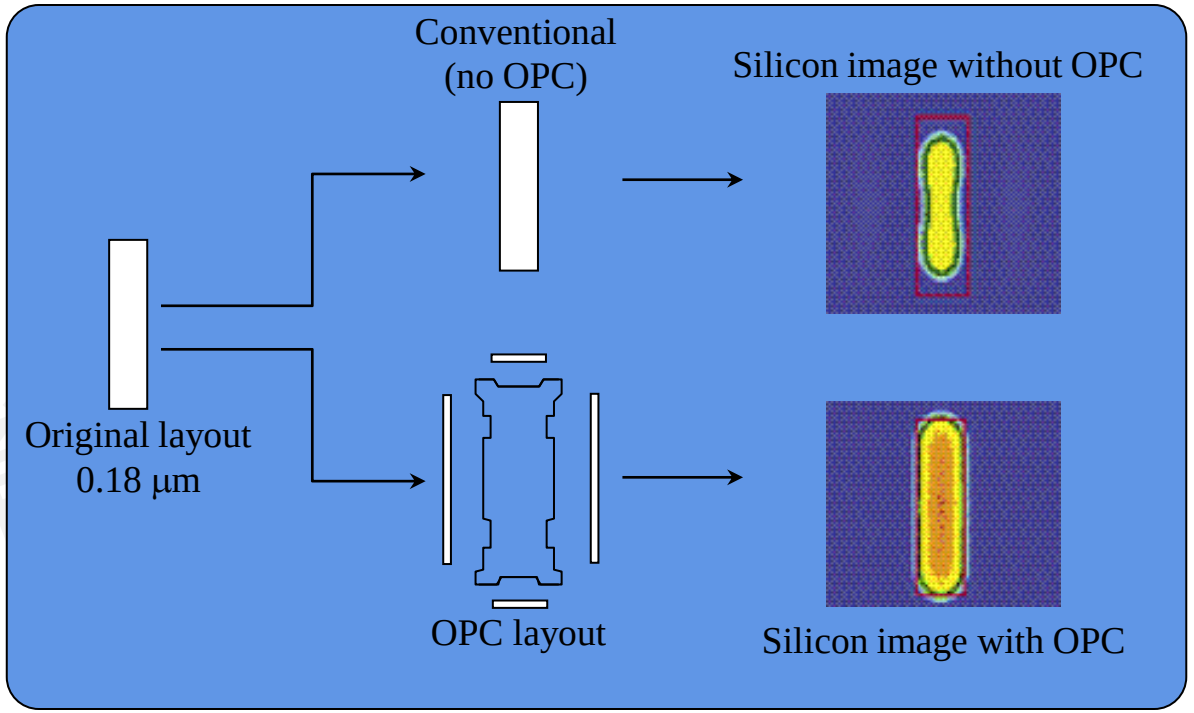
贴膜 ↔ 清洗 ↔ 修补 ↔ 检验

再检验 ↔ 包装出货



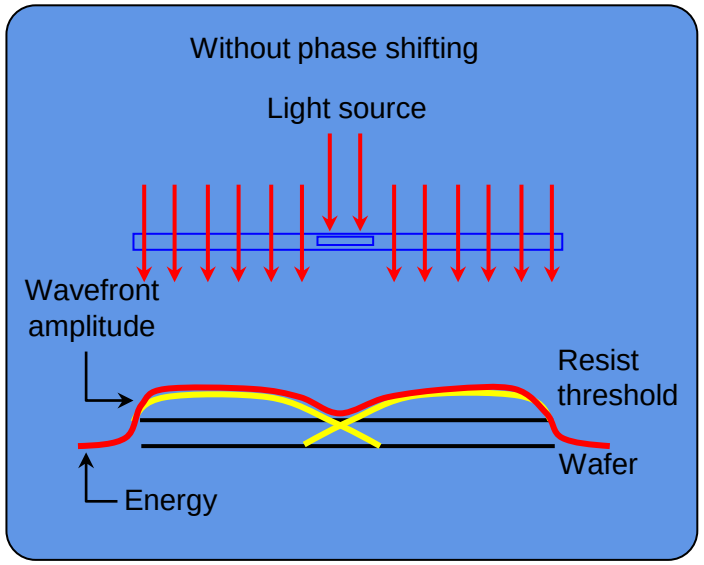
掩模版图形优化-OPC

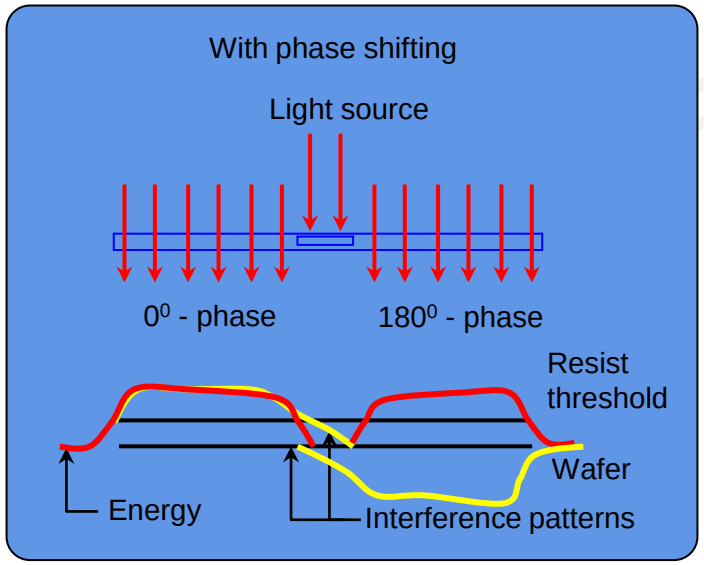


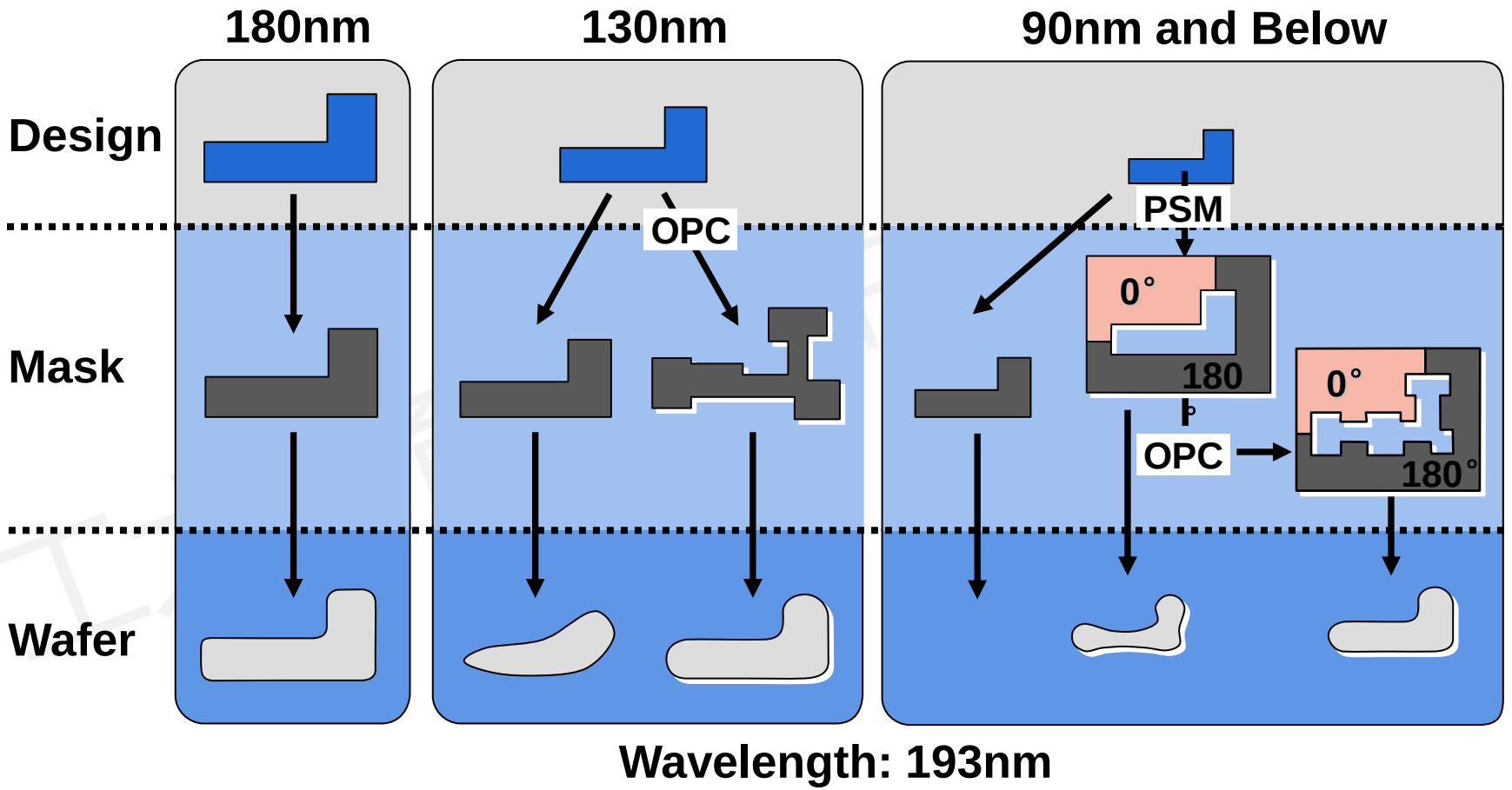


OPC – Optical Proximity Correction，光学临近效应修正是一种光刻增强技术，目的是为了保证生产过程中设计的图形的边缘得到完整的刻蚀。在掩模版上图形的边缘**通过添加额外的多边形**来纠正这些错误。根据宽度和间距约束（即**基于规则**的OPC），或者是通过使用紧凑的模型动态仿真(即**基于模型**的OPC)的结果预先计算出一个查找表，根据这个查找表来决定怎样改变图形边缘形状，最终找到最优解决方案。

掩模版图形优化-PSM

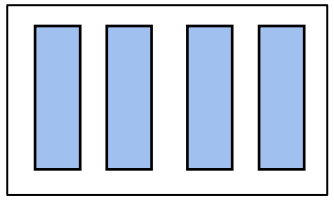


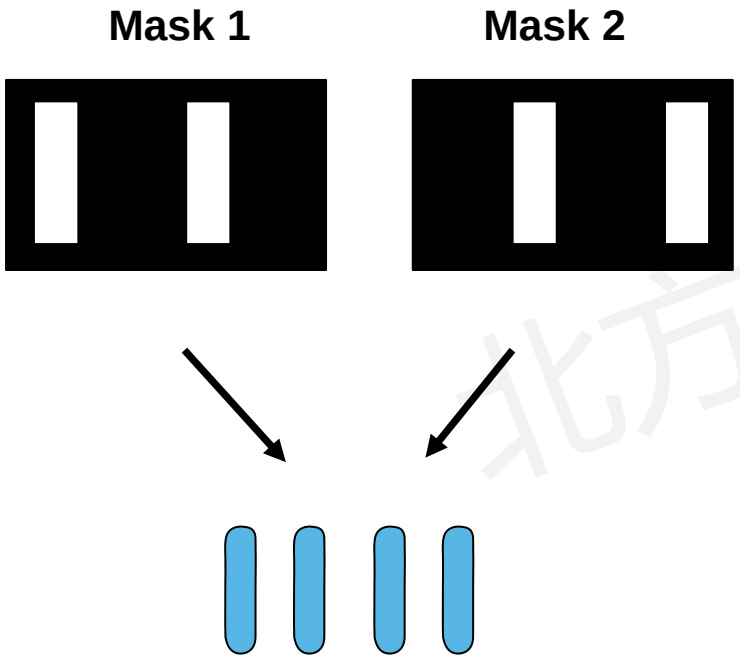


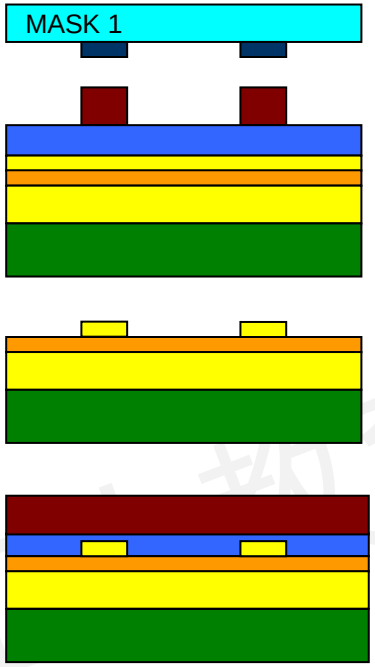


PSM – Phase Shift Mask,**通过改变掩膜结构**，减少临近效应，利用光的相干性，抵消部分衍射扩展效应，改变空间光强分布，使更多的能量从低频分配到高频上，弥补投影物镜通低频阻高频的缺点，提高空间图像的反差，改变像质，使分辨率和焦深增大

掩模版图形优化-DP



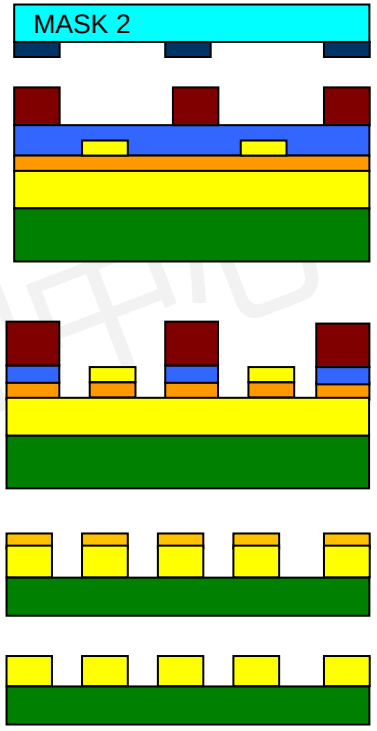




Pattern Photoresist with 1st pattern

Etch Pattern in poly (HM) Strip Resist & BARC

Coat 2nd Barc & Resist Layers



Pattern Photoresist with 2nd pattern

Open BARC Etch & Etch 2nd Oxide HM

Strip Resist & BARC Etch HM Pattern Into Poly

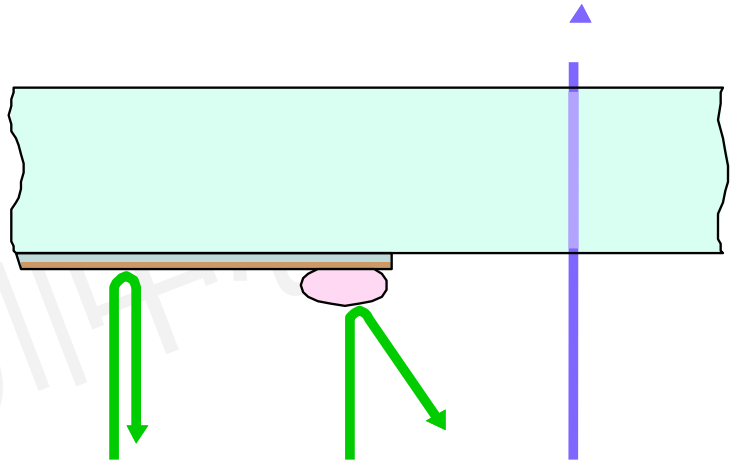
Strip HM

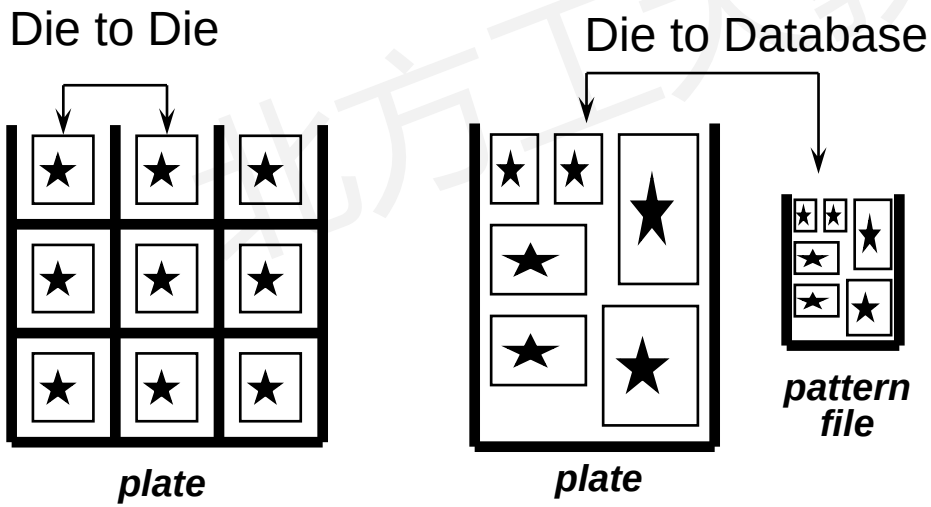
- Photoresist
- BARC (bottom anti-reflection coating)
- Oxide (HM)
- Poly
- Si Substrate

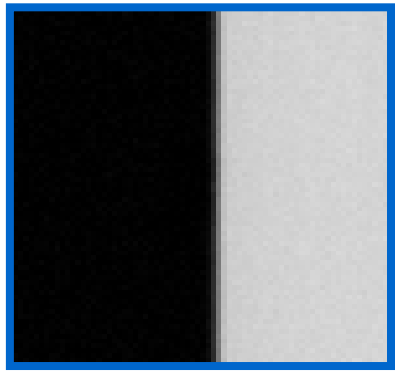
光刻掩模版检测

Mask Defect检验，分别有Die-to-Data Base (DB)、Die-to-Die (DD)及StartLight (SL)之功能

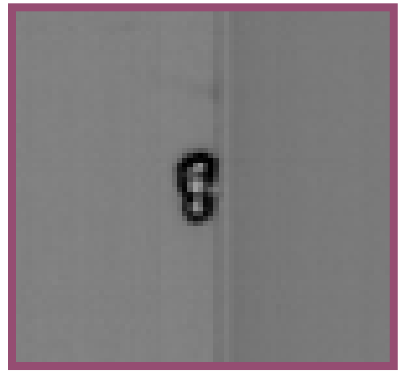
- **StarLight: 目的在检验Particle**
- **DD: 目的比较Mask重复性的Die之间是否有差别**
- **DB: 目的在比较Mask与 Data Base之间是否有差别**





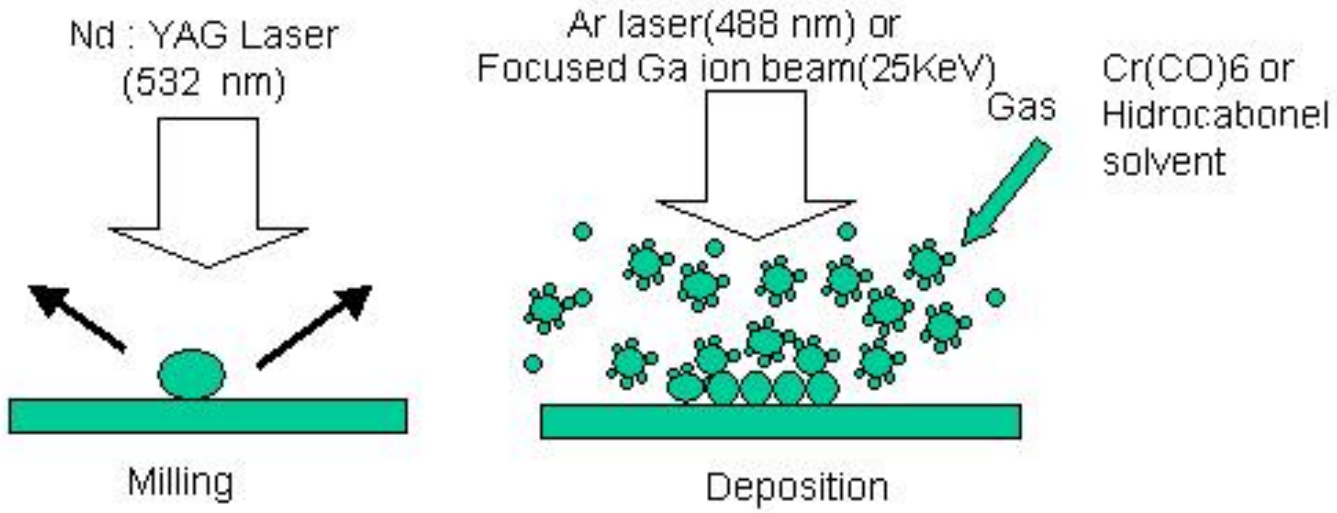


Transmitted light

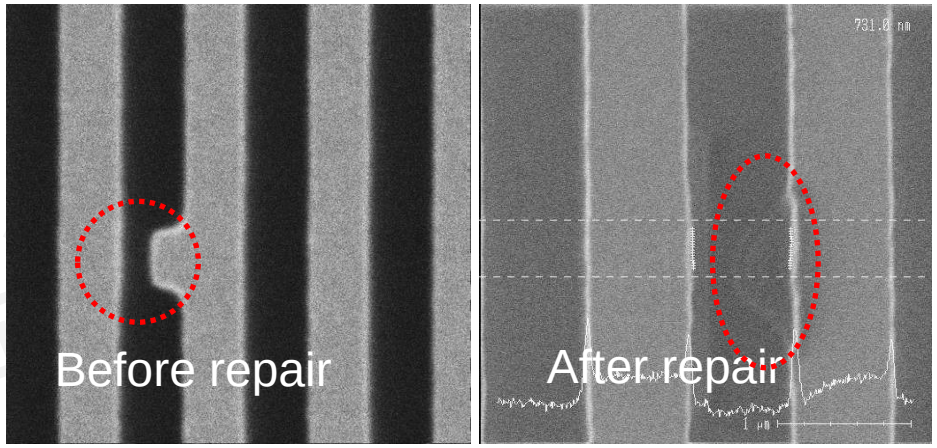


STAR*light*

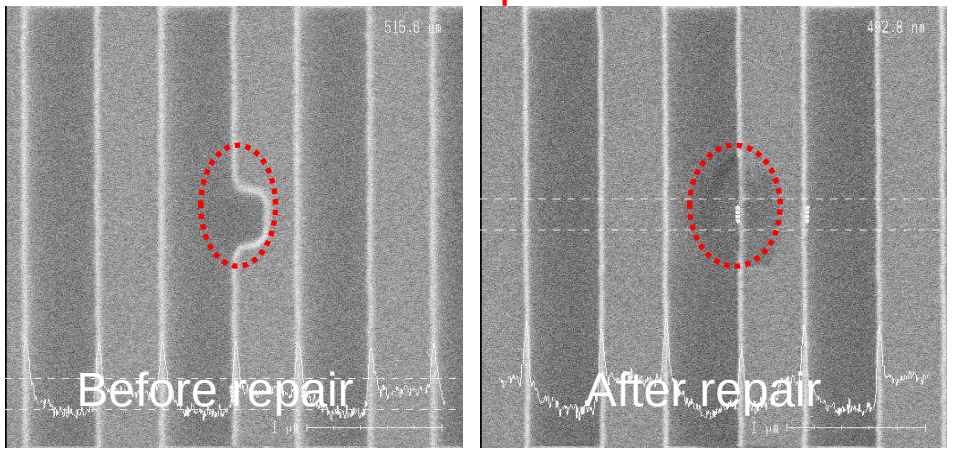
光刻掩模版修复



Opaque repair



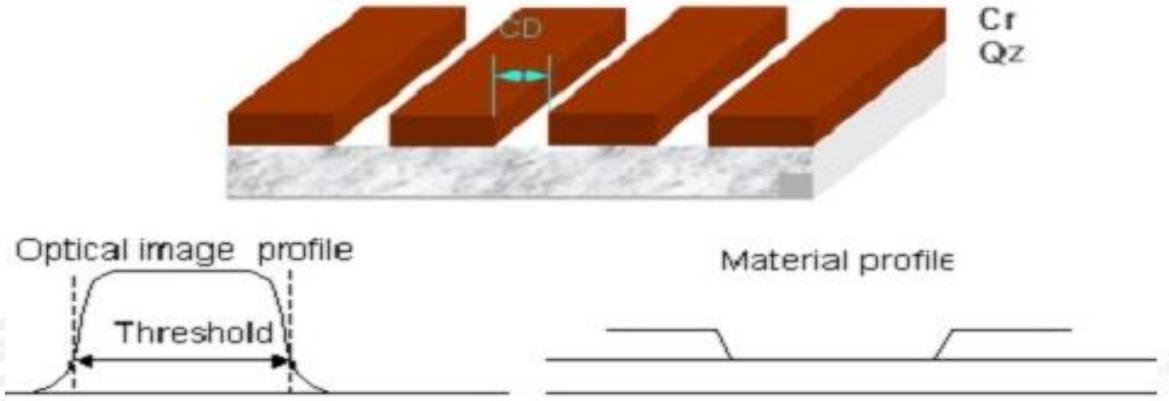
Clear repair

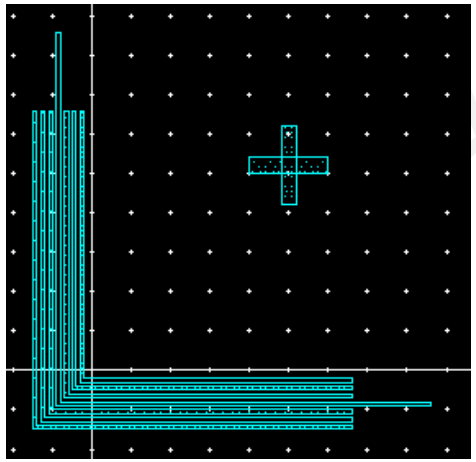


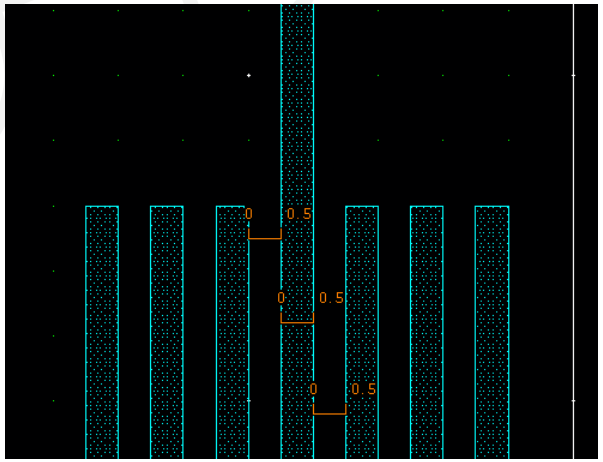
激光束掩模缺陷修补机是利用高能量的激光束打在掩模上，以高热的能量瞬间将铬挥发成汽态离开掩模基板，来达到缺陷的修补或是使用铬氧化物在高能激光下沈积在模板上

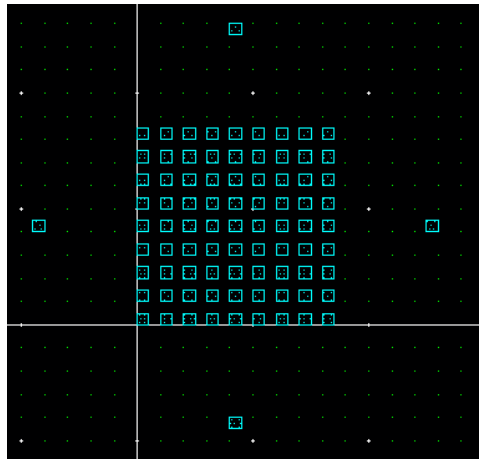
光刻掩模版关键因素 - CD

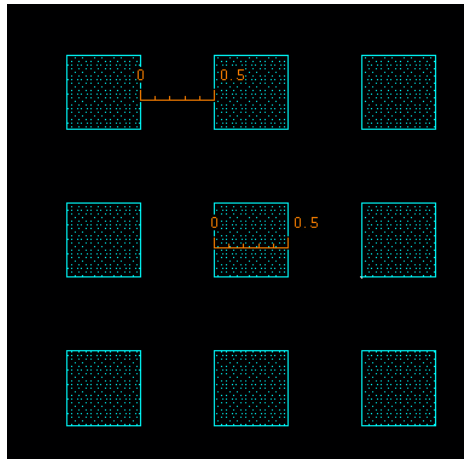
- 此工程为测定Pattern是否与客户所Design与Pattern相同的工程，主要参数为CD uniformity及MTT(mean to target)。均须在客户要求之值以内，不过超过。
- 量测方法有光学及电子束量测。光学量测的方法是藉由取得对物镜唇反射之光学影像，选定一定之基准值(Threshold)后，测定光学iamge左右侧面之距离;电子束测是利入射之电子所发生之二次电子分布，以 Threshold值之间距离测定CD
- 线宽测定可以Dark或是Clear



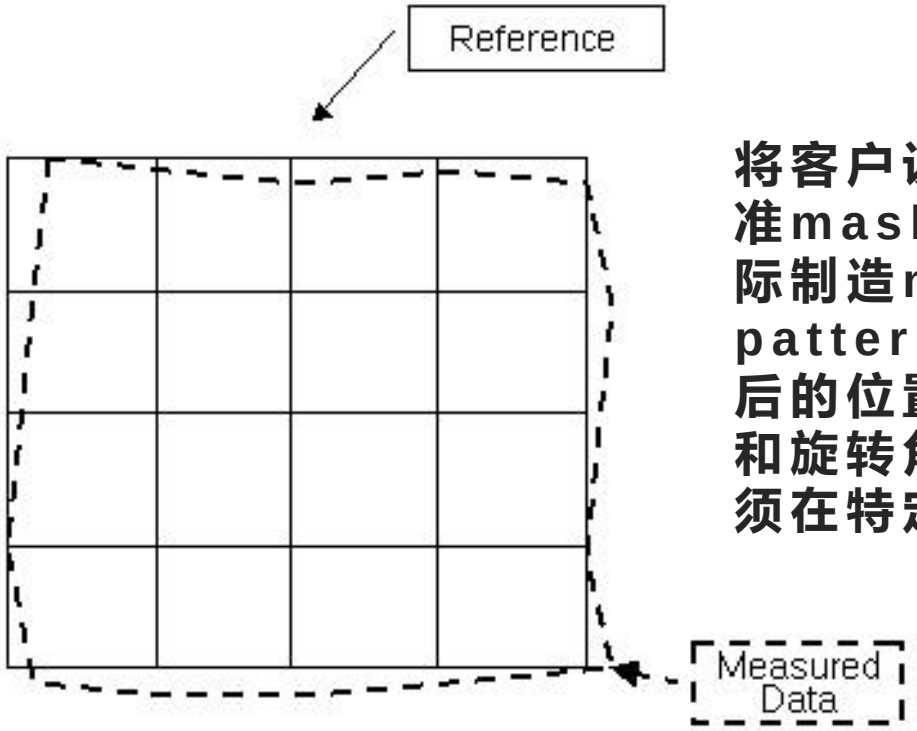




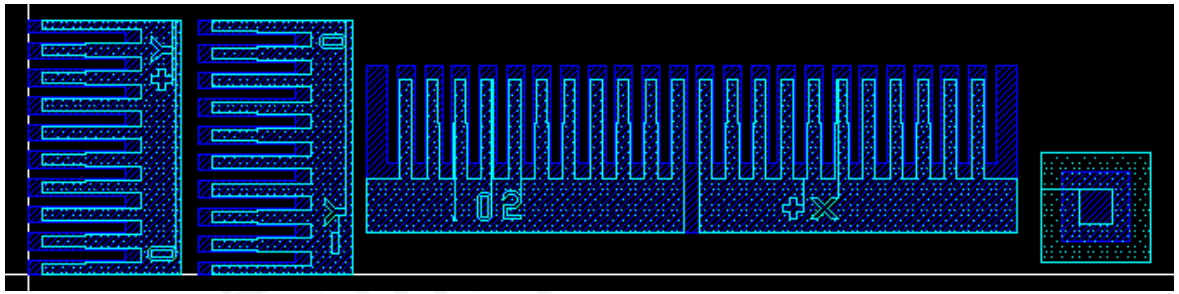


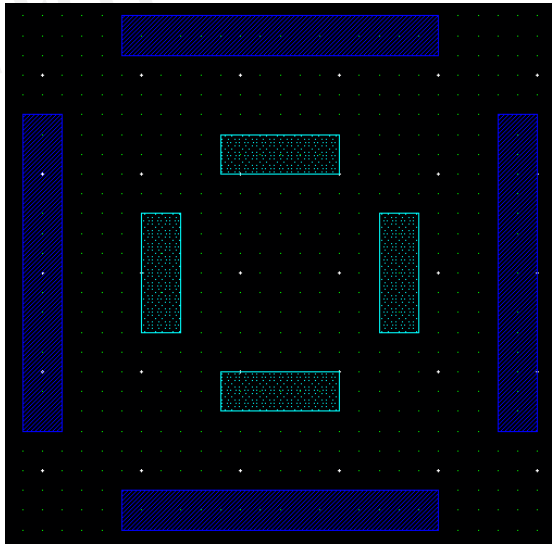


光刻掩模版关键因素 - Overlay



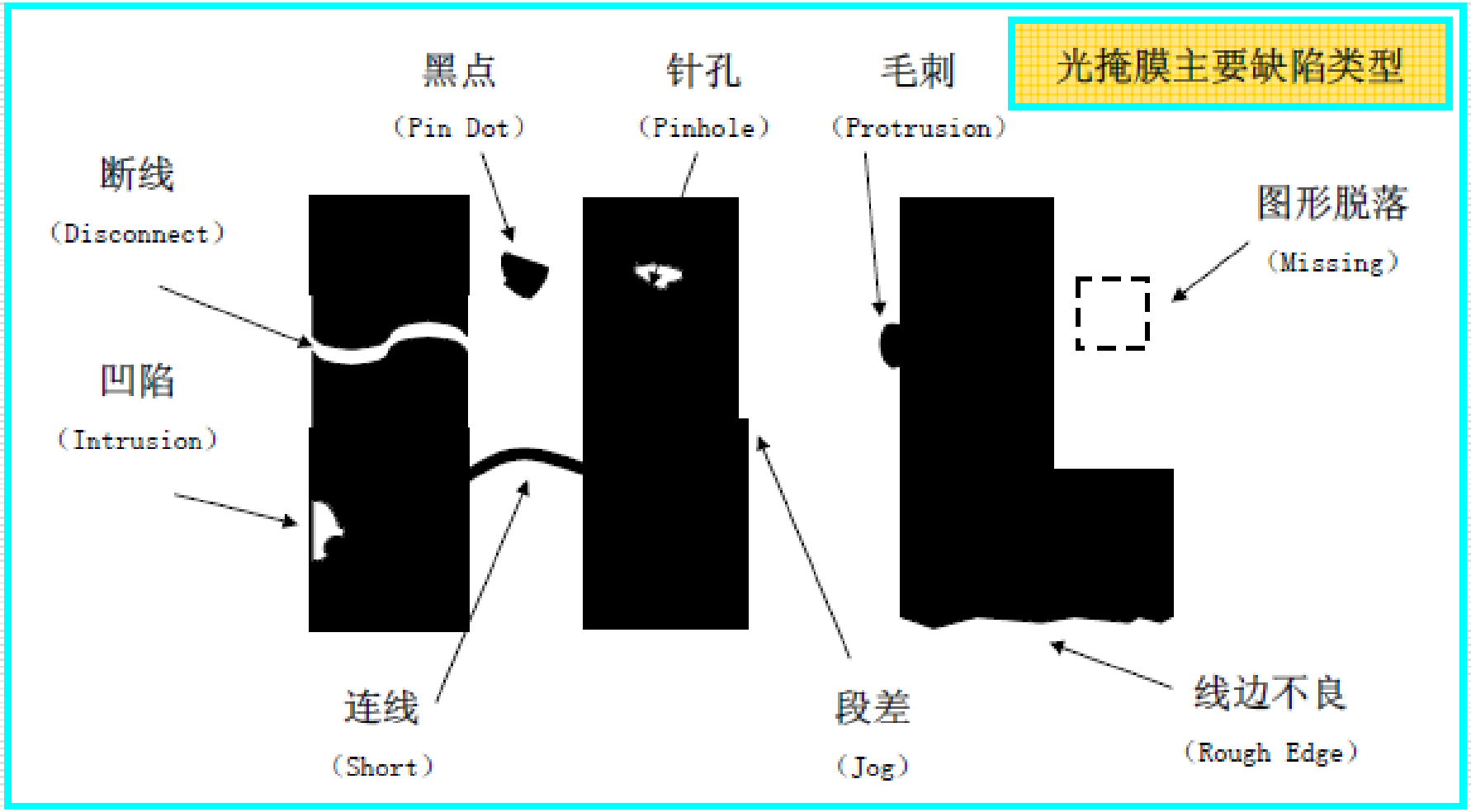
将客户设计基准mask与实际制造mask pattern比较后的位置偏差和旋转角度都须在特定值内





IC 是一种立体结构的组件，层层叠对，层与层间的上下关系非常重要，若叠对关系不良，将造成产品稳定性不良或没有良率，因此光掩模注记差的控制是必要的

光刻掩模版关键因素 - Defect



光刻版等级

光刻掩模版等级表（4:1 或 5:1）												
ITEM	Rank		S	Y	A	B	C	D	E	F	G	H	I
Design Rule	(um)		> 5	2-5	1-2	1	0.8	0.5	0.35	0.25	0.18	0.15	0.13
CD Tolerance	(±um)		±0.5	±0.3	±0.2	±0.15	±0.1	±0.075	±0.05	±0.04	±0.03	±0.025	±0.02
CD Range	(um)		≤0.5	≤0.3	≤0.2	≤0.15	≤0.1	≤0.07	≤0.05	≤0.04	≤0.035	≤0.03	≤0.025
CD mean to target	(um)		±0.5	±0.3	±0.2	±0.15	±0.1	±0.07	±0.04	±0.03	≤0.03	±0.02	±0.02
Registration & Overlay	Based on the 1st layer(um)		±0.5	±0.3	±0.2	±0.15	±0.12	±0.10	±0.07	±0.05	≤0.04	±0.03	±0.02
Defect	Defect size(um)		< 4	< 2	< 1.0	< 1.0	< 0.75	< 0.5	< 0.4	< 0.3	< 0.3	< 0.25	< 0.20
Particle	A. Pellicle Film	> 20um	None	None	None	None	None	None	None	None	None	None	None
		10-20um	≤10pcs	≤10pcs	≤10pcs	≤10pcs	≤5pcs	≤5pcs	≤5pcs	≤5pcs	≤5pcs	≤5pcs	≤5pcs
	B. Cr side	≥2.0um	None	None	None	None	None	None	None	None	None	None	None
		1.0-2.0um	---	---	≤5pcs	≤5pcs	≤5pcs	≤5pcs	≤5pcs	None	None	None	None
		0.5-1.0um	---	---	---	---	---	---	---	≤10pcs	≤10pcs	≤10pcs	≤10pcs
	C. Glass side	> 10um	None	None	None	None	None	None	None	None	None	None	None
Flatness	(um)		2um	2um	2um	2um	2um	2um	2um	1um	1um	1um	1um
Transparency	Tolerance(PSM)		---	---	---	---	---	---	---	---			
Phase Angle(degree)	Tolerance(PSM)		---	---	---	---	---	---	---	---			
Address Unit	Minimum drawing unit on Mask		---	---	---	---	---	5nm	5nm	4nm	1nm	1nm	1nm

- 模拟电路版图和PDK建模
- 数字标准单元版图和库模型建立
- 工艺掩模版优化和监控
- **Q&A**

Q1. DRC验证文件中常用基本运算有哪些？（　　）

A. AND; B. OR; C. NOT; D. INSIDE; E. OUTSIDE; F. INTERACT; G. SIZE; H. AREA; I. DENSITY

Q2. 数字标准单元库包含哪些基本单元？（　　）

A. 组合逻辑单元；　　B. 时序逻辑单元；　　C. 特殊单元

Q3.数字标准单元库中基准单元INVX1的设计要点是什么？（　　）

A. 足够大的噪声容限；　　B. 均衡的上升/下降时间；　　C. 均衡的上升/下降延时