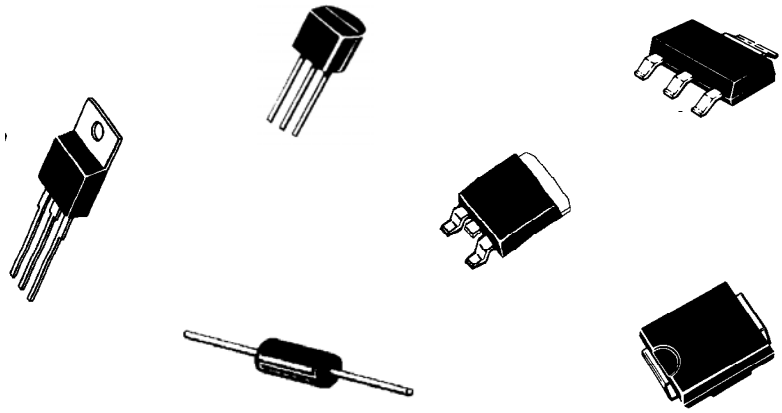
AEC - Q101 - REV - C
June 29, 2005

STRESS TEST QUALIFICATION FOR AUTOMOTIVE GRADE DISCRETE SEMICONDUCTORS



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STRESS TEST QUALIFICATION FOR DISCRETE SEMICONDUCTORS

1. SCOPE

1.1 Description

This document defines minimum stress test driven qualification requirements and references test conditions for qualification of discrete semiconductors (e.g. transistors, diodes, etc.). This document does not relieve the supplier of their responsibility to meet their own company's internal qualification program. Additionally, this document does not relieve the supplier from meeting any user requirements outside the scope of this document. In this document, "user" is defined as any company developing or using a discrete semiconductor part in production. The user is responsible to confirm and validate all qualification and assessment data that substantiates conformance to this document.

1.1.1 Purpose

The purpose of this specification is to determine that a device is capable of passing the specified stress tests and thus can be expected to give a certain level of quality / reliability in the application.

1.1.2 Definition of Stress-Test Qualification

AEC-Q101 Stress Test “Qualification” is defined as successful completion of the test requirements outlined in this document. The minimum temperature range for discrete semiconductors per this specification shall be -40°C to +125°C ambient, except the minimum range for all LEDs shall be –40°C to +85°C ambient. (Note: Some components may be derated to zero at the maximum temperature.)

1.1.3 Approval for Use in an Application

"Approval" is defined as user approval for use of a part in the application. The user’s method of approval is beyond the scope of this document.

1.2 Reference Documents

Current revision of the referenced documents will be in effect at the date of agreement to the qualification plan. Subsequent qualification plans will automatically use updated revisions of these referenced documents.

1.2.1 Military

1. MIL-STD-750 Test Methods for Semiconductor Devices

1.2.2 Industrial

1. UL-STD-94 Test for Flammability of Plastic Materials of Parts in Devices and Appliances.
2. JEDEC JESD-22 Reliability Test Methods for Packaged Devices
3. J-STD-002 Solderability Tests for Component Leads, Terminations, Lugs, Terminals and Wires.
4. J-STD-020 Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices
5. JESD22-A113 Preconditioning of Nonhermetic Surface Mount Devices Prior to Reliability Testing

1.2.3 AEC

1. AEC - Q001 Guidelines for Part Average Testing
2. AEC - Q101 - 001 ESD (Human Body Model)
3. AEC - Q101 - 002 ESD (Machine Model)
4. AEC - Q101 - 003 Discrete Component Wirebond Shear Test
5. AEC - Q101 - 004 Miscellaneous Test Methods
   Unclamped Inductive Switching
   Dielectric Integrity
   Destructive Physical Analysis
6. AEC – Q101 – 005 ESD (Charged Device Model)

1.2.4 Other

1. QS-9000
2. ISO-TS-16949

2. GENERAL REQUIREMENTS

2.1 Objective

Successful completion and documentation of the test results and the use of generic data from requirements outlined in this document allows the supplier to claim that the part is “AEC Q101 qualified”. The supplier, in agreement with the user, can perform qualification at sample sizes and conditions less stringent than what this document requires. However, that part cannot be considered “AEC Q101 qualified” until such time that the unfulfilled requirements have been successfully completed.

NOTE: This document does not include qualification requirements for Pb-free components. The next revision will include these requirements.

2.2 Precedence of Requirements

In the event of conflict in the requirements of this specification and those of any other documents, the following order of precedence applies:

1. The purchase order
2. The individual device specification
3. This document
4. The reference documents in Section 1.2 of this document
5. The supplier's data sheet

For the device to be considered a qualified part per this specification, the purchase order and/or individual device specification cannot waive or detract from the requirements of this document.

2.3 The Use of Generic Data to Satisfy Qualification and Requalification Requirements

The use of generic (family) data to simplify the qualification/requalification process is encouraged. To be considered, the generic data must be based on the following criteria:

1. Component qualification requirements listed in Table 2
2. A matrix of specific requirements associated with each characteristic of the device and manufacturing process as shown in Table 3.
3. Definition of family guidelines established in Appendix 1.
4. Represent a random sample of the normal population.

Table 2 defines a set of qualification tests that must be considered for both new device qualifications and requalification associated with a design or process change.

Table 3 defines a matrix of appropriate qualification tests that must be considered for any changes proposed for the component. Table 3 is the same for both new processes and requalification associated with a process change. This table is a superset of tests that the supplier and user should use as a baseline for discussion of tests that are required for the qualification/requalification in question. **It is the supplier's responsibility to present and document rationale for why any of the highlighted tests need not be performed.**

Appendix 1 defines the criteria by which components are grouped into a qualification family for the purpose of considering the data from all family members to be equal and generically acceptable to the qualification of the device in question. With proper attention to these qualification family guidelines, information applicable to other devices in the family can be accumulated. This information can be used to demonstrate generic reliability of a device family and minimize the need for device-specific qualification test programs. This can be achieved through qualification of a range of devices representing the “four corners” of the qualification family (e.g. highest/lowest voltage, largest/smallest die, etc). Sources of generic data should come from supplier-certified test labs, and can include internal supplier's qualifications, user-specific qualifications and supplier's in-process monitors. The generic data to be submitted must meet or exceed the test conditions specified in Table 2. Table 1 provides guidelines showing how the available part test data may be applied to reducing the number of lots required for qualification. Electrical characterization to the individual user device specification must be performed for each device submission, generic characterization data is not allowed. **The user(s) will be the final authority on the acceptance of generic data in lieu of specific device test data.**

Table 1: Part Qualification/Requalification Lot Requirements

Part Information	Lot Requirements for Qualification
New device, no applicable generic data.	Lot and sample size requirements per Table 2.
A part in a family is qualified. The part to be qualified is less complex and meets the Family Qualification Definition per Appendix 1.	Only device specific tests as defined in section 4.2 are required. Lot and sample size requirements per Table 2 for the required tests.
A new part that has some applicable generic data.	Review Appendix 1 to determine required tests from Table 2. Lot and sample sizes per Table 2 for the required tests.
Part process change.	Review Table 3 to determine which tests from Table 2 are required. Lot and sample sizes per Table 2 for the required tests.
Qualification/Requalification involving multiple sites.	Refer to Appendix 1, section 3.
Qualification/Requalification involving multiple families.	Refer to Appendix 1, section 3.

2.4 Test Samples

2.4.1 Lot Requirements

Lot requirements are designated in Table 2, herein.

2.4.2 Production Requirements

All qualification parts shall be produced on tooling and processes at the manufacturing site that will be used to support part deliveries at projected production volumes.

2.4.3 Reusability of Test Samples

Devices that have been used for nondestructive qualification tests may be used to populate other qualification tests. Devices that have been used for destructive qualification tests may not be used any further except for engineering analysis.

2.4.4 Sample Size Requirements

Sample sizes used for qualification testing and/or generic data submission must be consistent with the specified minimum sample sizes and acceptance criteria in Table 2. If the supplier elects to submit generic data for qualification/requalification, the specific test conditions and results must be reported. Existing applicable generic data should first be used to satisfy these requirements and those of section 2.3 for each test requirement in Table 2. Part specific qualification testing should be performed if the generic data does not satisfy these requirements**.**

2.4.5 Pre- and Post-stress Test Requirements

All pre and post stress test parts must be tested to the electrical characteristics defined in the individual user device detail specification at room temperature.

2.5 Definition of Test Failure After Stressing

Test failures are defined as devices exhibiting any of the following criteria:

1. Devices not meeting the electrical test limits defined in the first user's device specification or appropriate supplier generic device specification. Minimum test parametric requirements shall be as specified in Appendix 5.

2. Devices not remaining within ± 20% of the initial reading of each test (with the exception of leakage limits which are not to exceed 10 times the initial value for moisture tests and 5 times the initial value for all others) after completion of environmental testing. Devices exceeding these guidelines must be justified by the supplier and approved by the user. For leakages below 100 nA, tester accuracy may prevent a post stress analysis to initial reading.

3. Any device exhibiting external physical damage attributable to the environmental test.

If the cause of failure is agreed (by the manufacturer and the user) to be due to mishandling or ESD, the failure shall be discounted, but reported as part of the data submission.

2.6 Criteria for Passing Qualification / Requalification

Passing all appropriate qualification tests specified in Table 1, either by performing the tests (acceptance of zero failures using the specified minimum sample size) on the specific part or demonstrating acceptable family generic data (using the family definition guidelines defined in Appendix 1 and the total required lot and sample sizes), qualifies the device per this document.

Devices that have failed the acceptance criteria of tests required by this document require the supplier to satisfactorily determine root cause and corrective action to assure the user that the failure mechanism is understood and contained. The device shall not be considered as passing stress-test qualification until the root cause of the failure is determined and the corrective and preventive actions are confirmed to be effective. New samples or data may be requested to verify the corrective action. If generic data contains any failures, the data is not usable as generic data unless the supplier has documented corrective action or containment for the failure condition.

Any unique reliability tests or conditions requested by the user and not specified in this document shall be agreed upon between the supplier and user requesting the test, and will not preclude a device from passing stress-test qualification as defined by this document.

2.7 Alternative Testing Requirements

Any deviation from the test requirements and conditions listed in Table 2 are beyond the scope of this document. Deviations (e.g. accelerated test methods) must be demonstrated to the AEC for consideration and inclusion into future revisions of this document.

3. QUALIFICATION AND REQUALIFICATION

3.1 Qualification of a New Device

Stress test requirements and corresponding test conditions for a new device qualification are listed in Table 2. For each qualification, the supplier must present data for ALL of these tests, whether it is stress test results on the specific device or acceptable generic family data. A review is to be made of other parts in the same generic family to ensure that there are no common failure mechanisms in that family. Justification for the use of generic data, whenever it is used, must be demonstrated by the supplier and approved by the user. For each part qualification, the supplier must present Certificate of Design, Construction and Qualification to the requesting user. See Appendix 2.

3.2 Requalification of a Changed Device

The supplier will meet the user requirements for product/process changes.

3.2.1 Changes Requiring User Notification and/or Requalification

Process changes include, but are not limited to:

1. Location of a plant or production line in which fabrication, assembly or testing is to take place.

2. Die size, metallization, cross-section, geometry or construction technique (e.g. wafer stepping or re-design, but not including master mask restepping when no changes are made).

3. Device assembly process sequence, ~~or~~ final test~~ing process~~ program sequence or assembly/test equipment type.

4. Materials and finishes used to manufacture the device internally or externally (e.g. dopant type, lead frame material or plating, molding compound, etc.).

5. Internal connection methods, including die or lead attach.

6. Package sealing or encapsulation techniques in the specified packaging process; coating or passivation techniques.

7. Quality Assurance procedures that may affect the quality/reliability of the part.

As a minimum, any change to the product, as defined above, requires performing the applicable tests listed in Table 2, using Table 3 to determine the requalification test plan. Table 3 will be used as a guide for determining which tests need to be performed or whether equivalent generic data can be submitted for that test. A Qualification Plan agreement between the supplier and the user(s) with justification for performing or not performing any recommended test shall occur before the implementation of any requalification test plan.

3.2.2 Process Change Notification

The supplier shall submit a projection to the users of all forecasted process changes. The projection of any change~~s~~ shall be submitted a minimum of six months in advance. Information required for submission to the user, for each change, shall include the following as a minimum:

1. Benefit to the user (value, time and quality).
2. For each user part number involved in the change, the following information is required:
   a) Supplier and user part numbers
   b) An estimated date of the last production lot of unchanged parts.
   c) An estimated final order date and final ship date of unchanged parts.
   d) A projected shipment date and date code of changed parts.
3. A detailed description of the change in terms of the materials, processes, equipment, cosmetic or dimensional differences, characteristics, rating, circuit design, die size and wafer size, as applicable.
4. Technical data and rationale to support the proposed changes.
5. An electrical performance characterization comparison (between the new and original product) of all significant electrical parameters over temperature extremes that could be affected by the change. Changes in median and dispersion performance shall be noted even though conformance to specification limits is still guaranteed. (Include F-Test, T-Test, or ANOVA comparisons, as needed.)
6. The supplier shall submit an updated Certificate of Design, Construction and Qualification along with information required by this section (Section 3.2.2).
7. The results of completed supplier requalification tests of the changed device(s).

Items 1, 2, 3 & 4 are background information needed up front to evaluate the impact of the change on supply and reliability and to come to agreement on a qualification plan acceptable to the supplier and user. Items 5, 6 and 7 must be submitted prior to any final approval to implement any change on the user's product.

No changes shall be implemented without prior approval of the user.

3.2.3 Criteria for Passing Requalification

It is the responsibility of each user to review the data, change notices, and supporting documentation to either qualify or not qualify the change based on the results of the tests performed. Additionally, the criteria for passing qualification (Section 2.6) apply.

3.2.4 End User Approval

A change may not affect a part's qualification status, but may affect its performance in an application. Individual user authorization of a process change will be required for that user's particular application(s), and this method of authorization is outside the scope of this document.

3.3 Qualification Test Plan

The supplier is requested to initiate a discussion with each user (as needed) resulting in completion of a signed Qualification Test Plan agreement as soon as possible after supplier selection for new parts, and at the time of notification (reference 3.2.2) prior to process changes. The Qualification Test Plan, as defined in Appendix 3, shall be used to provide a consistent method of documentation supporting what testing will be performed as required by Tables 2 & 3.

4 QUALIFICATION TESTS

4.1 General Tests

Test details are given in Table 2. Not all tests apply to all devices. For example, certain tests apply only to hermetically packaged devices, others apply only to power MOSFET devices, and so on. The applicable tests for the particular device type are indicated in the "Note" column and the "Additional Requirements" column of Table 2. The "Additional Requirements" column of Table 2 also serves to highlight test requirements that supersede those described in the referenced test.

4.2 Device Specific Tests

The following tests must be performed on the specific device, i.e., family data is not allowed for these tests:

1. Electrostatic Discharge Characterization (Table 2, Test #11)

2. Parametric Verification (Table 2, Test #4) - The supplier must demonstrate that the part is capable of meeting parametric limits detailed in the individual user device specification.

4.3 Data Submittal Type

Data to be submitted to the user are classified in three types (Data Type column in Table 2):

Data Type 1 Data (generic or specific) from these tests should be formatted as defined in Section 4.4 and included in each qualification submission.

Data Type 2 Package specific data that should not be included with each qualification submission (except where the package is new). In place of this data the supplier can submit a "Document of Completion" that references successful completion of the specific test previously performed, provided no significant changes have been made. For Test #14 (Physical Dimensions) the Document of Completion should be completed referencing the appropriate user packaging specification.

For test 11 – Charged Device Model, small packages may not be able to hold enough charge to meet the specified discharge voltage. For these packages, perform the test once and, if there is insufficient charge, the supplier must instead perform HBM and MM. The supplier must document that the package could not hold sufficient charge to perform the test.

Data Type 3 Re-qualification data should be included in the qualification submission as required by Table 3. These tests shall be considered by the supplier during re-qualification plan development as useful tools to provide supporting rationale for new part qualification (including new packages) and/or process changes. It is the supplier's responsibility to present rationale for why any of these tests need not be performed.

4.4 Data Submission Format

A data summary shall be submitted as defined in Appendix 4. Raw data and histograms shall be submitted to the individual user upon request. **All data and documents (e.g. justification for non-performed tests, etc.) shall be maintained by the supplier in accordance with QS-9000 and/or TS-16949 requirements.**

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TABLE 2 - QUALIFICATION TEST DEFINITIONS									
#	Stress	Abrv	Data type	Note	Sample Size per lot	# of lots	Accept on # failed	Reference (current revision)	Additional Requirements
1	Pre- and Post-Stress Electrical Test	TEST	1	NG	All qualification parts tested per the requirements of the appropriate device specification.		0	User specification or supplier's standard specification	Test is performed as specified in the applicable stress reference at room temperature.
2	Pre-conditioning	PC	1	GS	SMD qualification parts for TC, AC,H^3TRB & IOL/PTC		0	JESD22 A-113	Performed on surface mount devices (SMDs) prior to TC, AC, H^3TRB & IOL/PTC stresses only. Use A113 Sensitivity Level 1. TEST before and after PC. Any replacement of parts must be reported.
3	External Visual	EV	1	NG	All qualification parts submitted for testing		0	JESD22 B-101	Inspect device construction, marking and workmanship.
4	Parametric Verification	PV	1	N	25	3 Note A	0	Individual AEC user specification	Test all parameters according to user specification over the device temperature range to insure specification compliance.
5	High Temperature Reverse Bias	HTRB	1	DGUVP	77	1 Note B	0	JESD22 A-108	1000 hours at junction temperature T_J = 150^{O}C, or specified T_J(max) rating, with device reverse biased to 80% of maximum breakdown voltage specification. The ambient temperature T_A is to be adjusted to compensate for current leakage. Can reduce duration to 500 hours through increasing T_J by 25^{O}C, adjusting T_A to compensate for current leakage. TEST before and after HTRB as a minimum.
6	High Temperature Gate Bias	HTGB	1	DGMUP	77	1 Note B	0	JESD22 A-108	1000 hours at junction temperature T_J = 150^{O}C, or specified T_J(max) rating, with gate biased at 100% of maximum gate voltage rating indicated in the detail specification with device biased OFF. The ambient temperature T_A is to be adjusted to compensate for current leakage. Can reduce duration to 500 hours through increasing T_J by 25^{O}C, adjusting T_A to compensate for current leakage. TEST before and after HTGB as a minimum.

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TABLE 2 - QUALIFICATION TEST DEFINITIONS									
#	Stress	Abrv	Data type	Note	Sample Size per lot	# of lots	Accept on # failed	Reference (current revision)	Additional Requirements
7	Temperature Cycling	TC	1	DGU	77	1 Note B	0	JESD22 A-104	1000 cycles (T_A = minimum range of -55°C to maximum rated junction temperature, not to exceed 150ºC). Can reduce duration to 400 cycles using T_A (max) = 25°C over device maximum rated junction temperature. TEST before and after TC as a minimum.
8	Autoclave	AC	1	CDG U	77	1 Note B	0	JESD22 A-102	96 hours, T_A = 121°C, RH = 100%, 15psig, TEST before and after AC.
9	High Humidity High Temp. Reverse Bias	H^3TRB	1	DGU V	77	1 Note B	0	JESD22 A-101	1000 hours at T_A = 85°C/85% RH with device reverse biased at 80% of rated breakdown voltage up to a maximum of 100V or limit of chamber. TEST before and after H3TRB as a minimum.
9 alt	Highly Accelerated Stress Test	HAST	1	CDG UV	77	1 Note B	0	JESD22 A-110	96 hours at T_A=130°C/85%RH with device reverse bias at 80% of rated voltage up to a voltage above which arcing in the chamber will likely occur (typically 42V). TEST before and after 96 hours HAST.
10	Intermittent Operational Life	IOL	1	DGTU WP	77	1 Note B	0	MIL-STD-750 Method 1037	Tested per duration indicated in Timing Requirements table on Page 13. T_A=25°C. Devices powered to insure $\Delta T_J \geq 100°C$ (not to exceed absolute maximum ratings). TEST before and after IOL as a minimum.
10 alt	Power and Temperature Cycle	PTC	1	DGTU W	77	1 Note B	0	JESD22 A-105	Perform PTC if $\Delta T_J \geq 100°C$ cannot be achieved with IOL. Tested per duration indicated for Timing Requirements in Table 2A. Devices powered and chamber cycled to insure $\Delta T_J \geq 100°C$ (not to exceed absolute maximum ratings). TEST before and after PTC as a minimum.

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TABLE 2 - QUALIFICATION TEST DEFINITIONS									
#	Stress	Abrv	Data type	Note	Sample Size per lot	# of lots	Accept on # failed	Reference (current revision)	Additional Requirements
11	ESD Characterization	ESD	1 (HBM, MM) 2 (CDM)	D	30 ea CDM/ HBM/MM	1	0	AEC Q101-001, 002 and 005	Supplier must perform at least two of the referenced ESD models through the end of 2005. CDM will be required as one of the two selected models as of 2006. For CDM, small packages may not be able to hold enough charge to meet the specified discharge voltage. For these packages, perform the test once and, if there is insufficient charge, the supplier must instead perform HBM and MM. The supplier must document that the package could not hold sufficient charge to perform the test. See attached procedure for details on how to perform the test. TEST before and after ESD.
12	D.P.A.	DPA	1	DG	2	1 Note B	0	AEC-Q101-004 Section 4	Random sample of devices that have successfully completed H^3TRB or HAST, and TC.
13	Physical Dimension	PD	2	NG	30	1	0	JESD22 B-100	Verify physical dimensions to the applicable user device packaging specification for dimensions and tolerances.
14	Terminal Strength	TS	2	DGL	30	1	0	MIL-STD-750 Method 2036	Evaluate lead integrity of leaded devices only.
15	Resistance to Solvents	RTS	2	DG	30	1	0	JESD22 B-107	Verify marking permanency. (Not required for laser etched parts or parts with no marking.)
16	Constant Acceleration	CA	2	DGH (1)	30	1 Note B	0	MIL-STD-750 Method 2006	Y1 plane only, 15K g-force. TEST before and after CA.
17	Vibration Variable Frequency	VVF	2	DGH (2)	Items 16 through 19 are sequential tests for hermetic packages. (See note H on Legend page.)			JESD22 B-103	Use a constant displacement of 0.06 inches (double amplitude) over the range of 20Hz to 100 Hz and a 50g constant peak acceleration over the range of 100 Hz to 2 KHz. TEST before and after VVF.
18	Mechanical Shock	MS	2	DGH (3)			0	JESD22 B-104	1500 g's for 0.5mS, 5 blows, 3 orientations. TEST before and after MS.
19	Hermeticity	HER	2	DGH (4)			0	JESD22 A-109	Fine and Gross leak test per individual user specification.

TABLE 2 - QUALIFICATION TEST DEFINITIONS									
#	Stress	Abrv	Data type	Note	Sample Size per lot	# of lots	Accept on # failed	Reference (current revision)	Additional Requirements
20	Resistance to Solder Heat	RSH	2	DG	30	1	0	JESD22 B-106	TEST before and after RSH. SMD devices shall be fully submerged during test unless justified by the supplier and agreed to by the user (e.g., submerge SOT223, not D2PAK).
21	Solderability	SD	2	DG	10	1 Note B	0	J-STD-002	Magnification 50x, Reference solder conditions in Table 2B. Test method A for through-hole, both B test methods and test method D for SMD.
22	Thermal Resistance	TR	3	DG	10 ea, pre & post change	1	0	JESD24-3, 24-4, 24-6 as appropriate	Measure TR to assure specification compliance and provide process change comparison data.
23	Wire Bond Strength	WBS	3	DGE	10 bonds from min of 5 devices	1	0	MIL-STD-750 Method 2037	Pre & Post process change comparison to evaluate process change robustness.
24	Bond Shear	BS	3	DGE	10 bonds from min of 5 devices	1	0	AEC-Q101-003	See attached procedure for details on acceptance criteria and how to perform the test.
25	Die Shear	DS	3	DG	5	1	0	MIL-STD-750 Method 2017	Pre & Post process change comparison to evaluate process change robustness.
26	Unclamped Inductive Switching	UIS	3	D	5	1	0	AEC-Q101-004 Section 2	Pre & Post process change comparison to evaluate process change robustness (Power MOS and internally clamped IGBTs only).
27	Dielectric Integrity	DI	3	DM	5	1	0	AEC-Q101-004 Section 3	Pre & Post process change comparison to evaluate process change robustness. All parts must exceed gate breakdown voltage minimum (Power MOS & IGBT only).

All electrical testing before and after the qualification stresses (including pre-conditioning) are performed to the limits detailed in the individual user specification at room temperature only. For generic qualifications, the supplier's standard specification limits at room temperature may be used.

LEGEND FOR TABLE 2

Notes:
- A For parametric verification data, sometimes circumstances may necessitate the acceptance of only one lot by the user. Should a subsequent user decide to use a previous user's qualification approval, it will be the subsequent user's responsibility to verify an acceptable number of lots were used.
- B Where generic (family) data is provided in lieu of component specific data, 3 lots are required.
- C Not applicable for LED's, phototransistors, and other optical devices.
- D Destructive test, devices are not to be reused for qualification or production.
- E Ensure that each size wire is represented in the sample size.
- G Generic data allowed. See Section 2.3.
- H Required for hermetic packaged devices only. Items 16 through 19 are performed as a sequential test to evaluate mechanical integrity of packages containing internal cavities. Number in parentheses below notes indicates sequence.
- L Required for leaded devices only.
- M Required for MOS & IGBT devices only.
- N Nondestructive test, devices can be used to populate other tests or they can be used for production.
- P Consideration should be made for whether this test is to be applied to a Smart Power device or substituted for a Q100 test. Elements for consideration include the amount of logic or sensing on the die, the intended user application, switching speed, power dissipation and pin count.
- S Required for surface mount devices only.
- T When testing diodes under Intermittent Op Life conditions the 100 degree junction temperature delta may not be achievable. Should this condition exist, a Power Temperature Cycling (Item 10alt) test shall be used in place of Intermittent Op Life (Item 10) to ensure the proper junction temperature changes occur. All other devices should use IOL.
- U For these tests only, it is acceptable to use unformed leaded packages (e.g., IPAK) to qualify new die going in the equivalent package (e.g., DPAK) provided the die size is within the range of sizes qualified for the equivalent package.
- V For bi-directional Transient Voltage Suppressor (TVS) devices, one-half the test duration in each direction shall be performed.
- W Not required for TVS devices. PV data in 4.2 will be after 100% Peak Pulse Power (Pppm) has been performed to rated Ippm current.

Table 2A

Intermittent Operational Life (Test 10) or Power Temp Cycling (Item 10alt) Timing Requirements			
Package Type	Number of Cycles Required $\Delta T_J \geq 100^oC$	Number of Cycles Required $\Delta T_J \geq 125^oC$	Time per cycle
Small (e.g. SMD SOTS thru D-pak, and all LEDs)	15,000	7,500	2 minutes on / 2 minutes off
Medium (e.g. TO-220, D^2-pak)	8,572	4,286	3.5 minutes on / 3.5 minutes off
Large (e.g. TO-3, TO-247)	6,000	3,000	5 minutes on / 5 minutes off
Leadless Not to exceed:	60,000/(x+y) 15,000 cycles	30,000/(x+y) 7,500 cycles	Fastest capable (minimum 2 min. on/off) x min. on + y min. off

Example 1: A package capable of 2 minutes on/4 minutes off would require 10,000 cycles [60,000/(2+4)] at $\Delta T_J \geq 100^oC$ or 5,000 cycles at $\Delta T_J \geq 125^oC$.

Example 2: A package capable of 1 minute on/1 minute off would require 15,000 cycles at $\Delta T_J \geq 100^oC$ or 7,500 cycles at $\Delta T_J \geq 125^oC$.

Table 2B

Solder Conditions Table (Test #21) Requirements				
Type	Test Method	Solder Temperature	Steam Age Category	Exception for Dry Heat
Leaded Through-Hole	A	235°C	3	----------
SMD Standard Process	B	235°C	3	----------
SMD Low Temperature Solder	B	215°C	--	4hrs @ 155ºC (in lieu of steam age)
SMD Dissolution of Metals test	D	260°C	3	----------

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Table 3 - Process Change Guidelines for the Selection of Tests

Note: A letter or "●" indicates that performance of that stress test should be **considered** for the appropriate process change

Table 2 Test #	3	4	5	6	7	8	9	9 alt	10/ alt	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	
Test Name / **Change**	**External Visual**	**Parametric Verification**	**High Temp. Rev. Bias**	**High Temp. Gate Bias**	**Temperature Cycle**	**Autoclave**	**H3TRB**	**High. Accel. Stress Test**	**Intermittent Oper. Life**	**ESD Characterization**	**Destruct. Phy. Analysis**	**Physical Dimensions**	**Terminal Strength**	**Resistance to Solvents**	**Constant Acceleration**	**Vibration**	**Mechanical Shock**	**Hermeticity**	**Resist. to Solder Heat**	**Solderability**	**Thermal Resistance**	**Wire Bond Strength**	**Wire Bond Shear**	**Die Shear**	**Unclamp.Induct.Switch**	**Dielectric Integrity**	**Notes**
DESIGN																											
Wafer Thickness		●	●		●				●		●								x		●	●	●				F
Wafer Diameter		●	●	●																							
Die Size		●	●		●				●	E	●								●		●			●	M		F
Layout		●	●	●	3				●	E	3														M		
Field Termination		●	●		●	●	●	●		E	●														M		
WAFER FAB																											
Wafer Source		●	●				●	●	●												●				9,M		R
Lithography		●	4	4			6,7	6,7														1					P
Diffusion		●	5,6	5		6	6	6		●	6														M		PR
Doping Profile/**Schottky Barrier**		●	5,**0**							●															M		R
Ion Implantation		●	5,6	●		6	6	6		●	6														M		PR
Polysilicon		●	●	●	●					E	●														M	●	P
Metallization (Top side)		●	8		●	●	●	●	●	E	●								●			●	●				
Metallization (Back side)		●			●		●	●	●										●		●			●			
Passivation/Glassivation		●	●	●	●	●	●	●	●	●	●											●					
Oxide		●		●	7	6	6	6	●	E	6,7															●	
Epitaxic Growth		●	●																						M		R
Etch		●	6	4		6,7	6,7	6,7			6,7											1,7			8,M	4	
Backside Operation		●			●	●	●	●	●										●		●			●			A
Fab Site Transfer		●	●	●	●	●	●	●	●	E	●										●	●	●	●	M	●	AIPRS
ASSEMBLY																											
Die Overcoat			●	●	●	●	●	●	●		●							H				●					
Leadframe Plating/**Lead Finish**	**D**				**C**	**C**	**C**	**C**				**D**		**D**				H		**D**	**C**	2**C**		**C**			
Leadframe Mat'l/Source	●				●	●	●	●	●			●	●					H	●	●	●	2		●			AFX
Package/LF Dimension					●		●	●	●			●						H			●			●			
Wire Bonding		●			●		●	●	●		●								●			●	●				
Die Scribe/Separation/Saw		●			●				●																		
Die Preparation/Clean		●			●	●	●	●														●		●			X
Die Attach		●			●	●	●	●	●									H	●		●			●			AX
Encapsulation Material	●	●	●	●	●	●	●	●	●		●	●		B				H	●	●	●					●	AFG
Encapsulation Process	●		●	●	●	●	●	●	●		●	●		B				H	●	●							AG
Hermetic Sealing	H				H	H	H	H			H		H		H	H	H	H	H								
New Package	●	●	●	●	●	●	●	●	●	●	●	●	●	B	**H**	**H**	**H**	H	●	●	●			●		●	F
Test Process/Sequence		●																									
Package Marking														**B**													
Assembly Site Transfer	●	●	●	●	●	●	●	●	●		●	●	●	●			**H**	H	●	●		●	●	●			AGISX

A Acoustic Microscopy
B If not laser etched
C Only for Leadframe Plating change
D Only for Lead Finish change
E If Applicable
F Finite Element Analysis
G Glass Transition Temperature
H Hermetic device only
I Infant Mortality Rate
M Power MOS/**IGBT** devices only
P CV Plot (MOS only)
R Spreading Resistance Profile
S Steady State Mortality Rate
X X-Ray
1 If bond pads are affected
2 Verify #2 (package) post
3 Only for changes at the periphery
4 Only for oxide etches or etches prior to oxidation
5 For source or channel region changes
6 For field termination changes
7 For passivation changes
8 For contact changes
9 For epitaxial changes
0 Required for Schottky barrier changes.

APPENDIX 1 - Definition of a Qualification Family

The qualification of a particular process will be defined within, but not limited to, the categories listed below. The supplier will provide a complete description of each process and material of significance. There must be valid and obvious links between the data and the subject of qualification.

For devices to be categorized in a qualification family, they all must share the same major process and materials elements as defined below. For each qualification test, two or more qualification families can be combined if the reasoning is technically sound (i.e., supported by rationale clearly detailing similarity). All devices using the same process and materials are to be categorized in the same qualification family for that process and are acceptable by association when one family member successfully completes qualification with the exception of the device specific requirements of section 4.2.

Prior qualification data 3 years old or newer obtained from a device in a specific family may be extended to the qualification of subsequent devices in that family provided the supplier can insure no process changes have been made.

For broad changes that involve multiple attributes (e.g. site, material(s), process(es)), refer to section 2.3 that allows for the selection of worst-case test vehicles to cover all the possible permutations.

1. Fab Process

Each process technology (e.g., Power MOS, Bipolar, Zener etc.) must be considered and subjected to stress-test qualification separately. No matter how similar, processes from one fundamental fab technology cannot be used for the other.

Family requalification with the appropriate tests is required when the process or a material is changed. The important attributes defining a qualification family are listed below:

1) Wafer Fab Technology

- Power MOS
- Small Signal MOS
- Power Bipolar
- Small Signal Bipolar
- IGBT
- Optocoupler
- Phototransistors
- Rectifier
- Ultrafast Rectifier
- Schottky Rectifier
- Zener
- Transient Voltage Suppressor
- Pin
- Varactor
- Germanium
- Gallium Arsenide
- Photo Diodes
- SCRs
- LEDs

2) **Wafer Fab Process** - consisting of the same attributes listed below:
   - Process flow
   - Layout design rules
   - Doping Material (E.G. Antimony, Arsenic, Boron)
   - Number of masks
   - Cell Density (where applicable)
   - Lithographic process (e.g. contact vs. projection, E-beam vs. X-ray, photoresist polarity)
   - Doping process (e.g. diffusion vs. ion implantation)
   - Passivation/Glassivation material and thickness range
   - Oxidation process and thickness range (for gate and field oxides)
   - Front/back metallization material, thickness range and number of levels

3) **Wafer Fab Site**

2. Assembly Process

The processes for each package type must be considered and subjected to stress-test qualification separately. For devices to be categorized in a qualification family, they all must share the same major process and material elements as defined below. Family requalification with the appropriate tests are required when the process or a material is changed. The supplier must submit technical justification to the user(s) to support the acceptance of generic data with package type, die sizes, paddle sizes and die aspect ratios different than the device being considered for stress-test qualification.

The important attributes defining a qualification family are listed below:

1) **Package Type** (e.g. TO-220, SOT-23, DO-41, SOIC, etc.)
   - Range of paddle (flag) size qualified for the die size/aspect ratio under consideration.

2) **Assembly Process** - consisting of the same attributes listed below:
   - Leadframe base material
   - Leadframe plating (internal and external to the package)
   - Die attach material / method
   - Wire bond material, wire diameter, and process
   - Plastic mold compound or other encapsulation material

3) **Assembly Site**

3. Qualification of Multiple Families and Sites

When the specific product or process attribute to be qualified or requalified will affect more than one wafer fab family or assembly family, the qualification test vehicles should be three lots of a single device type from each of the technology and package families that are projected to be most sensitive to the changed attribute with sample sizes split to include a minimum of 30 pieces from each of 3 assembly lots from each assembly / fab site.

Below is the recommended process for qualifying changes across many process and product families:

1) Identify all products affected by the proposed process changes.

2) Identify the critical structures and interfaces potentially affected by the proposed change.

3) Identify and list the potential failure mechanisms and associated failure modes for the critical structures and interfaces. Note that steps 1 - 3 are equivalent to the creation of an FMEA.

4) Define the product groupings or families based upon similar characteristics as they relate to the technology process and package families and device sensitivities to be evaluated, and provide technical justification for these groupings.

5) Provide the qualification test plan, including a description of the change, the matrix of tests and the representative products, which will address each of the potential failure mechanisms and associated failure modes.

6) Robust process capability must be demonstrated at each site (e.g. control of each process step, capability of each piece of equipment involved in the process, equivalence of the process step-by-step across all affected sites) for each of the affected process step(s).

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APPENDIX 2 - Certification of Design, Construction and Qualification

The following information, as applicable, is required to identify a component that has met the requirements of this specification. This page is available as a stand-alone document located on the AEC website.

Supplier		Glass transition temperature (T_G)	
User P/N		Lead material type	
Generic P/N		Lead material manufacturer	
Supplier P/N		Lead plating/ Coating and thickness	
Die line or Process		Leadframe material type	
Wafer Diameter		Header plating (Die land area)	
Wafer Fab Site(s)		Max junction temperature (T_j)	
ID method (multiple sites)		Max thermal resistance junction to case (θ_{JC})	
Assembly Location(s)		Max thermal resistance junction to ambient (θ_{JA})*	
Test Location(s)		Front metal type	
Die attach Method & Material		Front metal thickness	
Bond wire material & dia.		Back metal type (All layers)	
Bond type & method (at die)		Back metal thickness (All layers)	
Bond type & method (at leadframe)		Die conformal coating	
No. of bonds over active area		Die size (width x length x thickness) in mils	
Package material type & ID		Die passivation & thickness range	
Package material manufacturer		No. of mask steps	

* Show conditions (i.e. pad size, board material, copper thickness, etc.)

Attachments:
1) Die Photo
2) Package outline drawing
3) Die cross-section drawing
4) Wirebond & die placement diagram
5) Test circuits, bias levels and conditions

Requirements:
1) A separate Certificate of Design, Construction and Qualification shall be submitted for each P/N and assembly location.
2) Document shall be signed by a responsible individual at the supplier who can verify that all of the above information is correct. Type name and sign.

Completed by: Date:	Certified by: Date:
(Typed/Printed) (Signature) (Title)	

APPENDIX 3 - Qualification Test Plan

The supplier is requested to complete and submit the Discrete Semiconductor Qualification Test Plan as part of the pre-launch Control Plan whenever qualification submission is required. Acceptance and subsequent sign-off of the plan will establish a qualification agreement between the user and the supplier determining requirements for both new parts and process changes prior to commencement of testing. Where "family" data is being proposed, the plan will document how the reliability testing previously completed fulfills the requirements outlined in this specification. An approved copy of the Qualification Test Plan shall be included with each qualification submission.

The test plan section of the form should detail ONLY the testing that will be performed on the specific part shown. For process change qualifications, multiple parts can be included on the same plan. Supporting generic or family data reports should be noted in the comment section and attached. When requesting use of generic or family data, attach a separate page detailing similarities or differences between parts referencing the criteria in Appendix 1. There must be valid and obvious links between the data and the subject of qualification.

The example below is provided to demonstrate how the Qualification Test Plan Form, found on the AEC website, should be used. In this case, a bipolar discrete device was chosen as being representative of a typical new part qualification requesting reduced component testing by including generic test data. The part comes from a supplier who previously qualified the package, assembly site etc. This example is shown for illustration purposes only and should not limit any requirements from Table 1 herein.

Page 1 of 1 — Discrete Semiconductor Component Qualification Plan — Rev: A 4/24/04

User P/N:	N611045BFDAARA	User Component Engineer:	John Doe
User Spec. #:	ES-N611045BFDAARA	General Specification:	AEC-Q101
Supplier:	Sam's Discount Semiconductors (SDS)	Supplier Manufacturing Site:	Shanghai, China
Supplier Generic P/N:	PZT3904	Required PPAP Submission Date:	7/1/04
Supplier Internal P/N:	SDF-3417-AR	Family Type:	Bipolar SOT-223, 20 mil square die
Reason for Qual:	New device qualification		

Item	Test	Test Conditions	Exceptions	Est. Start	Est. Comp.	# Lots	S. S.	Remarks
1	TEST	Electrical Characterization @25C		4/1/04	4/5/04	all	all	
2	Preconditioning	per AEC-Q101		4/8/04	4/10/04	all	all	
3	External Visual	per AEC-Q101		4/11/04	4/12/04	all	all	
4	Parametric Verification	Characterization @-55, 25, & 150C		4/15/04	4/19/04	3	30	
5	HTRB	Reverse biased @64V		4/22/04	6/24/04	1	77	
6	HTGB		N/A Bipolar device					
7	Temperature Cycling		Use attached generic data for this package related test.					generic data uses -65/150C (rather than -55C)
8	Autoclave	Ta = 121C, P = 15PSIG, RH = 100%	Use attached generic data for this package related test.					
9	H3TRB	Reverse biased @64V		4/22/04	6/24/04	1	77	
10	IOL		T on/off = 2 minutes, 15,000 cycles	4/22/04	6/24/04	1	77	SDS internal standard
11	ESD	per AEC-Q101		4/22/04	6/24/04	1	30	
12	DPA	per AEC-Q101		6/24/04	6/24/04	1	2	2 ea from H3TRB and TC only.

Comments:
1. Supplier requests 1 lot qualification of this device type in addition to attached rel reports fo similar parts.
   Rel Report #23-602 (PZT3906, the PNP compliment of this part) and #23-665 (PZTA62 NPN Darlington with larger 35 MIL die)
2. In addition, the die is qualified in SOT-23 version of this device, the SOT-223 package is qualified with larger (35 MIL) bipolar die (N611002BFDAARA & N611007BFDBARA).
3. Attached quarterly reliability results for 2002 & 2003 on generic PZT3904.
4. These devices all share the same wafer and assembly processes.
5. Tests 14-23 covered by annual SOT-223 packaging qual last approved 11/03.

Prepared by (supplier):	Approved by (User):
Typed/Printed	Typed/Printed
Signature	Signature
Title	Title

Example of Discrete Semiconductor Qualification Test Plan

APPENDIX 4 - Data Presentation Format

The supplier is required to complete and submit an Environmental Test Summary and Parametric Verification Summary with each Discrete Semiconductor PPAP submittal. Figure 4-1 is an example of a completed Environmental Test Summary. Figure 4-2 is an example of a completed Parametric Verification Summary. The format of both summaries shall be followed. Soft copies of the formats may be found on the AEC website or is available upon request.

Production Part Approval -
Environmental Test Summary

Supplier		User Part Number			
Sam's Discount Semiconductors		N611045BFDAARA			
Name Of Laboratory		Part Description			
SDS Qual Lab		Bipolar SOT-223 Transistor			
Test #	Test Description	Test Conditions	# Lots	# Tested	# Failed
2	Preconditioning	Per Spec	1	77	0
3	External Visual	Per Spec	3	381	0
5	HTRB	Reverse Biased @ 64V	1	77	0
10	H3TRB	Reverse Biased @ 64V	1	77	0
11	IOL	T on/off = 2 min., 15K Cycles	1	77	0
12	ESD	Per Spec	1	30	N/A
13	DPA	Per Spec	1	2	0

Figure 4-1 Environmental Test Summary Example

Production Part Approval -
Parametric Verification Summary

Supplier	User Part Number
Sam's Discount Semiconductors	N611045BFDAARA
Lot Number	Temperature
JB-117A (Test Lot 2)	25 Degrees C

Test Name	Unit	Spec LSL	Spec USL	MIN	MAX	MEAN	STD.DEV.	Cpk
BV_{CEO}	V	40	-	46.3	54.2	49.4	1.1	1.45
BV_{CBO}	V	60	-	65.7	73.9	69.4	1.21	1.7
BV_{EBO}	V	6	-	6.7	8.3	7.2	0.9	1.64
I_{BL}	nA	-	50	0.15	37.2	24.2	0.2	10.2
I_{CEX}	nA	-	50	0.02	12.3	8.7	0.45	9.8
$h_{FE}1$	--	40	-	45.6	93.2	72.3	6.7	1.8
$h_{FE}2$	--	70	-	71.7	114.2	96.2	5.2	2.01
$h_{FE}3$	--	100	300	103.2	294.4	187.3	19.1	2.7
$h_{FE}4$	--	60	-	78.7	114.3	98.7	3.7	1.95
$h_{FE}5$	--	30	-	37.2	46.2	41.2	0.9	2.7
$V_{CESAT}1$	V	-	0.2	0.07	0.17	0.12	0.011	1.81
$V_{CESAT}2$	V	-	0.3	0.16	0.25	0.21	0.01	1.41
$V_{BESAT}1$	V	0.65	0.85	0.71	0.81	0.76	0.01	2
$V_{BESAT}2$	V	-	0.95	0.56	0.86	0.63	0.015	3.7
f_T	MHz	300	-	463	587	505	12	1.72
C_{OBO}	pF	-	4	2.7	3.6	3.13	0.15	2.1
C_{IBO}	pF	-	8	2.6	4.5	3.25	0.2	2.2
h_{IE}	Kohm	1	10	2.3	4.6	3.7	0.2	1.8
h_{RE}	10^{-4}	0.5	8	0.79	1.57	1.23	0.13	1.83
h_{fe}	--	100	400	214	363	303	9	3.8

Figure 4-2 Parametric Verification Summary Example
Other equivalent formats are acceptable if approved by the user

APPENDIX 5 - MINIMUM PARAMETRIC TEST REQUIREMENTS

For Table 1 Test #1 (Pre & Post Stress Electrical Test), The following electrical parameters shall be used (as a minimum):

Transistors

Bipolar	FET	IGBT
BV_{CEX}	BV_{DSS}	BV_{CES}
I_{CEX}	I_{DSS}	I_{CES}
I_{EBX} or I_{CBX}	I_{GSS}	I_{GES}
$V_{CE(SAT)}$	$R_{DS(ON)}$	$V_{CE(SAT)}$
h_{FE}	G_{fs} (if specified)	h_{FE}
	$V_{GS(th)}$ or $V_{GS(OFF)}$	$V_{GE(th)}$

Diodes

V_F, I_R, V_{BR} (Diodes)
V_F, I_R, I_V (LEDs)
V_Z or V_{CLAMP} (Zeners)
R_F (PIN Diode, if applicable)

Varactors

I_R, C_T

Opto Electronics

V_F, I_R, V_{BR} (Diodes)
V_F, I_R, I_V (LEDs)
BV_{CEO}, I_{CEO}, $V_{CE(SAT)}$ (Transistors)

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Revision History

REV	DATE OF CHANGE	BRIEF SUMMARY AND PURPOSE OF CHANGE
-	May 15, 1996	Initial Release
A	May 5, 1999	General Revision - Corrected errors, made clarifications, changed lot requirements. Removed CDF and “Automotive Grade” designations throughout.
B	July 25, 2000	Update signature block on page 1; Removed "Parts must be mounted to test boards." from "Additional Requirements" for Pre-conditioning in Table 1 page 8; Changed "IOL" to "PTC" in "Additional Requirements" for Power and Temperature Cycle in Table 1 page 9; Removed revision from "Reference" for Resistance to Solder Heat in Table 1 page 10 (i.e. B-106-A becomes B-106); Added note U to "Legend for Tables 1 and 2" on page 11.
C	June 29, 2005	Revised table numbers throughout document Section 1.1.2 - Definition of Stress Test Qualification clarification Section 1.2.2 – Delete one, add two Industrial standard references Section 1.2.3 – Delete two, add one AEC standard references Section 1.2.4 – Add two quality standard references Section 2.1 – Define what "AEC Q101 Qualified" means Section 2.3 – Reference to Table 1 Table 1 – Part Qualification/Requalification Lot Requirements Section 2.4.3 - Editorial Section 2.5 – Current leakage measurement accuracy limit Section 3.2 – Requirements of supplier for process changes Section 3.2.1 – Process Change definition Section 3.2.2 – Remove reference Section 4.2 – Family data disallowance clarification Section 4.3 – Charged Device Model limitations Section 4.4 – Reference to TS-16949 Table 2: Qualification Test Definitions Test 2 – PC before PTC required Test 3 – JEDEC reference Test 5 – Ambient/Junction temperature requirements Test 6 - Ambient/Junction temperature requirements Test 7 – Temperature extremes requirement Test 8 – Added note Test 9 – Ambient temperature and test requirements Test 9alt – New alternative test option Test 10 – Test requirement and added note Test 10alt – Test criteria, requirement and added note Test 11 – Criteria for CDM requirement Test 12 – HAST as alternative Test 20 – Allowance for alteration of test method Test 21 – Clarification of test method Legend – 5 new notes to table 2 Table 2A – IOL/PTC cycling requirements per package type Table 2B – Solder conditions per package type Table 3 – New changes and notes added Appendix 2 – Reference to website, clarify requirements Appendix 3 – Reference to website Appendix 4 - Reference to website

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Attachments

AEC-Q101-001	Electrostatic Discharge Test - Human Body Model
AEC-Q101-002	Electrostatic Discharge Test - Machine Model
AEC-Q101-003	Wire Bond Shear Test
AEC-Q101-004	Miscellaneous Test Methods
AEC-Q101-005	Electrostatic Discharge Test – Capacitive Discharge Model

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ATTACHMENT 1

AEC - Q101-001 Rev-A

HUMAN BODY MODEL (HBM) ELECTROSTATIC DISCHARGE (ESD) TEST

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Component Technical Committee

METHOD - 001

DISCRETE COMPONENT
HUMAN BODY MODEL (HBM)
ELECTROSTATIC DISCHARGE (ESD) TEST

1. SCOPE

1.1 Description:

The purpose of this specification is to establish a reliable and repeatable procedure for determining the HBM ESD sensitivity for discrete components.

1.2 Reference Documents:

EOS/ESD Association Specification STM5.1
JEDEC Specification EIA/JESD22-A114

1.3 Terms and Definitions:

The terms used in this specification are defined as follows.

1.3.1 Component Failure:

A condition in which a component does not meet all the requirements of the acceptance criteria, as specified in section 5, following the ESD test.

1.3.2 Device Under Test (DUT):

An electronic component being evaluated for its sensitivity to ESD.

1.3.3 Electrostatic Discharge (ESD):

The transfer of electrostatic charge between bodies at different electrostatic potentials.

1.3.4 Electrostatic Discharge Sensitivity:

An ESD voltage level resulting in component failure.

1.3.5 ESD Simulator:

An instrument that simulates the human body model ESD pulse as defined in this specification.

1.3.6 Human Body Model (HBM) ESD:

An ESD pulse meeting the waveform criteria specified in this test method.

1.3.7 Maximum Withstanding Voltage:

The maximum ESD voltage at which, and below, the component is determined to pass the failure criteria requirements specified in section 4.

1.3.8 PUT:

The pin and/or terminal under test.

1.3.9 Ringing current (IR):

The high frequency current oscillation usually following the pulse rise time.

1.3.10 Worst Case Pin and/or Terminal Pair (WCP):

WCP is the pin and/or terminal pair representing the worst case waveform that is within the limits and closest to the minimum or maximum parameter values as specified in Table 1. The WCP shall be identified for each socket.

2. EQUIPMENT:

2.1 Test Apparatus:

The apparatus for this test consists of an ESD pulse simulator and DUT socket. Figure 1 shows a typical equivalent HBM ESD circuit. Other equivalent circuits may be used, but the actual simulator must be capable of supplying pulses that meet the waveform requirements of Table 1, Figure 2, and Figure 3.

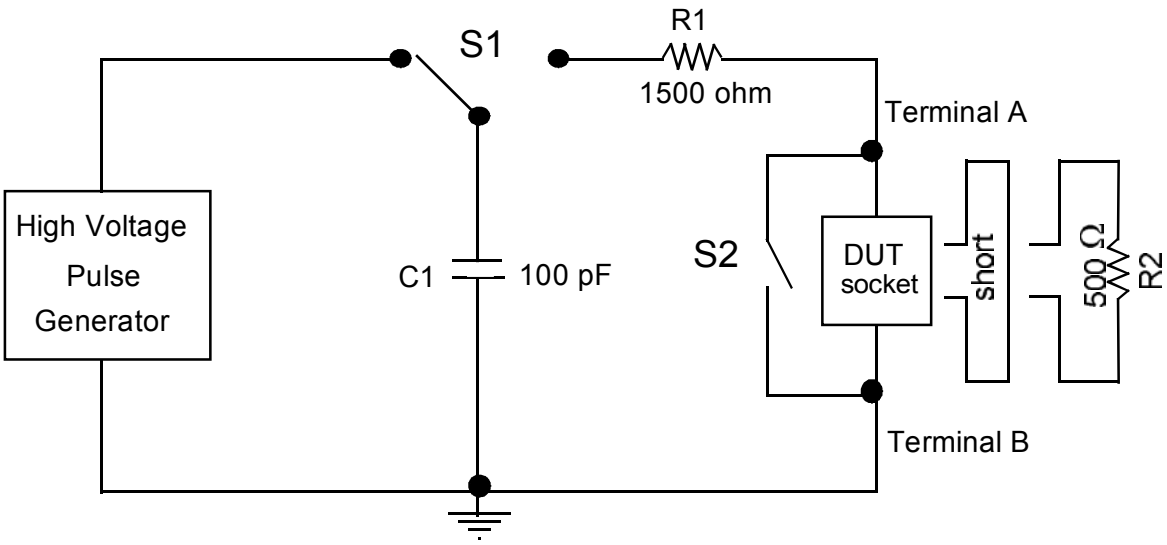


Figure 1: Typical Equivalent HBM ESD Circuit

Notes:

1. Figure 1 is shown for guidance only; it does not attempt to represent all associated circuit components, parasitics, etc..
2. The performance of any simulator is influenced by its parasitic capacitance and inductance.
3. Precautions must be taken in simulator design to avoid recharge transients and multiple pulses.
4. R2, used for Equipment Qualification as specified in section 2.3, shall be a low inductance, 1000 Volt, 500 ohm resistor with ±1% tolerance.
5. Piggybacking of DUT sockets (the insertion of secondary sockets into the main DUT socket) is allowed only if the combined piggyback set (main DUT socket with the secondary DUT socket inserted) waveform meets the requirements of Table 1, Figure 2, and Figure 3.
6. Reversal of terminals A and B to achieve dual polarity is not permitted
7. S2 should be closed 10 to 100 milliseconds after the pulse delivery period to ensure the DUT socket is not left in a charged state. S2 should be opened at least 10 milliseconds prior to the delivery of the next pulse.

2.2 Measurement Equipment:

Equipment shall include an oscilloscope and current probe to verify conformance of the simulator output pulse to the requirements of this document as specified in Table 1, Figure 2, and Figure 3.

2.2.1 Current Probe:

The current probe shall have a minimum bandwidth of 350 Mhz and maximum cable length of 1 meter (Tektronix CT-1 or equivalent).

2.2.2 Evaluation Loads:

The two evaluation loads shall be: 1) a low inductance, 1000 volt, 500 ohm sputtered film resistor with + 1% tolerance, and 2) an 18 AWG tinned copper shorting wire. The lead length of both the shorting wire and the 500 ohm resistor shall be as short as possible and shall span the maximum distance between the worst case pin and/or terminal pair (WCP) while passing through the current probe as defined in section 2.2.1.

2.2.3 Oscilloscope:

The oscilloscope and amplifier combination shall have a minimum bandwidth of 350 Mhz, a minimum sensitivity of 100 milliamperes per large division and a minimum visual writing speed of 4 cm per nanosecond.

2.3 Equipment Qualification:

Equipment qualification must be performed during initial acceptance testing or after repairs are made to the equipment that may affect the waveform. The simulator must meet the requirements of Table 1 and Figure 2 for five (5) consecutive waveforms at all voltage levels using the worst case pin and/or terminal pair (WCP) on the highest pin count, positive clamp test socket DUT board with the shorting wire per Figure 1. The simulator must also meet the requirements of Table 1 and Figure 3 for five (5) consecutive waveforms at the 1000 volt level using the worst case pin and/or terminal pair (WCP) on the highest pin count, positive clamp test socket DUT board with the 500 ohm load per Figure 1. Thereafter, the test equipment shall be periodically qualified as described above; a period of one (1) year is the maximum permissible time between full qualification tests.

2.4 Simulator Waveform Verification:

The performance of the simulator can be dramatically degraded by parasitics in the discharge path. Therefore, to ensure proper simulation and repeatable ESD results, it is recommended that waveform performance be verified on the worst case pin and/or terminal pair (WCP) using only the shorting wire per section 2.4.1. The worst case pin and/or terminal pair (WCP) for each socket and DUT board shall be identified and documented. The waveform verification shall be performed when a socket/mother board is changed or on a weekly basis (if the equipment is used for at least 20 hours). If at any time the waveforms do not meet the requirements of Table 1 and Figure 2 at either the 1000 or 4000 volt level, the testing shall be halted until waveforms are in compliance.

2.4.1 Waveform Verification Procedure:

a. With the required DUT socket installed and with no component in the socket, attach a shorting wire in the DUT socket such that the worst case pin and/or terminal pair (WCP) is connected between terminal A and terminal B as shown in Figure 1. Place the current probe around the shorting wire.

b. Set the horizontal time scale of the oscilloscope at 5 nanoseconds per division or less.

c. Initiate a positive pulse at either the 1000 or 4000 volt level per Table 1. The simulator shall generate only one (1) waveform per pulse applied.

d. Measure and record the rise time, peak current and ringing current. All parameters must meet the limits specified in Table 1 and Figure 2.

e. Initiate a negative pulse at either the 1000 or 4000 volt level per Table 1. The simulator shall generate only one (1) waveform per pulse applied.

f. Measure and record the rise time, peak current and ringing current. All parameters must meet the limits specified in Table 1 and Figure 2.

g. Set the horizontal time scale of the oscilloscope at 100 nanoseconds per division or greater and initiate a positive pulse at either the 1000 or 4000 volt level per Table 1. The simulator shall generate only one (1) waveform per pulse applied.

h. Measure and record the decay time and ringing current. All parameters must meet the limits specified in Table 1 and Figure 2.

i. Initiate a negative pulse at either the 1000 or 4000 volt level per Table 1. The simulator shall generate only one (1) waveform per pulse applied.

j. Measure and record the decay time and ringing current. All parameters must meet the limits specified in Table 1 and Figure 2.

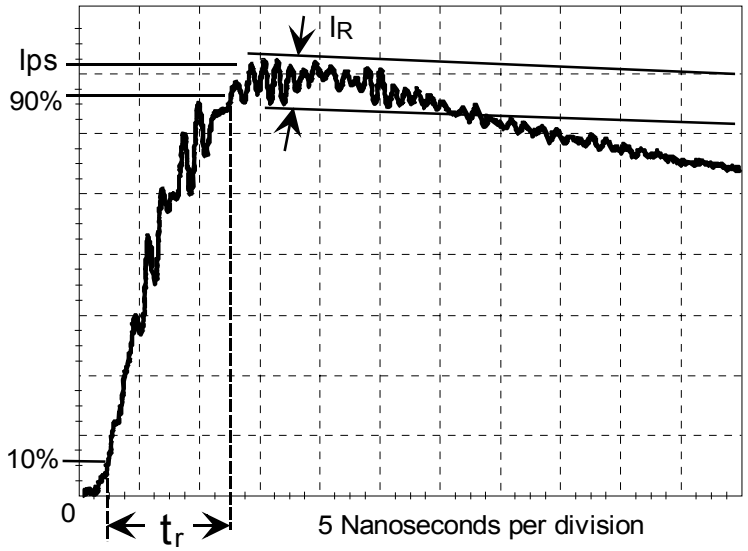
Table 1: HBM Waveform Specification

Voltage Level (V)	Ipeak for Short, I_{ps} (A)	Ipeak for 500 Ohm * I_{pr} (A)	Rise Time for Short, t_r (ns)	Rise Time for 500 Ohm * t_{rr} (ns)	Decay Time for Short, t_d (ns)	Ringing Current I_R (A)
1000	0.60 - 0.74	.375 - .55	2.0 - 10	5.0 - 25	130 - 170	15% of I_{ps} and I_{pr}
2000	1.20 - 1.46	Not Applicable	2.0 - 10	Not Applicable	130 - 170	15% of I_{ps} and I_{pr}
4000	2.40 - 2.94	Not Applicable	2.0 - 10	Not Applicable	130 - 170	15% of I_{ps} and I_{pr}
8000	4.80 - 5.86	Not Applicable	2.0 - 10	Not Applicable	130 - 170	15% of I_{ps} and I_{pr}

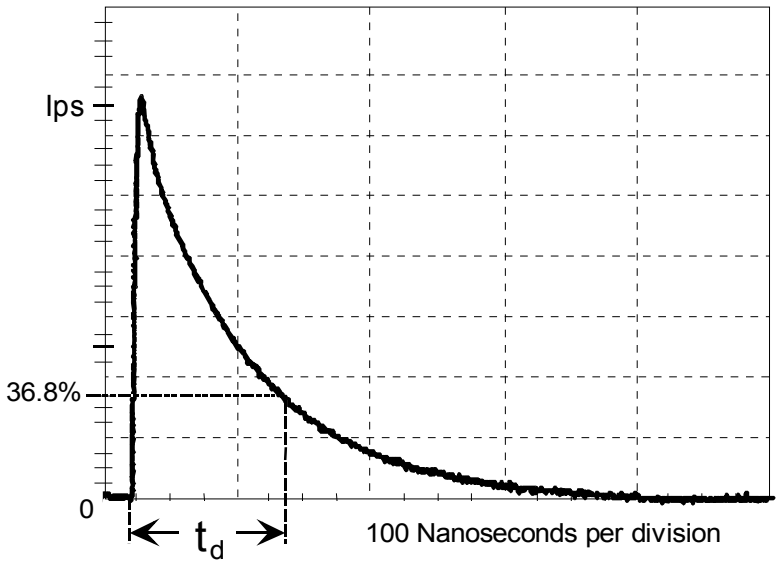
*** The 500 ohm load is used only during Equipment Qualification as specified in section 2.3.**

2.5 Automated ESD Test Equipment Relay Verification:

If using automated ESD test equipment, the system diagnostics test shall be performed on all high voltage relays per the equipment manufacturer's instructions. This test normally measures continuity and will identify any open or shorted relays in the test equipment. Relay verification must be performed during initial equipment qualification and on a weekly basis. If the diagnostics test detects relays as failing, all sockets boards using those failed relays shall not be used until the failing relays have been replaced. The test equipment shall be repaired and requalified per section 2.3.

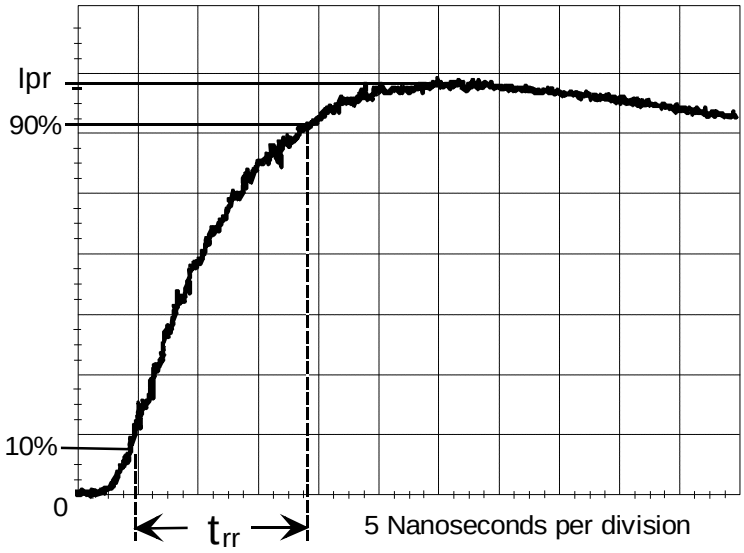


(a) Pulse rise time, (t_r)



(b) Pulse decay time, (t_d)

Figure 2: HBM Current Waveforms through a Shorting Wire



(a) Pulse rise time, (t_{rr})

Figure 3: HBM Current Waveform through a 500 Ohm Resistor *

*** The 500 ohm load is used only during Equipment Qualification as specified in section 2.3.**

3. TEST PROCEDURE:

3.1 Sample Size:

Each sample group shall be composed of ten (10) components per stress voltage level (for a total sample size of 30 components as specified in Table 1 of AEC-Q101). Each sample group shall be stressed at one (1) stress voltage level, following the test flow diagram of Figure 4, using all pin and/or terminal combinations specified in section 3.2. Each stress voltage level requires a new sample group of ten (10) components.

3.2 Pin and/or Terminal Combinations:

Each pair of pins and/or terminals and all combinations of pin and/or terminal pairs for each component shall be subjected to test pulses at each stress voltage polarity following the ESD levels stated in Figure 4. Any pin and/or terminal not under test shall be in an electrically open (floating) state.

3.3 Test Temperature:

Each component shall be subjected to ESD pulses at room temperature.

3.4 Measurements:

Prior to ESD testing, complete parametric testing (initial electrical verification) shall be performed on all sample groups and all components in each sample group per applicable user device specification at room temperature followed by hot temperature, unless specified otherwise in the user device specification. A data log of each component shall be made listing all parameter measurements as defined in Table 2. The data log will be compared to the parameters measured during final electrical verification testing to determine the failure criteria of section 4.

3.5 Detailed Procedure:

The ESD testing procedure shall be per section 3.2, Figure 4, and as follows:

a. Follow the recommended test flow diagram of Figure 4.

b Connect a selected PUT (see section 3.2) to terminal B.

c. Connect an individual component pin and/or terminal to terminal A. Leave all other component pins and/or terminals unconnected.

d. Apply one (1) positive pulse at the specified voltage to the PUT. Wait a minimum of 500 milliseconds before applying the next test pulse. The use of three (3) pulses at each stress voltage polarity is also acceptable, and may be required per user agreement.

e. Apply one (1) negative pulse at the specified voltage to the PUT. Wait a minimum of 500 milliseconds before applying the next test pulse. The use of three (3) pulses at each stress voltage polarity is also acceptable, and may be required per user agreement.

f. Disconnect the PUT from testing and connect the next individual component pin and/or terminal to terminal A. Leave all other component pins and/or terminals unconnected.

g. Repeat steps (d) through (f) until every pin and/or terminal not connected to terminal B is pulsed at the specified voltage (see section 3.2).

h. Repeat steps (b) through (g) until all pin and/or terminal combinations have been stressed.

i. Test the next component in the sample group and repeat steps (b) through (h) until all components in the sample group have been tested at the specified voltage level.

j. Submit the components for complete parametric testing (final electrical verification) per the user device specification at room temperature followed by hot temperature, unless specified otherwise in the user device specification, and determine whether the components meet the failure criteria requirements specified in section 4. It is permitted to perform the parametric testing (final electrical verification) per user device specification after all sample groups have been tested.

k. Using a new sample group, select the next stress voltage level as specified in Figure 4 and repeat steps (b) through (j)

l. Repeat steps (b) through (k) until failure occurs or the maximum withstanding voltage level has been reached.

4. FAILURE CRITERIA:

A component will be defined as a failure if, after exposure to ESD pulses, the component fails any of the following criteria:

1. The component exceeds the allowable shift values for the specific key parameters listed in Table 2. Other component parameters and allowable shift values may be specified in the user device specification. During initial parametric testing, a data log shall be made for each component listing the applicable parameter measurement values. This data log will be compared to the parameters measured during final parametric testing to determine the shift value. Components exceeding the allowable shift value will be defined as a failure.

2. The component no longer meets the user device specification requirements. Complete parametric testing (initial and final electrical verification) shall be performed per applicable user device specification at room temperature followed by hot temperature, unless specified otherwise in the user device specification.

Table 2: Key Parameters and Allowable Shift Values

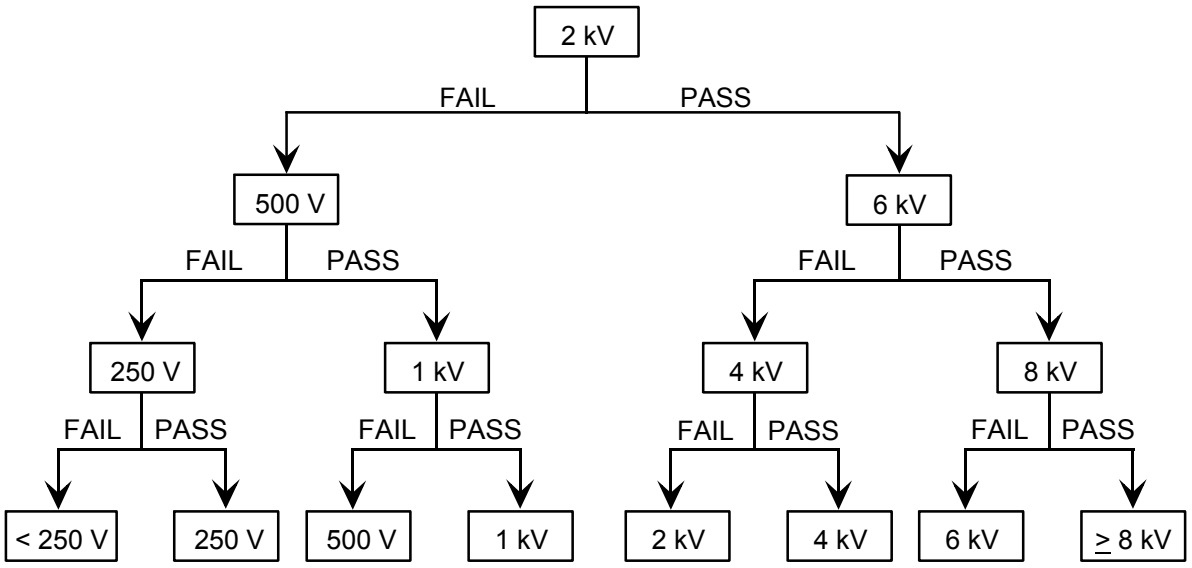
Component Type	Parameters	Maximum Allowable Shift Values
Bipolar	I_{CES}, I_{CBO}, and I_{EBO}	Ten times (10X) the initial measurement
FET	I_{DSS} and I_{GSS}	Ten times (10X) the initial measurement
IGBT	I_{CES} and I_{GES}	Ten times (10X) the initial measurement
Diode	I_R	Ten times (10X) the initial measurement

5. ACCEPTANCE CRITERIA:

A component passes a voltage level if all components stressed at that voltage level and below pass. All the samples must meet the measurement requirements specified in section 3 and the failure criteria requirements specified in section 4. Using the classification levels specified in Table 3, classify the components according to the highest ESD voltage level survived during ESD testing. The ESD withstanding voltage shall be defined for each component by the supplier.

Table 3: Discrete Component HBM ESD Classification Levels

Component Classification	Maximum Withstand Voltage
H0	≤ 250 V
H1A	> 250 V to ≤ 500 V
H1B	> 500 V to ≤ 1000 V
H1C	> 1000 V to ≤ 2000 V
H2	> 2000 V to ≤ 4000 V
H3A	> 4000 V to ≤ 8000 V
H3B	> 8000 V



Note 1: Classify the components according to the highest ESD voltage level survived during ESD testing.

Figure 4: Discrete Component HBM ESD Test Flow Diagram

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Revision History

Rev #	Date of change	Brief summary listing affected sections
-	May 15, 1996	Initial Release.
A	July 18, 2005	Revised the following: Sections 1.2, 2.1, 3.1, 3.5 (d and e), and 5; Tables 1 and 3; Figure 1. Revision to section 3.5 (d and e) reflects a change from three (3) ESD pulses with a one (1) second minimum delay between consecutive ESD pulses at each stress polarity to one (1) ESD pulse with a 500 millisecond minimum delay between consecutive ESD pulses. This change is required to align with industry standards. The use of three (3) ESD pulses with a one (1) second minimum delay between consecutive ESD pulses is also acceptable, and may be required per user agreement. Revision to Table 1 reflects a $\pm$10% tolerance applied to all Ips (Ipeak for short) parameter values.

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ATTACHMENT 2

AEC - Q101-002 Rev-A

MACHINE MODEL (MM) ELECTROSTATIC DISCHARGE (ESD) TEST

Automotive Electronics Council

Component Technical Committee

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Automotive Electronics Council
Component Technical Committee

METHOD - 002

DISCRETE COMPONENT
MACHINE MODEL (MM)
ELECTROSTATIC DISCHARGE (ESD) TEST

1. SCOPE

1.1 Description:

The purpose of this specification is to establish a reliable and repeatable procedure for determining the MM ESD sensitivity for discrete components.

1.2 Reference Documents:

EOS/ESD Association Specification STM5.2
JEDEC Specification EIA/JESD22-A115

1.3 Terms and Definitions:

The terms used in this specification are defined as follows.

1.3.1 Component Failure:

A condition in which a component does not meet all the requirements of the acceptance criteria, as specified in section 5, following the ESD test.

1.3.2 Device Under Test (DUT):

An electronic component being evaluated for its sensitivity to ESD.

1.3.3 Electrostatic Discharge (ESD):

The transfer of electrostatic charge between bodies at different electrostatic potentials.

1.3.4 Electrostatic Discharge Sensitivity:

An ESD voltage level resulting in component failure.

1.3.5 ESD Simulator:

An instrument that simulates the machine model ESD pulse as defined in this specification.

1.3.6 Machine Model (MM) ESD:

An ESD pulse meeting the waveform criteria specified in this test method, approximating an ESD pulse from a machine or mechanical equipment.

1.3.7 Major Pulse Period (t_{pm}):

The time (t_{pm}) measured between first and third zero crossing points.

1.3.8 Maximum Withstanding Voltage:

The maximum ESD voltage at which, and below, the component is determined to pass the failure criteria requirements specified in section 4.

1.3.9 PUT:

The pin and/or terminal under test.

1.3.10 Worst Case Pin and/or Terminal Pair (WCP):

WCP is the pin and/or terminal pair representing the worst case waveform that is within the limits and closest to the minimum or maximum parameter values as specified in Table 1. The WCP shall be identified for each socket. It is permissible to use the worst case pin and/or terminal pair that has been previously identified by the Discrete Component HBM ESD method (AEC - Q101-001) when performing the Simulator Waveform Verification as defined in section 2.4.

2. EQUIPMENT:

2.1 Test Apparatus:

The apparatus for this test consists of an ESD pulse simulator and DUT socket. Figure 1 shows a typical equivalent MM ESD circuit. Other equivalent circuits may be used, but the actual simulator must be capable of supplying pulses which meet the waveform requirements of Table 1, Figure 2, and Figure 3.

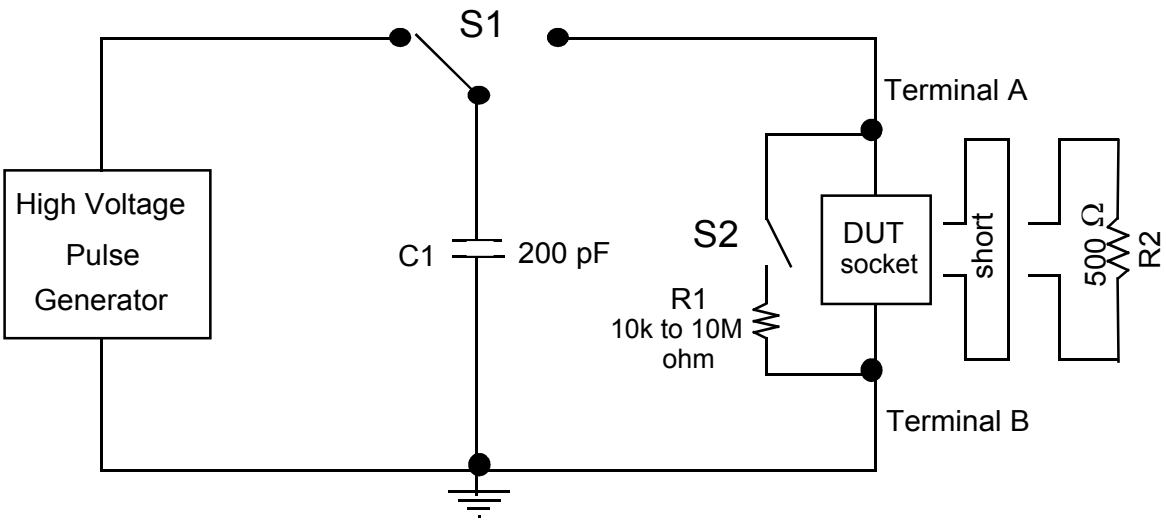


Figure 1: Typical Equivalent MM ESD Circuit

Notes:

1. Figure 1 is shown for guidance only; it does not attempt to represent all associated circuit components, parasitics, etc..
2. The performance of any simulator is influenced by its parasitic capacitance and inductance.
3. Precautions must be taken in simulator design to avoid recharge transients and multiple pulses.
4. R2, used for Equipment Qualification as specified in section 2.3, shall be a low inductance, 1000 Volt, 500 ohm resistor with ±1% tolerance.
5. Piggybacking of DUT sockets (the insertion of secondary sockets into the main DUT socket) is allowed only if the combined piggyback set (main DUT socket with the secondary DUT socket inserted) waveform meets the requirements of Table 1, Figure 2, and Figure 3.
6. Reversal of terminals A and B to achieve dual polarity is not permitted
7. S2 should be closed 10 to 100 milliseconds after the pulse delivery period to ensure the DUT socket is not left in a charged state. S2 should be opened at least 10 milliseconds prior to the delivery of the next pulse.

2.2 Measurement Equipment:

Equipment shall include an oscilloscope and current probe to verify conformance of the simulator output pulse to the requirements of this document as specified in Table 1, Figure 2, and Figure 3.

2.2.1 Current Probe:

The current probe shall have a minimum bandwidth of 350 Mhz and maximum cable length of 1 meter (Tektronix CT-1, CT-2, or equivalent). A CT-2 probe or equivalent should be used with voltages greater than 800 volts.

2.2.2 Evaluation Loads:

The two evaluation loads shall be: 1) a low inductance, 1000 volt, 500 ohm sputtered film resistor with ± 1% tolerance, and 2) an 18 AWG tinned copper shorting wire. The lead length of both the shorting wire and the 500 ohm resistor shall be as short as possible and shall span the maximum distance between the worst case pin and/or terminal pair (WCP) while passing through the current probe as defined in section 2.2.1.

2.2.3 Oscilloscope:

The oscilloscope and amplifier combination shall have a minimum bandwidth of 350 Mhz, a minimum sensitivity of 100 milliamperes per large division and a minimum visual writing speed of 4 cm per nanosecond.

2.3 Equipment Qualification:

Equipment qualification must be performed during initial acceptance testing or after repairs are made to the equipment that may affect the waveform. The simulator must meet the requirements of Table 1 and Figure 2 for five (5) consecutive waveforms at all voltage levels using the worst case pin and/or terminal pair (WCP) on the highest pin count, positive clamp test socket DUT board with the shorting wire per Figure 1. The simulator must also meet the requirements of Table 1 and Figure 3 for five (5) consecutive waveforms at the 400 volt level using the worst case pin and/or terminal pair (WCP) on the highest pin count, positive clamp test socket DUT board with the 500 ohm load per Figure 1. Thereafter, the test equipment shall be periodically qualified as described above; a period of one (1) year is the maximum permissible time between full qualification tests.

2.4 Simulator Waveform Verification:

The performance of the simulator can be dramatically degraded by parasitics in the discharge path. Therefore, to ensure proper simulation and repeatable ESD results, it is recommended that waveform performance be verified on the worst case pin and/or terminal pair (WCP) using only the shorting wire per section 2.4.1. The worst case pin and/or terminal pair (WCP) for each socket and DUT board shall be identified and documented. The waveform verification shall be performed when a socket/mother board is changed or on a weekly basis (if the equipment is used for at least 20 hours). If at any time the waveforms do not meet the requirements of Table 1 and Figure 2 at the 400 volt level, the testing shall be halted until waveforms are in compliance.

2.4.1 Waveform Verification Procedure:

a. With the required DUT socket installed and with no component in the socket, attach a shorting wire in the DUT socket such that the worst case pin and/or terminal pair (WCP) is connected between terminal A and terminal B as shown in Figure 1. Place the current probe around the shorting wire.

b. Set the horizontal time scale of the oscilloscope at 20 nanoseconds per division or greater.

c. Initiate a positive pulse at the 400 volt level per Table 1. The simulator shall generate only one (1) waveform per pulse applied.

d. Measure and record the first peak current, second peak current, and major pulse period. All parameters must meet the limits specified in Table 1 and Figure 2.

e. Initiate a negative pulse at the 400 volt level per Table 1. The simulator shall generate only one (1) waveform per pulse applied.

f. Measure and record the first peak current, second peak current, and major pulse period. All parameters must meet the limits specified in Table 1 and Figure 2.

Table 1: MM Waveform Specification

Voltage Level (V)	Positive First Peak Current for Short, I_{ps1} (A)	Positive Second Peak Current for Short, I_{ps2} (A)	Major Pulse Period for Short, t_{pm} (ns)	Positive First Peak Current for 500 Ohm *, I_{pr} (A)	Current at 100 ns for 500 Ohm *, I_{I00} (A)
100	1.5 – 2.0	67% to 90% of I_{ps1}	66 - 90	Not Applicable	Not Applicable
200	3.0 - 4.0	67% to 90% of I_{ps1}	66 - 90	Not Applicable	Not Applicable
400	6.0 - 8.1	67% to 90% of I_{ps1}	66 - 90	0.85 to 1.2	0.29 $\pm$ 10%
800	11.9 – 16.1	67% to 90% of I_{ps1}	66 - 90	Not Applicable	Not Applicable

*** The 500 ohm load is used only during Equipment Qualification as specified in section 2.3.**

2.5 Automated ESD Test Equipment Relay Verification:

If using automated ESD test equipment, the system diagnostics test shall be performed on all high voltage relays per the equipment manufacturer's instructions. This test normally measures continuity and will identify any open or shorted relays in the test equipment. Relay verification must be performed during initial equipment qualification and on a weekly basis. If the diagnostics test detects relays as failing, all sockets boards using those failed relays shall not be used until the failing relays have been replaced. The test equipment shall be repaired and requalified per section 2.3.

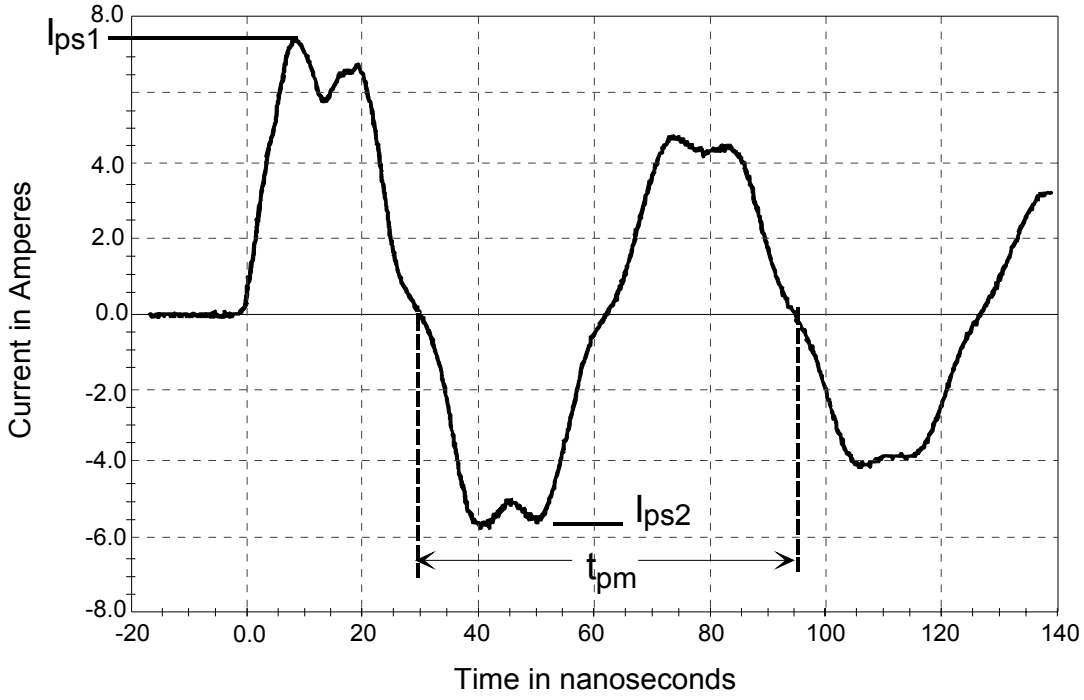


Figure 2: MM Current Waveform through a Shorting Wire, 400 volt discharge

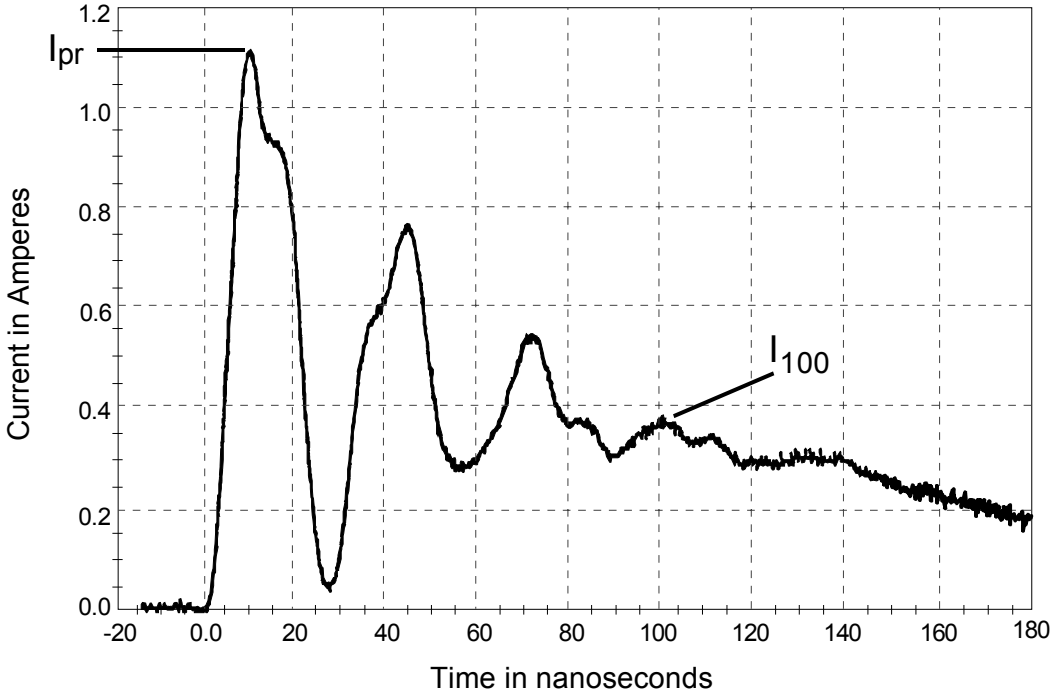


Figure 3: MM Current Waveform through a 500 Ohm Resistor *, 400 volt discharge

*** The 500 ohm load is used only during Equipment Qualification as specified in section 2.3.**

3. TEST PROCEDURE:

3.1 Sample Size:

Each sample group shall be composed of ten (10) components per stress voltage level (for a total sample size of 30 components as specified in Table 1 of AEC - Q101). Each sample group shall be stressed at one (1) stress voltage level, following the test flow diagram of Figure 4, using all pin and/or terminal combinations specified in section 3.2. Each stress voltage level requires a new sample group of ten (10) components.

3.2 Pin and/or Terminal Combinations:

Each pair of pins and/or terminals and all combinations of pin and/or terminal pairs for each component shall be subjected to three (3) pulses at each stress voltage polarity following the ESD levels stated in Figure 4. Any pin and/or terminal not under test shall be in an electrically open (floating) state.

3.3 Test Temperature:

Each component shall be subjected to ESD pulses at room temperature.

3.4 Measurements:

Prior to ESD testing, complete parametric testing (initial electrical verification) shall be performed on all sample groups and all components in each sample group per applicable user device specification at room temperature followed by hot temperature, unless specified otherwise in the user device specification. A data log of each component shall be made listing all parameter measurements as defined in Table 2. The data log will be compared to the parameters measured during final electrical verification testing to determine the failure criteria of section 4.

3.5 Detailed Procedure:

The ESD testing procedure shall be per section 3.2, Figure 4, and as follows:

a. Follow the recommended test flow diagram of Figure 4.

b Connect a selected PUT (see section 3.2) to terminal B.

c. Connect an individual component pin and/or terminal to terminal A. Leave all other component pins and/or terminals unconnected.

d. Apply one (1) positive pulse at the specified voltage to the PUT. Wait a minimum of one (1) second before applying the next test pulse. The use of three (3) pulses at each stress voltage polarity is required.

e. Apply one (1) negative pulse at the specified voltage to the PUT. Wait a minimum of one (1) second before applying the next test pulse. The use of three (3) pulses at each stress voltage polarity is required.

f. Disconnect the PUT from testing and connect the next individual component pin and/or terminal to terminal A. Leave all other component pins and/or terminals unconnected.

g. Repeat steps (d) through (f) until every pin and/or terminal not connected to terminal B is pulsed at the specified voltage (see section 3.2).

h. Repeat steps (b) through (g) until all pin and/or terminal combinations have been stressed.

i. Test the next component in the sample group and repeat steps (b) through (h) until all components in the sample group have been tested at the specified voltage level.

j. Submit the components for complete parametric testing (final electrical verification) per the user device specification at room temperature followed by hot temperature, unless specified otherwise in the user device specification, and determine whether the components meet the failure criteria requirements specified in section 4. It is permitted to perform the parametric testing (final electrical verification) per user device specification after all sample groups have been tested.

k. Using a new sample group, select the next stress voltage level as specified in Figure 4 and repeat steps (b) through (j)

l. Repeat steps (b) through (k) until failure occurs or the maximum withstanding voltage level has been reached.

4. FAILURE CRITERIA:

A component will be defined as a failure if, after exposure to ESD pulses, the component fails any of the following criteria:

1. The component exceeds the allowable shift values for the specific key parameters listed in Table 2. Other component parameters and allowable shift values may be specified in the user device specification. During initial parametric testing, a data log shall be made for each component listing the applicable parameter measurement values. This data log will be compared to the parameters measured during final parametric testing to determine the shift value. Components exceeding the allowable shift value will be defined as a failure.

2. The component no longer meets the user device specification requirements. Complete parametric testing (initial and final electrical verification) shall be performed per applicable user device specification at room temperature followed by hot temperature, unless specified otherwise in the user device specification.

Table 2: Key Parameters and Allowable Shift Values

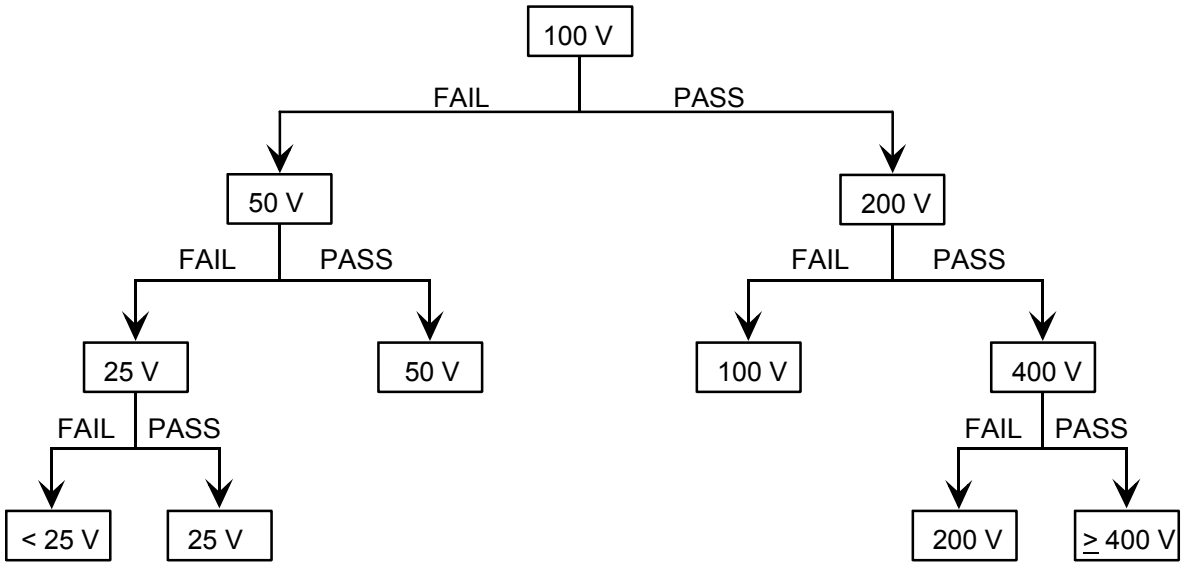
Component Type	Parameters	Maximum Allowable Shift Values
Bipolar	I_{CES}, I_{CBO}, and I_{EBO}	Ten times (10X) the initial measurement
FET	I_{DSS} and I_{GSS}	Ten times (10X) the initial measurement
IGBT	I_{CES} and I_{GES}	Ten times (10X) the initial measurement
Diode	I_R	Ten times (10X) the initial measurement

5. ACCEPTANCE CRITERIA:

A component passes a voltage level if all components stressed at that voltage level and below pass. All the samples must meet the measurement requirements specified in section 3. and the failure criteria requirements specified in section 4. Using the classification levels specified in Table 3, classify the components according to the highest ESD voltage level survived during ESD testing. The ESD withstanding voltage shall be defined for each component by the supplier.

Table 3: Discrete Component MM ESD Classification Levels

Component Classification	Maximum Withstand Voltage
M0	≤ 25 V
M1A	> 25 V to ≤ 50 V
M1B	> 50 V to ≤ 100 V
M2	> 100 V to ≤ 200 V
M3	> 200 V to ≤ 400 V
M4	> 400 V



Note 1: Classify the components according to the highest ESD voltage level survived during ESD testing.

Figure 4: Discrete Component MM ESD Test Flow Diagram

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Revision History

Rev #	Date of change	Brief summary listing affected sections
-	Apr. 24, 1996	Initial Release.
A	July 18, 2005	Revised the following: Sections 1.2, 2.1, 3.1, and 5; Tables 1 and 3; Figures 1 and 3.

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ATTACHMENT 3

AEC - Q101-003 Rev-A

WIRE BOND SHEAR TEST

Automotive Electronics Council

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Automotive Electronics Council
Component Technical Committee

METHOD - 003

DISCRETE COMPONENT
WIRE BOND SHEAR TEST

1. SCOPE:

1.1 Description:

This test establishes a procedure for determining the strength of the interface between a gold ball bond and a die bonding surface, or an aluminum wedge/stich bond and a die or package bonding surface, on either pre-encapsulation or post-encapsulation components. This strength measurement is extremely important in determining two features:

1) the integrity of the metallurgical bond which has been formed.

2) the reliability of gold and aluminum wire bonds to die or package bonding surfaces.

This test method can be used only when the ball height and diameter for ball bonds, or the wire height (1.25 mil and larger at the compressed bond area) for wedge/stitch bonds, are large enough and adjacent interfering structures are far enough away to allow suitable placement and clearance (e.g., above the bonding surface and between adjacent bonds) when performing the wire bond shear test.

The wire bond shear test is destructive. It is appropriate for use in process development, process monitoring, and/or quality assurance.

1.2 Reference Documents:

Not Applicable

1.3 Terms and Definitions:

The terms and definitions shall be in accordance with the following sections.

1.3.1 Ball Bond:

The welding of a thin wire, usually gold, to a die bonding surface, usually an aluminum alloy bond pad, using a thermal compression or thermosonic wire bonding process. The ball bond includes the enlarged spherical portion of the wire (sometimes referred to as the nail head and formed by the flame-off and first bonding operation in thermal compression and thermosonic process),the underlying bonding surface, and the intermetallic weld interface. For the purposes of this document, all references to ball bonds are applicable to gold ball bonds on die bonding surfaces; other ball bond material combinations may require a new set of failure criteria (see section 4.1).

1.3.2 Bonding Surface:

Either 1) the die surface (e.g., die bond pad) or 2) the package bonding surface (e.g., plated leadframe post or finger, downbond to the flag or paddle, etc.) to which the wire is ball, wedge, or stitch bonded.

1.3.3 Bond Shear:

A process in which an instrument uses a chisel shaped tool to shear or push a ball or wedge/stitch bond off the bonding surface (see Figure 1). The force required to cause this separation is recorded and is referred to as the bond shear strength. The bond shear strength of a gold ball bond, when correlated to the diameter of the ball bond, is an indicator of the quality of the metallurgical bond between the gold ball bond and the die bonding surface metallization. The bond shear strength of an aluminum wedge/stitch bond, when compared to the manufacturer's bond wire tensile strength, is an indicator of the integrity of the weld between the aluminum wire and the die or package bonding surface.

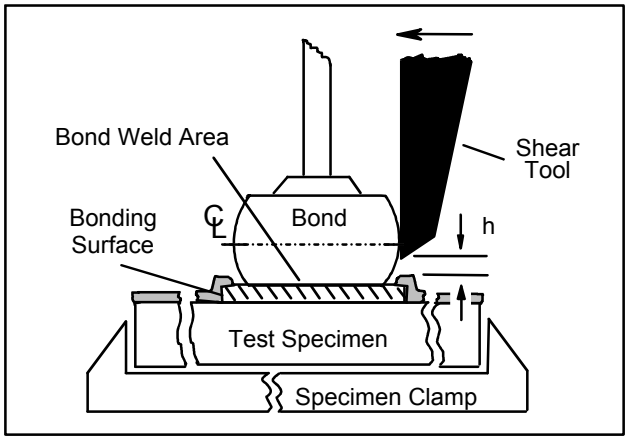


Figure 1: Bond Shear Set-up

1.3.4 Definition of Bond Shear Types for Ball and Wedge/Stitch Bonds (see Figure 3):

1.3.4.1 Type 1 - Bond Lift:

A separation of the entire wire bond from the bonding surface with only an imprint being left on the bonding surface. There is very little evidence of intermetallic formation or welding to the bonding surface metallization.

1.3.4.2 Type 2 - Bond Shear:

A separation of the wire bond where: 1) A thin layer of bonding surface metallization remains with the wire bond and an impression is left in the bonding surface, or 2) Intermetallics remain on the bonding surface and with the wire bond, or 3) A major portion of the wire bond remains on the bonding surface.

1.3.4.3 Type 3 - Cratering:

A condition under the bonding surface metallization in which the insulating layer (oxide or interlayer dielectric) and the bulk material (silicon) separate or chip out. Separation interfaces which show pits or depressions in the insulating layer (not extending into the bulk) are not considered craters. It should be noted that cratering can be caused by several factors including the wire bonding operation, the post-bonding processing, and even the act of wire bond shear testing itself. Cratering present prior to the shear test operation is unacceptable.

1.3.4.4 Type 4 - Die Surface Contact:

The shear tool contacts the die surface and produces an invalid shear value. This condition may be due to improper placement of the specimen, a die surface not parallel to the shearing plane, a low shear height, or instrument malfunction. This bond shear type is not acceptable and shall be eliminated from the shear data.

1.3.4.5 Type 5 - Shearing Skip:

The shear tool removes only the topmost portion of the ball or wedge/stich bond. This condition may be due to improper placement of the specimen, a die surface not parallel to the shearing plane, a high shear height, or instrument malfunction. This bond shear type is not acceptable and shall be eliminated from the shear data.

1.3.4.6 Type 6 - Bonding Surface Lift:

A separation between the bonding surface metallization and the underlying substrate or bulk material. There is evidence of bonding surface metallization remaining attached to the ball or wedge/stich bond.

1.3.5 Footprint:

An impression of the compressed wedge/stitch bond area created in the bonding surface during the ultrasonic wire bonding process. The bond footprint area is normally larger than the actual metallurgical weld interface.

1.3.6 Shear Tool or Arm:

A tungsten carbide, or equivalent, chisel with specific angles on the bottom and back of the tool to insure a shearing action.

1.3.7 Wedge/Stitch Bond:

The welding of a thin wire, usually aluminum, to a die or package bonding surface using an ultrasonic wire bonding process. The wedge bond, sometimes referred to as a stitch bond, includes the compressed (ultrasonically bonded) area of the bond wire and the underlying bonding surface. When wedge/stitch bonding to an aluminum alloy bonding surface, no intermetallic exists because the two materials are of the same composition; but rather the two materials are combined and recrystallized by the ultrasonic energy of the welding process. For the purposes of this document, all references to wedge/stich bonds are applicable to aluminum wedge/stich bonds only; gold wedge/stich bonds are not required to be wire bond shear tested.

2. APPARATUS AND MATERIAL:

The apparatus and materials required for wire bond shear testing shall be as follows:

2.1 Inspection Equipment:

An optical microscope system or scanning electron microscope providing a minimum of 70X magnification.

2.2 Measurement Equipment:

An optical microscope or measurement system capable of measuring the wire bond diameter to within ± 0.1 mil.

2.3 Workholder:

Fixture used to hold the component being tested parallel to the shearing plane and perpendicular to the shear tool. The fixture shall also eliminate component movement during wire bond shear testing. If using a caliper controlled workholder, place the holder so that the shear motion is against the positive stop of the caliper. This is to insure that the recoil movement of the caliper controlled workholder does not influence the wire bond shear test.

2.4 Wire Bond Shear Equipment:

The wire bond shear equipment must be capable of precision placement of the shear tool approximately 0.1 mil above the topmost part of the bonding surface. This distance (h) shall insure the shear tool does not contact the die or package bonding surface and shall be less than the distance from the topmost part of the bonding surface to the center line (C_L) of the ball or wedge/stich bond.

2.5 Bond Shear Tool:

Required shear tool parameters include but are not limited to: flat shear face, sharp shearing edge, and shearing width of 1.5 to 2 times (1.5X to 2X) the bond diameter or bond length. The shear tool should be designed so as to prevent plowing and drag during wire bond shear testing. The shear tool should be clean and free of chips (or other defects) that may interfere with the wire bond shear test.

3. PROCEDURE:

3.1 Calibration:

Before performing the wire bond shear test, it must be determined that the equipment has been calibrated in accordance with the manufacturer's specifications and is presently in calibration. Recalibration is required if the equipment is moved to another location.

3.2 Visual Examination of Wire Bonds to be Shear Tested After Decapsulation:

Before performing wire bond shear testing on a component which has been opened using wet chemical and/or dry etch techniques, the bonding surfaces shall be examined to insure there is no absence of metallization on the bonding surface area due to chemical etching and wire bonds are attached to the bonding surface. Ball or wedge/stitch bonds on bonding surfaces with evidence of degradation from chemical attack or absence of metallization shall not be used for wire bond shear testing. Wire bonds on bonding surfaces without degradation from chemical attack may not be attached to the bonding surface due to other causes (e.g., package stress). These wire bonds are considered valid and shall be included in the shear data as a zero (0) gram value. Wire bonds must also be examined to ensure adjacent interfering structures are far enough away to allow suitable placement and clearance (above the bonding surface and between adjacent wire bonds) when performing the wire bond shear test.

3.3 Sample Sizes:

The sample size shall be as specified in Table 1 of CDF-AEC-Q101.

3.4 Measurement of the Ball Bond Diameter to Determine the Ball Bond Failure Criteria:

Once the bonding surfaces have been examined and prior to performing wire bond shear testing, the diameter of all ball bonds (from at least one representative sample to be tested) shall be measured and recorded. For asymmetrical ball bonds, determine the average using both the largest (d_{large}) and the smallest diameter (d_{small}) values (see Figure 2). These ball bond diameter measurements shall be used to determine the mean, or average, diameter value. The resulting mean, or average, ball bond diameter shall then be used to establish the failure criteria as defined in section 4.1. If process-monitor data has established the nominal ball bond diameter, then that value may be used to determine the failure criteria as defined in section 4.1.

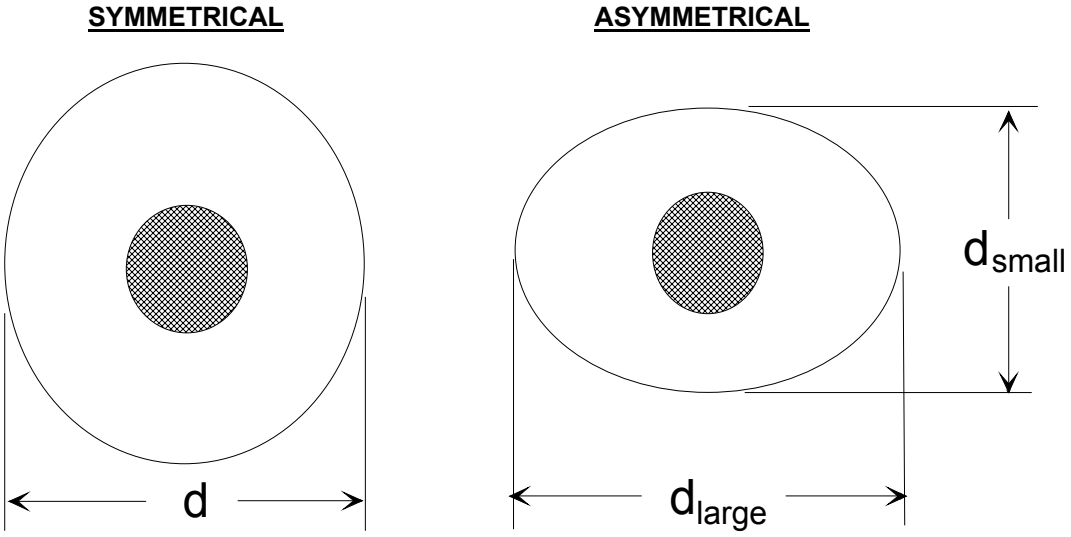


Figure 2: Ball Bond Diameter Measurement (symmetrical vs. asymmetrical)

3.5 Wire Bond Shear Test Procedure:

The wire bond shear testing procedure shall be performed as follows:

a. The wire bond shear equipment shall pass all self diagnostic tests prior to performing the wire bond shear test.

b. The wire bond shear equipment and test area shall be free of excessive vibration or movement. Examine the shear tool to verify it is in good condition and is not bent or damaged. Check the shear tool to verify it is in the up position.

c. Adjust the workholder to match the component being tested. Secure the component to the workholder. Make sure the die or package bonding surface is parallel to the shearing plane of the shear tool. It is important that the shear tool does not contact the bonding surface or adjacent structures during the shearing operation as this will give incorrect high readings.

d. Position the component so that the wire bond to be tested is located adjacent to the shear tool. Lower the shear tool (or raise the component depending upon wire bond shear equipment used) to approximately the die or package bonding surface but not contacting the surface (approximately the thickness of the wire bond above the die or package bonding surface).

e. For ball bond shear testing, position the ball bond to be tested so that the shear motion will travel perpendicular to the die edge. Wire bond shear testing is required for ball bonds located at the die bonding surface interface only.

f. For aluminum wedge/stitch bond shear testing, a wire height at the compressed bond area of 1.25 mils and larger is required. For wires too small for wire bond shear testing (less than 1.25 mils in height at the compressed bond area), only a footprint inspection is required (see section 3.7). Position the wedge/stitch bond to be tested so that the shear motion will travel toward the long side of the wedge/stitch bond and is free of any interference (i.e. shear the outside wedge/stitch bond first and then shear toward the previously sheared wedge/stitch bond). Wire bond shear testing is required for aluminum wedge/stitch bonds located at die and package bonding surfaces; gold wedge/stich bonds are not required to be wire bond shear tested.

g. Position the shear tool a distance of approximately one ball bond diameter (or one aluminum wire diameter for wedge/stitch bonds) from the wire bond to be shear tested and shear the wire bond.

3.6 Examination of Sheared Wire Bonds:

All wire bonds shall be sheared in a planned/defined sequence so that later visual examination can determine which shear values should be eliminated due to an improper shear. The wire bonds shall be examined using at least 70X magnification to determine if the shear tool skipped over the wire bond (type 5) or the shear tool scraped or plowed into the die surface (type 4). See Figure 3 for bond shear types and illustrations.

Readings in which either a bond shear type 4 or 5 defective shear condition occurred shall be eliminated from the shear data. Bond shear type 1, 2, 3, and 6 shall be considered acceptable and included in the shear data.

Sheared wire bonds in which a bond shear type 3 cratering condition has occurred shall be investigated further to determine whether the cracking and/or cratering is due to the wire bonding process or the act of wire bond shear testing. Cratering caused prior to the wire bond shear test operation is unacceptable. Cratering resulting from the act of wire bond shear testing shall be considered acceptable and included in the shear data.

3.7 Footprint Inspection of Aluminum Wedge/Stitch Bonds:

a. All aluminum wire bonding processes to both die and package bonding surfaces shall have a bond footprint inspection performed.

b. For wires too small for wire bond shear testing (less than 1.25 mils in height at the compressed bond area), the wires shall be removed at the wedge/stitch bond location using a small sharp blade to peel or pluck the wire bond from the bonding surface. The removal of the aluminum wire shall be sufficient such that the wire bond interface can be visually inspected and the metallurgical wire bond area determined.

c. For larger wires (greater than 1.25 mils in height at the compressed bond area), the wires shall be inspected after wire bond shear testing to examine the failure mode and to determine the wedge/stitch bond footprint coverage.

3.8 Bond Shear Data:

Data shall be maintained for each wire bond sheared. The data shall identify the wire bond (location, ball bond and/or wire diameter, wire material, method of bonding, and material bonded to), the shear strength, and the bond shear type (as defined in section 1.3.4 and Figure 3).

4. FAILURE CRITERIA:

The following failure criteria are not valid for components that have undergone environmental stress testing or have been desoldered from circuit boards.

4.1 Failure Criteria for Gold Ball Bonds:

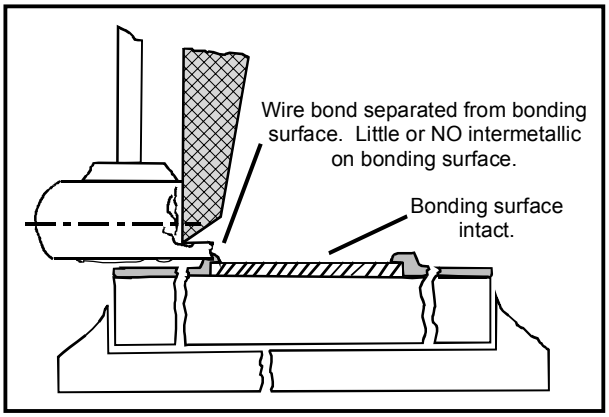
The gold ball bonds on a component shall be considered acceptable if the minimum individual and sample average ball bond shear values are greater than or equal to the values specified in Figure 4 and Table 1. This criteria is applicable for gold wire ball bonds on aluminum alloy bonding surfaces. Other material combinations may require a new set of failure criteria.

Alternate minimum ball bond shear values may be proposed by the supplier if supporting data justifies the proposed minimum values.

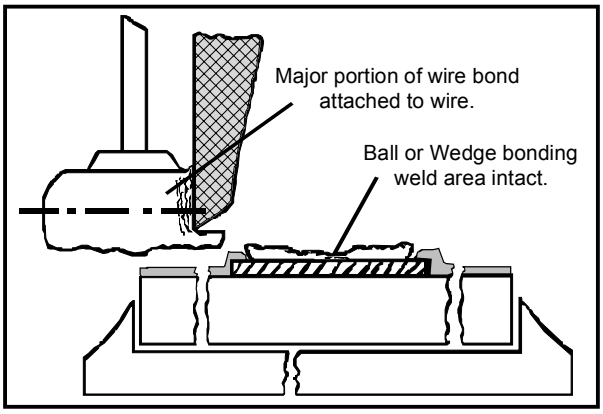
4.2 Failure Criteria for Wedge/Stitch Bonds:

The aluminum wedge/stitch bonds on a component shall be considered acceptable if the minimum shear values are greater than or equal to the manufacturer's bond wire tensile strength.

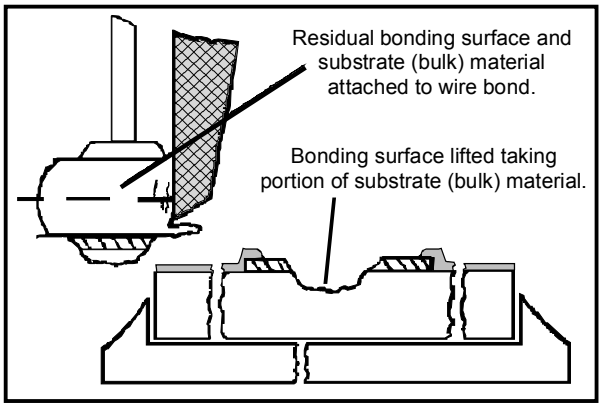
In addition, the percent of the wedge/stitch bond footprint in which bonding occurs shall be greater than or equal to 50%. If it is necessary to control the wire bonding process using SPC for percent coverage, a C_{pk} value can be calculated to this limit.



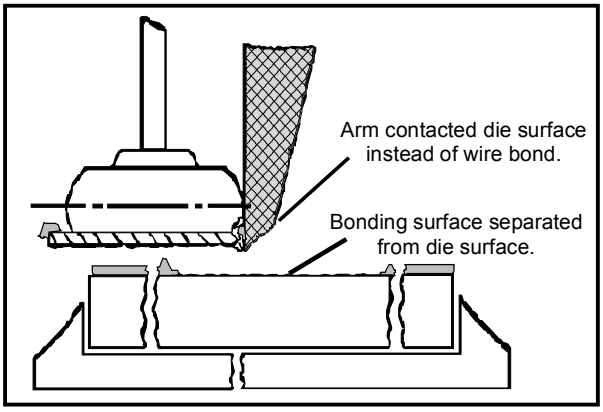
TYPE 1: Bond Lift



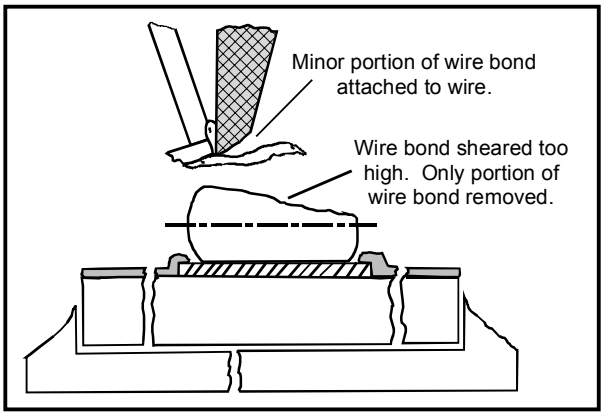
TYPE 2: Bond Shear - Gold/Aluminum



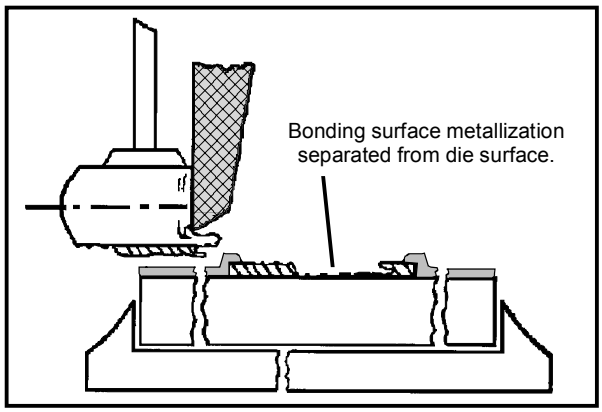
TYPE 3: Cratering



TYPE 4: Die Surface Contact



TYPE 5: Shearing Skip



TYPE 6: Bonding Surface Lift

Figure 3: Wire Bond Shear Types *

*** (Shear types are illustrated using ball bonds; these types also apply to wedge/stitch bonds)**

MINIMUM SHEAR VALUES

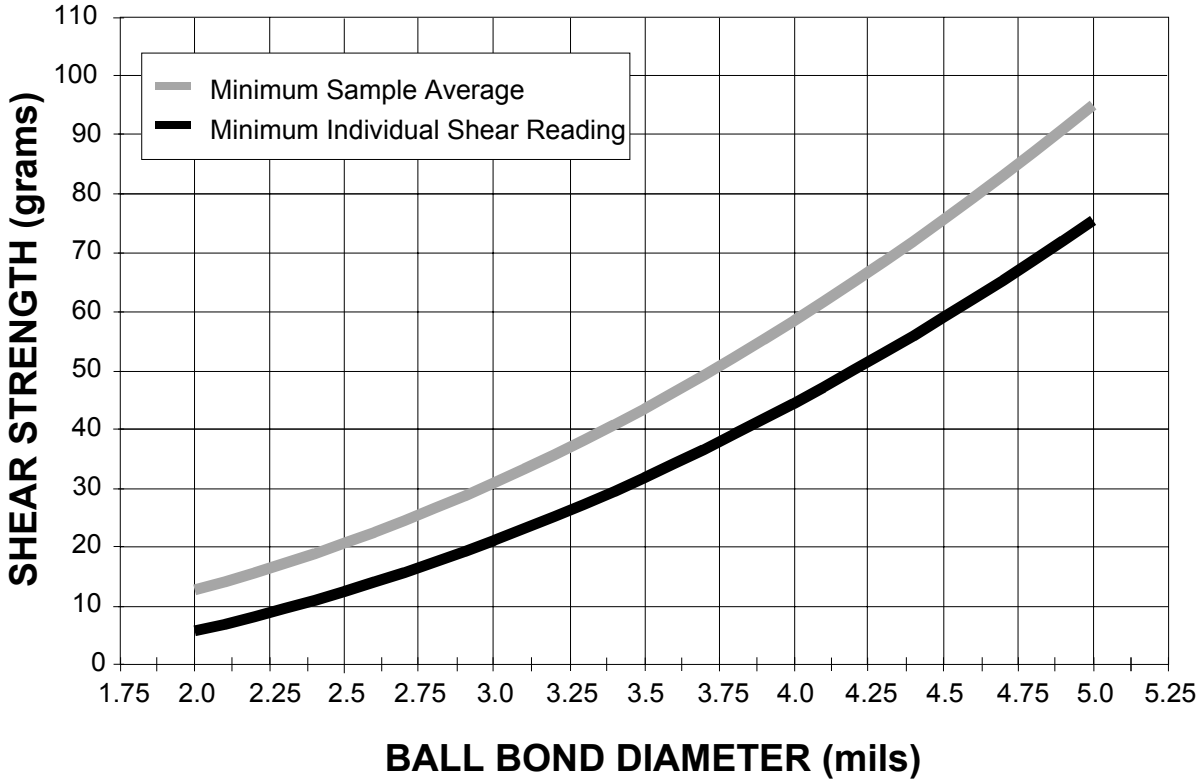


Figure 4: Minimum Acceptable Individual and Sample Average Ball Bond Shear Values *, see Table 1 for exact ball bond shear values *

*** (Shear values are applicable for gold wire ball bonds on aluminum alloy bonding surfaces)**

Table 1: Minimum Acceptable Individual and Sample Average Ball Bond Shear Values *

*** (Shear values are applicable for gold wire ball bonds on aluminum alloy bonding surfaces)**

Ball Bond Diameter (mils)	Minimum Sample Average (grams)	Minimum Individual Shear Reading (grams)
2.0	12.6	5.7
2.1	14.0	6.8
2.2	15.5	8.1
2.3	17.1	9.5
2.4	18.8	10.9
2.5	20.6	12.4
2.6	22.4	14.0
2.7	24.4	15.6
2.8	26.5	17.4
2.9	28.6	19.2
3.0	30.8	21.1
3.1	33.2	23.1
3.2	35.6	25.1
3.3	38.1	27.2
3.4	40.7	29.4
3.5	43.4	31.7
3.6	46.2	34.1
3.7	49.1	36.5
3.8	52.1	39.1
3.9	55.2	41.7
4.0	58.3	44.3
4.1	61.6	47.1
4.2	65.0	50.0
4.3	68.4	52.9
4.4	71.9	55.8
4.5	75.6	59.0
4.6	79.3	62.1
4.7	83.1	65.3
4.8	87.0	68.6
4.9	91.0	72.0
5.0	95.1	75.5

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Revision History

Rev #	Date of change	Brief summary listing affected sections
-	May 15, 1996	Initial Release.
A	July 18, 2005	Added new Section 1.3.5. Revised the following: Sections 1.1, 1.3.1, 1.3.4.1, 1.3.4.4, 1.3.4.5, 2.2, 2.5, 3.2, 3.5, 3.6 (b); Figure 3.

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ATTACHMENT 4

AEC - Q101-004 Rev-

MISCELLANEOUS TEST METHODS

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METHOD - 004

MISCELLANEOUS TEST METHODS

1. SCOPE

1.1 Description:

This document establishes the procedure and criteria for performing miscellaneous qualification tests referred to in Table 2 (Process Change Guidelines for the Selection of Tests) of AEC-Q101. The tests described in this document are:

Section 2 - Unclamped Inductive Switching (UIS)
Section 3 - Dielectric Integrity (DI)
Section 4 - Destructive Physical Analysis (DPA)

2. UNCLAMPED INDUCTIVE SWITCHING (UIS):

2.1 Description:

This test is used to determine the capability of a power MOSFET or IGBT to dissipate energy stored in an inductive load. Power MOSFETs have a parasitic back diode that is subjected to the energy stored in the inductor when the device is turned off, if no external clamp is provided. This test can also be used to determine ruggedness of IGBTs with a clamp incorporated within the package. Data generated by this test will be used to compare the ruggedness of power devices before and after various supplier initiated process changes. This is considered a destructive test. Devices subjected to the test shall not be shipped as production material.

2.2 Equipment:

The following equipment is required to conduct the test:

a. Oscilloscope with probes to measure drain current and voltage.
b. Inductors capable of handling the current range of interest without saturating.
c. Power supply capable of supplying the required voltage and current.
d. Pulse generator (to drive the gate).

2.3 Supplier Defined Variables:

a. Drain Current (I_D)
b. Gate Voltage (V_{GS})
c. Rated Breakdown Voltage ($V_{(BR)DSS}$)
d. Supply Voltage (V_{DD})
e. Time in Avalanche (t_{AV})
f. Inductance (L)

2.4 UIS Test Procedure:

2.4.1 The DUT is connected to the test fixture as shown in Figure 1.

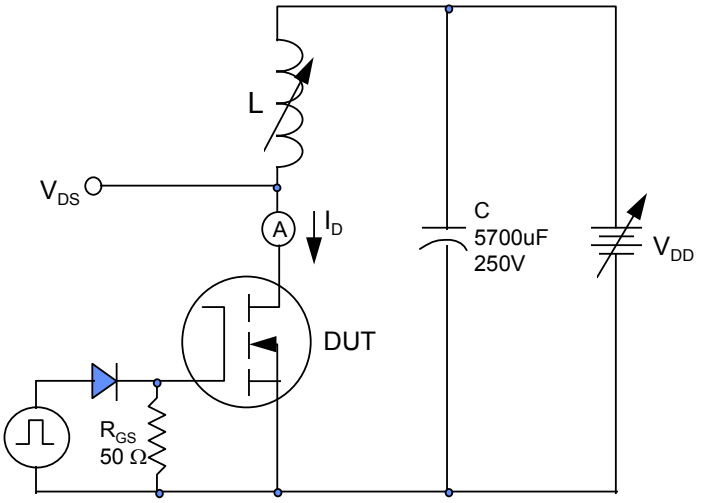

Figure 1: UIS Test Circuit

2.4.2 The Gate of the DUT is connected to a pulse generator to provide a single pulse with the signal level at the maximum rated gate to source voltage.

2.4.3 The gate is turned on allowing current to ramp in the inductor to the pre-determined value (see Figure 2).

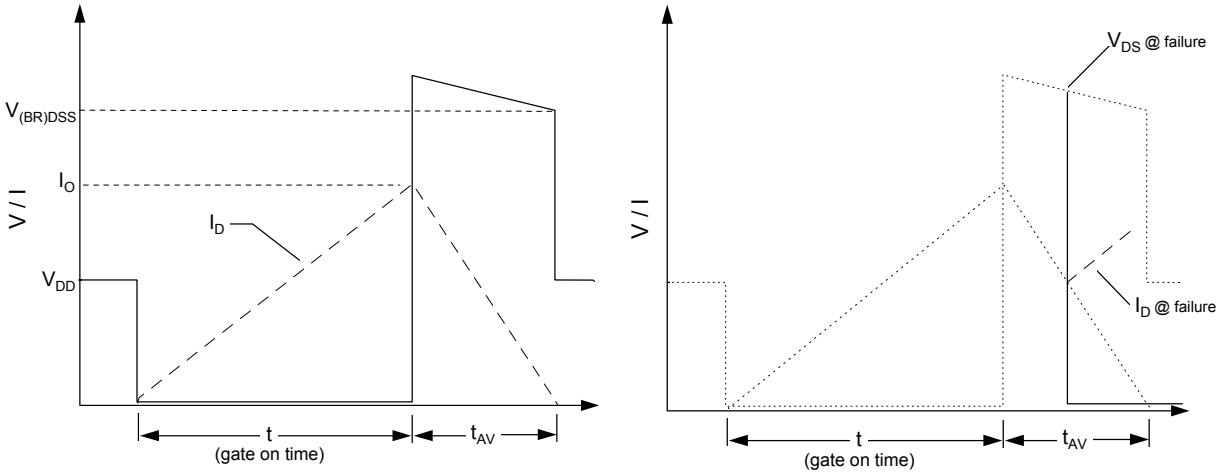

Figure 2: UIS Test Waveforms

2.4.4 When the pre-determined current value is reached, the gate is turned off, and the drain voltage and current is monitored (voltage & current) with an oscilloscope during reverse blocking to insure that the back diode clamps until the inductor energy is dissipated.

2.4.5 Increase the current in maximum 1 amp increments until failure. A failure is indicated by a collapse of the blocking voltage before the inductor energy is dissipated **OR** the presence of current flow after the inductor energy has dissipated (indicating latch-up).

2.4.6 Record I_{AV} & V_{DS} at the point where failure occurs. Capability is expressed as a function of the time in avalanche and current. Time in avalanche can be calculated using the formula:

$$t_{AV} = \frac{L * I_{AV}}{V_{DS\ @\ failure} - V_{DD}}$$

3. DIELECTRIC INTEGRITY (DI):

3.1 Description:

This test is used to determine the dielectric strength of the gate oxide of a power MOSFET or other MOS gated device. Data generated by this test will be used to compare the ruggedness of power devices before and after various supplier initiated process changes. This is considered a destructive test. Devices subjected to the test shall not be shipped as production material.

3.2 Equipment:

The following equipment is required to conduct the test:

a. Voltage controlled power supply
b. Sensitive current measurement instrument

3.3 Dielectric Integrity Test Procedure:

a. The DUT is connected to the test equipment as shown in Figure 3.

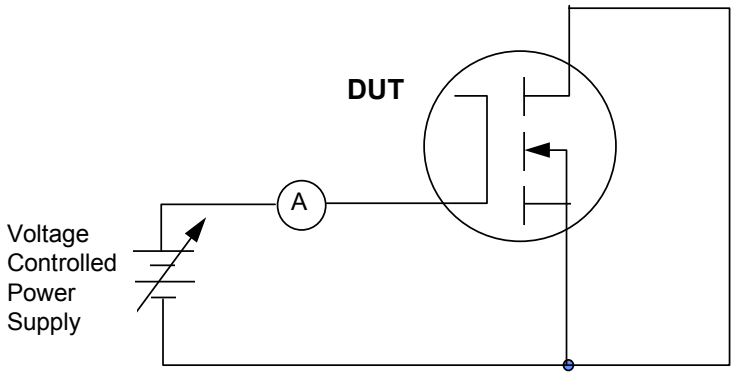

Figure 3: Dielectric Integrity Test Circuit

b. The voltage is increased in maximum 1 volt increments while the gate current is monitored.

c. Dielectric strength is defined as the gate voltage reading previous to which the gate current increases by an order of magnitude (from the previous reading).

d. Record and report this voltage and current for each DUT.

4. DESTRUCTIVE PHYSICAL ANALYSIS (DPA):

4.1 Description:

The purpose of this examination is to determine the capability of a device's internal materials, design, and workmanship to withstand forces induced by various stresses induced during environmental testing.

4.2 Equipment:

a. Optical microscope having magnification capability of up to 50X
b. De-capsulation equipment

4.3 Procedure:

a. Parts selected for this test must have successfully completed environmental testing as defined in Table 2 (Process Change Guidelines for the Selection of Tests) of AEC-Q101.

b. The parts shall be opened or de-capsulated in order to expose the internal die/substrate and determine the extent of any mechanical damage. The process used to de-capsulate the device must insure that it does not cause degradation of the leads and bonds. The internal die or substrate must be completely exposed and free of packaging material.

c. The devices shall be examined under a magnification of up to 50X to the criteria listed in section 4.4, herein.

d. Failed devices shall be analyzed to determine the cause of the failure. A Failure Analysis Report documenting this analysis shall be prepared on all failures. If the analysis shows that the failure was caused by the package opening process, the test shall be repeated on a second group of parts.

4.4 Failure Criteria:

Devices shall be considered failed if they exhibit any of the following:

a. Visible evidence of non-conforming to the devices' Certificate of Design, Construction and Qualification.
b. Visible evidence of corrosion, contamination, delamination or metallization voids.
c. Visible evidence of die/substrate cracks or defects (e.g. scratches, glassivation, etc.).
d. Visible evidence of wire, die, or termination bond defects.
e. Visible evidence of dendrite growth or electromigration.

Automotive Electronics Council
Component Technical Committee

Revision History

Rev #	Date of change	Brief summary listing affected sections
-	May 15, 1996	Initial Release.

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ATTACHMENT 5

AEC - Q101-005 Rev-

CAPACITIVE DISCHARGE MODEL (CDM) ELECTROSTATIC DISCHARGE (ESD) TEST

Automotive Electronics Council
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METHOD - 005

DISCRETE COMPONENT
CHARGED DEVICE MODEL (CDM)
ELECTROSTATIC DISCHARGE (ESD) TEST

1. SCOPE

1.1 Description:

The purpose of this specification is to establish a reliable and repeatable procedure for determining the CDM ESD sensitivity for electronic components. This test method does not include socketed CDM.

1.2 Reference Documents:

ESD Association Specification STM5.3.1
JEDEC Specification EIA/JESD22-C101

1.3 Terms and Definitions:

The terms used in this specification are defined as follows.

1.3.1 Charged Device Model (CDM) ESD:

An ESD pulse meeting the waveform criteria specified in this test method, approximating an ESD event that occurs when a component becomes charged (e.g., triboelectric) and discharges to a conductive object or surface.

1.3.2 Component Failure:

A condition in which a component does not meet all the requirements of the acceptance criteria, as specified in section 5, following the ESD test.

1.3.3 Device Under Test (DUT):

An electronic component being evaluated for its sensitivity to ESD.

1.3.4 Electrostatic Discharge (ESD):

The transfer of electrostatic charge between bodies at different electrostatic potentials.

1.3.5 Electrostatic Discharge Sensitivity:

An ESD voltage level resulting in component failure.

1.3.6 ESD Simulator:

An instrument that simulates the charged device model ESD pulse as defined in this specification.

1.3.7 Pin Under Test (PUT):

The pin and/or terminal under test; this includes all component pins as well as all power supply and ground pins.

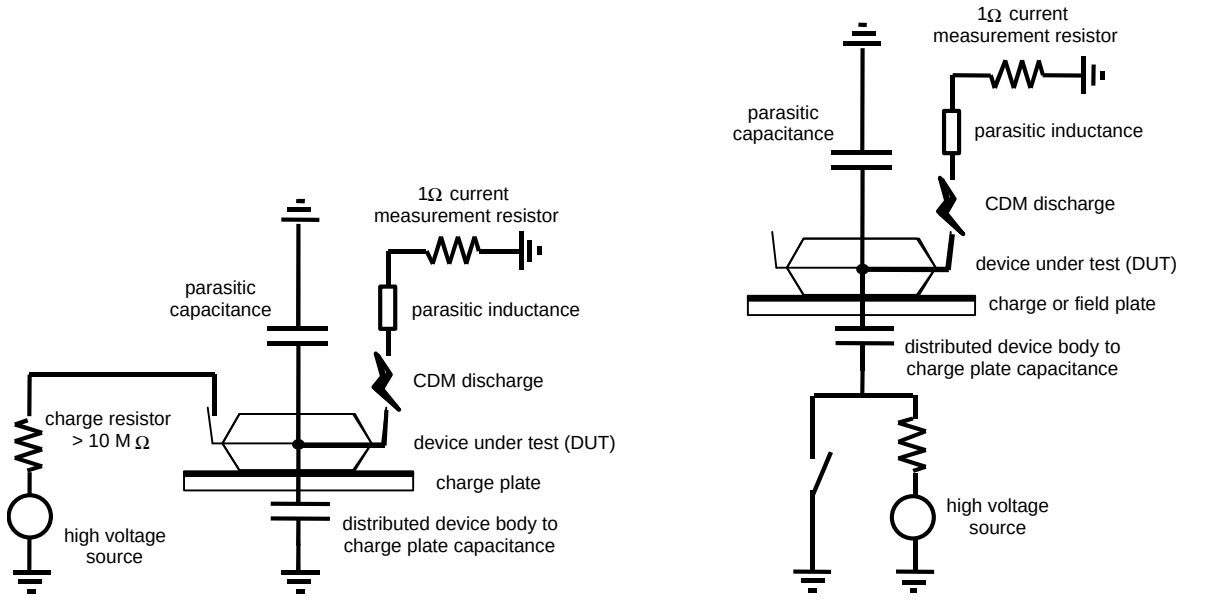
1.3.8 Withstanding Voltage:

The ESD voltage level at which, and below, the component is determined to pass the failure criteria requirements specified in section 4.

2. EQUIPMENT:

2.1 Test Apparatus:

The apparatus for this test consists of an ESD pulse simulator; Figure 1 shows a typical equivalent CDM ESD circuit. Other equivalent circuits may be used, but the actual simulator must be capable of supplying pulses that meet the waveform requirements of Table 2, Table 3, and Figure 3.



(a) Direct charge CDM **(b) Field induced charge CDM**

Note: Parasitics in the charge and discharge path of the test equipment can greatly affect test results

Figure 1: Charged Device Model ESD Typical Equivalent Circuit for (a) Direct Charge and (b) Field Induced Charge

2.2 Measurement Equipment:

Equipment shall include an oscilloscope/digitizer, current probe, attenuators, and cable/connector assemblies to verify conformance of the simulator output pulse to the requirements of this document as specified in Table 2, Table 3, and Figure 3.

2.2.1 Oscilloscope/Digitizer:

The oscilloscope/digitizer shall have a minimum bandwidth of 1.0GHz and nominal input impedance of 50Ω (Tektronix SCD1000, HP 7104, or equivalent).

2.2.2 Current Probe:

The current probe shall be an inductive current transducer or coaxial resistive probe with a minimum bandwidth of 5GHz.

2.2.3 Attenuator:

The attentuator, if required, shall be high precision (+0.1dB precision at 1.0GHz) with impedance of 50Ω.

2.2.4 Cable/Connector Assembly:

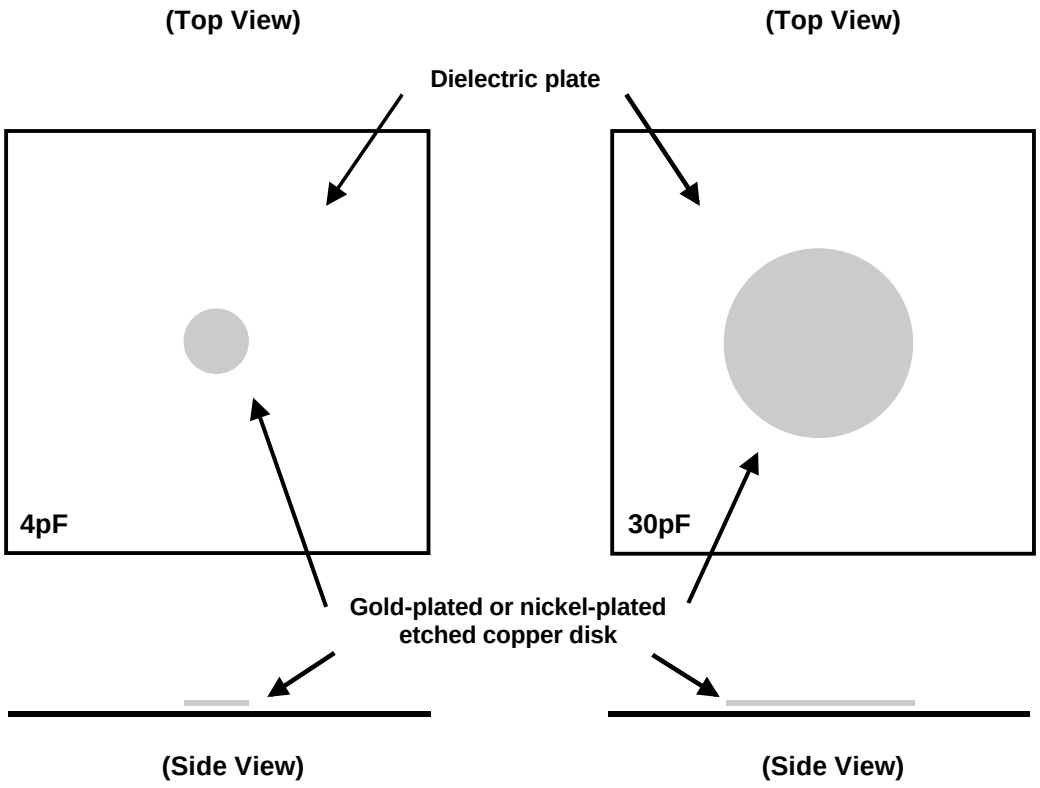
The cable/connector assembly, if required, shall be low loss (less than 0.4dB loss up to 1GHz) with impedance of 50Ω.

2.2.5 Verification Modules:

The two verification modules shall be gold-plated or nickel-plated etched copper disks on single sided FR-4 material (thickness = 0.8mm). The disks shall be: 1) a small disk (diameter approximately = 9 mm) configuration with a capacitance value of 4pF ±5% measured at 1MHz, and 2) a large disk (diameter approximately = 26mm) configuration with a capacitance of 30pF ±5% measured at 1MHz. Each disk shall be created using an etching process and centered on FR-4 material measuring at least 30mm by 30mm. Capacitance shall be measured with the non-metallized and non-disk side of the verification module in direct contact with the metal surface of a ground plane. Verification module parameters and illustrations are shown in Table 1 and Figure 2.

Table 1: Verification Module Parameters

Verification Module	Parameter	Accepted Value
4pF	Capacitance	3.8pF to 4.2pF
	Disk diameter	~ 9mm
	FR-4 material size	≥ 30mm by 30mm
	FR-4 thickness	0.8mm
30pF	Capacitance	28.5pF to 31.5pF
	Disk diameter	~ 26mm
	FR-4 material size	≥ 30mm by 30mm
	FR-4 thickness	0.8mm



(a) 4pF verification module (~ 9mm disk) **(b) 30pF verification module (~ 26mm disk)**

Figure 2: Verification Module Illustrations, (a) 4pF and (b) 30pF

2.2.6 Capacitance Meter:

The capacitance meter shall have a resolution of 0.2pF when measured at 1.0MHz with 3% accuracy.

2.3 Equipment Calibration and Qualification:

All peripheral equipment (including but not limited to the oscilloscope/digitizer, current probe, attenuators, cable/connector assemblies, verification modules, and capacitance meter) shall be periodically calibrated according to manufacturer's recommendations. A period of one (1) year is the maximum permissible time between full calibration tests. Qualification of the CDM simulator must be performed during initial acceptance testing or after repairs that are made to the equipment that may affect the waveform. The simulator must meet the requirements of Table 2 and Figure 3 for five (5) consecutive waveforms at all voltage levels using the 4pF verification module shown in Figure 2. Simulators not capable of producing the maximum voltage level shown in Table 2 shall be qualified to the highest voltage level possible. The simulator must also meet the requirements of Table 3 and Figure 3 for five (5) consecutive waveforms at the 500 volt level using the 30pF verification module shown in Figure 2. Thereafter, the test equipment shall be periodically qualified as described above; a period of one (1) year is the maximum permissible time between full qualification tests.

2.4 Verification Module Calibration:

The capacitance value of verification modules can be dramatically degraded by excessive use (indentations due to repetitive pogo pin contact, cracks in metallization, warping, etc.). Therefore, to ensure proper capacitance values, it is recommended that module capacitance be verified per section 2.4.1. When modules are degraded to the point they no longer meet the specified capacitance requirements shown in Table 1, they must be replaced.

2.4.1 Verification Module Capacitance Measurement Procedure:

a. Using the 4pF verification module, place the non-metallic side of the module in direct contact with the metallic surface of a ground plane. Capacitance measurements can be affected by air gaps between the module and the ground plane (e.g., due to warping of the FR-4 material, etc.). Therefore, the air space between the module and the ground plane must be minimized. This can be accomplished by applying slight pressure using the capacitance meter probes; care must be taken to avoid damaging the disk metallization.

b. Using the capacitance meter defined in section 2.2.6, measure the capacitance of the verification module to the ground plane. The capacitance value shall meet the requirements defined in Table 1.

c. Repeat steps (a) and (b) using the 30pF verification module.

2.5 Simulator Waveform Verification:

The performance of the simulator can be dramatically degraded by parasitics in the discharge path. Therefore, to ensure proper simulation and repeatable ESD results, it is recommended that waveform performance be verified using the 4pF verification module. The waveform verification shall be performed prior to performing CDM testing. If at any time the waveforms do not meet the requirements of Table 2 and Figure 3 at the 500 volt level, the testing shall be halted until waveforms are in compliance.

2.5.1 Waveform Verification Procedure:

a. Prior to performing waveform verification, verification modules and tester components (e.g., pogo pin, charge plate, etc.) must be cleaned with isoproponal (isopropyl alcohol) using a procedure approved by the user's internal safety organization. Once clean, avoid direct skin contact. If handling is required, the use of vacuum tweezers or personnel finger cots is strongly recommended.

b. Place the 4pF verification module in direct contact with the charge plate of the CDM simulator. If a dielectric film is used during component testing, it shall be less than 130 microns thick and must be in place during the waveform verification procedure.

c. Set the horizontal time scale of the oscilloscope at 0.5 nanoseconds per division or less.

d. Raise the charge plate potential to positive 500 volts. With the discharge pin centered within the 4pF metallic disk, bring the discharge pin in direct contact with the verification module and initiate a discharge.

e. Measure and record the rise time, first peak current, second peak current, third peak current, and full width at half height. All parameters must meet the limits specified in Table 2 and Figure 3.

f. Raise the charge plate potential to negative 500 volts. With the discharge pin centered within the 4pF metallic disk, bring the discharge pin in direct contact with the verification module and initiate a discharge.

g. Measure and record the rise time, first peak current, second peak current, third peak current, and full width at half height. All parameters must meet the limits specified in Table 2 and Figure 3.

Table 2: CDM Waveform Specification for 4pF Verification Module

Voltage Level (V)	1st peak current for 4pF I_{p1}(A) (±20%)	2nd peak current for 4pF I_{p2} (A)	3rd peak current for 4pF I_{p3} (A)	Rise Time t_r (ps)	Full width at half height for 4pF **FWHH** (ps)
250	2.25	< 50% of I_{p1}	< 25% of I_{p1}	< 400	< 600
500	4.50	< 50% of I_{p1}	< 25% of I_{p1}	< 400	< 600
1000	9.00	< 50% of I_{p1}	< 25% of I_{p1}	< 400	< 600
2000	18.00	< 50% of I_{p1}	< 25% of I_{p1}	< 400	< 600

Table 3: CDM Waveform Specification for 30pF Verification Module

Voltage Level (V)	1st peak current for 30pF * I_{p1} (A) (±20%)	2nd peak current for 30pF * I_{p2} (A)	3rd peak current for 30pF * I_{p3} (A)	Rise Time T_r for 30pF * (ps)	Full width at half height for 30pF * **FWHH** (ps)
500	14.00	< 50% of I_{p1}	< 25% of I_{p1}	< 400	< 1000

*** The 30pF verification module is used only during Equipment Qualification as specified in section 2.3.**

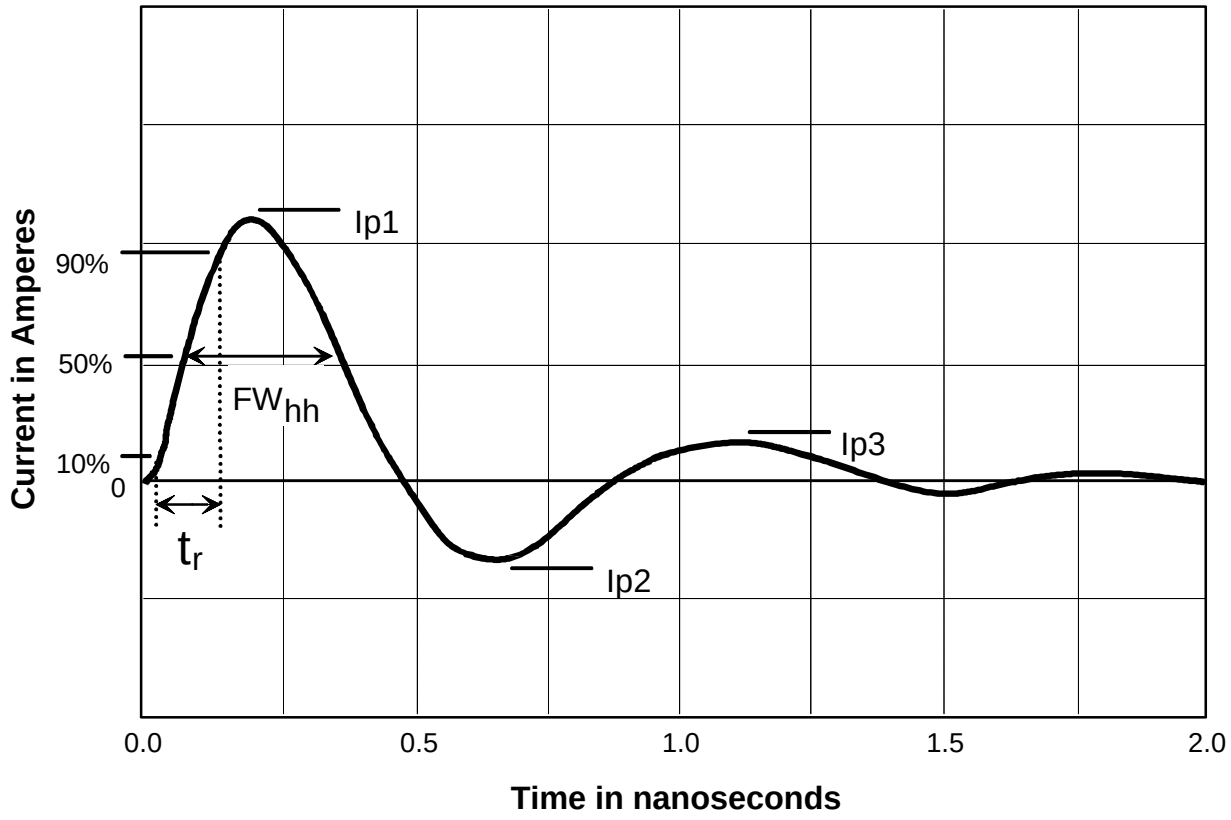


Figure 3: Typical CDM Current Waveform

3. PROCEDURE:

3.1 Sample Size:

Each sample group shall be composed of ten (10) components per stress voltage level. Each sample group shall have all component pins and/or terminals (including power and ground pins) stressed at one (1) voltage level, following the test flow diagram of Figure 4. Each stress voltage level requires a new sample group of ten (10) components.

3.2 Charging and Discharging Methods:

There are two acceptable methods of charging a DUT: Direct Charging and Field-induced Charging. Either method may be used to perform CDM ESD testing and must be recorded. While several methods exist for discharging a DUT, the direct contact discharge method is the only acceptable method to discharge a DUT for this test method.

3.2.1 Direct Charging Method:

The DUT is placed “dead-bug” (upside down with pins and/or terminals pointing up) with component body in direct contact with the charge plate and charged either through the pin(s) providing the best ohmic connection to the substrate of the DUT or through all DUT pins simultaneously (see Figure 1). To prevent damaging the DUT, ensure both the component and charging mechanism are at ground potential prior to initiating the CDM test. Contact to the charging pin(s) must be made prior to raising the charge potential. Once the DUT is charged, a pin under test (PUT) is discharged (except any pin(s) directly connected to the substrate of the

DUT). It is permissible to leave the charging probe in direct contact with the charging pin during the discharge event provided the discharge waveform meets the requirements of Table 2, Table 3, and Figure 3. After discharging the PUT, the DUT shall be re-charged and the process is repeated for each pin to be tested. All charge pins must be recorded.

3.2.2 Field-induced Charging Method:

The DUT is placed "dead-bug" (upside down with pins and/or terminals pointing up) with component body in direct contact with the field charging plate and charged by raising the potential of the charge plate (see Figure 1). To prevent damaging the DUT, ensure both the component and charge plate are at ground potential prior to initiating the CDM test. Once the DUT is charged, a pin under test (PUT) is discharged. After discharging the PUT, the DUT shall be re-charged and the process is repeated for each pin to be tested. The field charging plate shall be at least seven times (7X) larger in area than the DUT and shall meet the requirements of Table 2, Table 3, and Figure 3. If a dielectric film is used during component testing, it shall be less than 130 microns thick and must be in place during the waveform verification procedure.

3.2.3 Charging Small Components:

Small component packages may not be able to hold enough charge to meet the specified discharge voltage levels. For these packages, perform the test once and, if there is insufficient charge, the supplier must instead perform both HBM and MM ESD testing. The supplier shall document that the package could not hold sufficient charge to perform the CDM ESD test.

3.2.4 Direct Discharging Method:

Direct contact discharge is initiated within a relay and can add parasitics to the discharge path (care must be taken to minimize these parasitics). A discharge probe (e.g., pogo pin), connected to the relay, is placed in direct contact with the PUT and produces a very repeatable CDM event.

3.3 Test Temperature:

Each component shall be subjected to ESD pulses at room temperature.

3.4 Measurements:

Prior to ESD testing, complete parametric testing (initial electrical verification) shall be performed on all sample groups and all components in each sample group per applicable user device specification at room temperature followed by hot temperature, unless specified otherwise in the user device specification. A data log of each component shall be made listing all parameter measurements as defined in Table 4. The data log will be compared to the parameters measured during final electrical verification testing to determine the failure criteria of section 4.

3.5 Cleaning Method:

To avoid charge loss during CDM testing, components should be cleaned with isopropanol (isopropyl alcohol) using a procedure approved by the local safety organization. Components should then be handled only by vacuum tweezers, personnel wearing finger cots or equivalent, or plastic tweezers which have been neutralized by holding in an ionized air stream. The CDM tester should be cleaned periodically with isopropanol (isopropyl alcohol) to remove any surface contamination that could result in charge loss. Particular attention should be paid to the discharge probe, charging probe, and the charge plate on which the component is placed.

3.6 Detailed Procedure:

The ESD testing procedure shall be per the test flow diagram of Figure 4 and as follows:

a. Place clean DUT “dead-bug” (upside down with pins and/or terminals pointing up) with component body in direct contact with the charge plate.

b. Follow the recommended test flow diagram of Figure 4.

c. Select a charging method and charge the DUT to a positive potential.

d. Select a PUT and discharge the DUT. After discharging, wait a minimum of 1 second and re-charge the DUT. The use of three (3) discharges at each charge voltage polarity is required.

e. Set the charge voltage to a negative potential.

f. Repeat steps (c) through (d) using the same PUT.

g. Repeat steps (b) through (f) until every PUT (all component pins and/or terminals) is discharged at the specified voltage.

h. Test the next component in the sample group and repeat steps (a) through (g) until all components in the sample group have been tested at the specified voltage level.

i. Submit the components for complete parametric testing (final electrical verification) per the user device specification at room temperature followed by hot temperature, unless specified otherwise in the user device specification, and determine whether the components meet the failure criteria requirements specified in section 4. It is permitted to perform the parametric testing (final electrical verification) per user device specification after all sample groups have been tested.

j. Using the next sample group, select the next stress voltage level as specified in Figure 4 and repeat steps (a) through (i).

k. Repeat steps (a) through (j) until failure occurs or the component fails to meet the 125 volt stress voltage level.

4. FAILURE CRITERIA:

A component will be defined as a failure if, after exposure to ESD pulses, the component fails any of the following criteria:

1. The component exceeds the allowable shift values for the specific key parameters listed in Table 4. Other component parameters and allowable shift values may be specified in the user device specification. During initial parametric testing, a data log shall be made for each component listing the applicable parameter measurement values. This data log will be compared to the parameters measured during final parametric testing to determine the shift value. Components exceeding the allowable shift value will be defined as a failure.

2. The component no longer meets the user device specification requirements. Complete parametric testing (initial and final electrical verification) shall be performed per applicable user device specification at room temperature followed by hot temperature, unless specified otherwise in the user device specification.

Table 4: Key Parameters and Allowable Shift Values

Component Type	Parameters	Maximum Allowable Shift Values
Bipolar	I_{CES}, I_{CBO}, and I_{EBO}	Ten times (10X) the initial measurement
FET	I_{DSS} and I_{GSS}	Ten times (10X) the initial measurement
IGBT	I_{CES} and I_{GES}	Ten times (10X) the initial measurement
Diode	I_R	Ten times (10X) the initial measurement

5. ACCEPTANCE CRITERIA:

A component passes a voltage level if all components stressed at that voltage level and below pass. All the samples must meet the measurement requirements specified in section 3 and the failure criteria requirements specified in section 4. Using the classification levels specified in Table 5, the supplier shall classify the components according to the maximum withstanding voltage level. Due to the complex nature of the CDM event, a change in manufacturing process, design, materials, or component package may require reclassification according to this test method.

Table 5: Discrete Component CDM ESD Classification Levels

Component Classification	Maximum Withstand Voltage
C0	≤ 125 V
C1	> 125 V to ≤ 250 V
C2	> 250 V to ≤ 500 V
C3	> 500 V to ≤ 750 V
C4	> 750 V to ≤ 1000 V
C5	> 1000 V

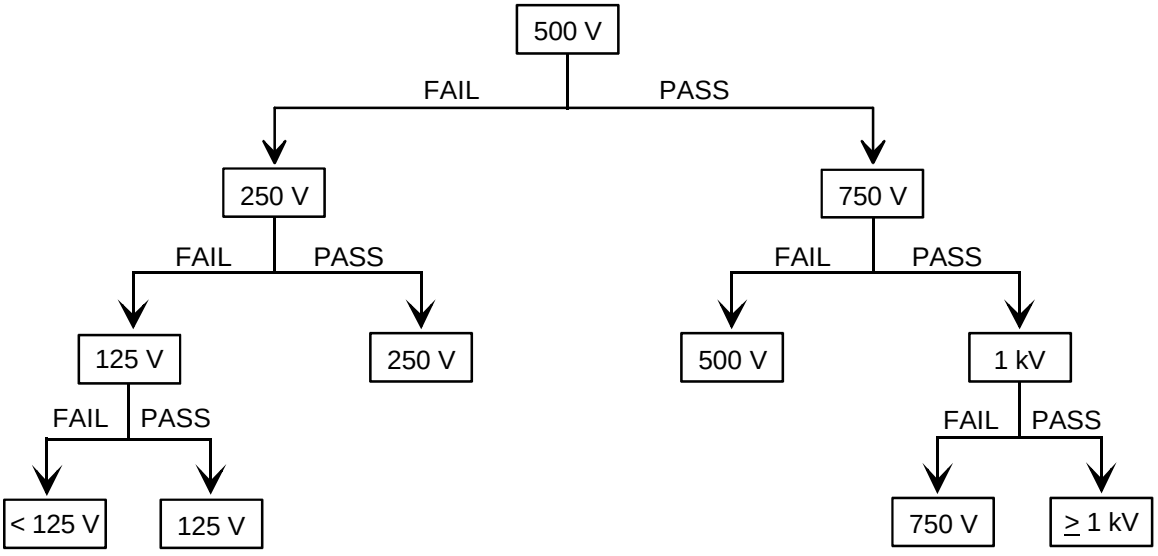


Figure 4: Discrete Component CDM ESD Test Flow Diagram

Automotive Electronics Council
Component Technical Committee

Revision History

Rev #	Date of change	Brief summary listing affected sections
-	July 18, 2005	Initial Release.