1200 V GaN Vertical Fin Power Field-Effect Transistors

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***Abstract*—**We demonstrate record performance in a novel normally-off GaN vertical transistor with submicron fin-shaped channels. This vertical fin transistor only needs n-GaN layers, with no requirement for epitaxial regrowth or p-GaN layers. A specific on-resistance of 0.2 mΩ·cm^2 and a breakdown voltage over 1200 V have been demonstrated with extremely high ON current (over 25 kA/cm^2) and low OFF current at 1200 V (below 10^{-4} A/cm^2), rendering an excellent Baliga's figure of merit up to 7.2 GW/cm^2. A threshold voltage of 1 V was achieved and was stable up to 150 °C. Large devices with high current up to 10 A and breakdown voltage over 800 V were also demonstrated. These results show the great potential of GaN vertical fin transistors for high-current and high-voltage power applications.

I. Introduction

Lateral and vertical GaN-based devices are excellent candidates for high-power electronics. Vertical GaN devices have several potential advantages over lateral devices: 1) higher breakdown voltage (*BV*) and current for a given chip area; 2) superior reliability and 3) easier thermal management [1]. Until now, two main structures have been demonstrated for vertical GaN power transistors: current-aperture vertical electron transistor (CAVET) [2-4] and trench MOSFET [5-6].

Despite the blocking capability over 1200 V demonstrated in GaN transistors, the development of vertical GaN power transistors has been hindered by the requirement for epitaxial regrowth or p-type GaN. The epitaxial regrowth (e.g. required for CAVETs) greatly increases the complexity and cost of device fabrication. P-type GaN (e.g. required for fabricating trench MOSFETs) has low ratio for the acceptor activation as well as much lower carrier mobility compared to that in n-GaN. It is also difficult to make normally-off CAVETs due to the polarization in AlGaN/GaN heterojuncitons. To overcome these challenges, our group recently demonstrated a novel device structure, the GaN vertical fin power field-effect transistor (FET) [6]. This transistor only needs n-GaN layers with no requirement for p-GaN or epitaxial regrowth. A *BV* of 800 V, an on-resistance (R_{on}) of 0.36 mΩ·cm^2 and normally-off operation have been demonstrated [6]. However, higher *BV* and current are needed to justify the competitiveness of this novel device for high power applications.

In this work, by improving wafer structure, electric field (E-field) engineering and Ohmic contact techniques, we successfully demonstrated a *BV* of 1200 V with an R_{on} of 0.2 mΩ·cm^2 in normally-off GaN vertical fin power FETs. Large devices with a current of 10 A were also demonstrated.

II. Device Design & Fabrication

In vertical fin power FETs (**Fig. 1**), the current is controlled through fin-shaped vertical n-GaN channels, which are surrounded by gate dielectrics and metal electrodes. At zero gate bias, the electrons in the fin channels are depleted due to the work function difference between the gate metal and GaN. By shrinking the fin width below 500 nm, the depletion regions induced by the two free surfaces of the fin merge, fully depleting the fin channel and inducing a normally-off transistor operation. At increased gate bias, the depletion width decreases and electrons accumulate at the dielectric-GaN interfaces, forming conduction channels.

The epitaxial structure consists of 0.3 μm-thick n$^+$-GaN cap layer, 7 μm-thick n$^-$-GaN drift layer and 2 μm-thick n-GaN layer, grown by MOCVD on free-standing GaN substrates (**Fig. 2**). The drift region was doped with carbon to compensate the non-intentional-doping in GaN (**Fig. 2**). A net donor concentration of ~3×10^{15} cm^{-3} was measured in the drift region, from the *C-V* measurement of vertical Schottky barrier diodes fabricated after removing the n$^+$-GaN cap layer (**Fig. 3**).

The device fabrication (**Fig. 4**) starts with the formation of the sub-micron fins aligned to *a*-plane by optimized Cl_2/BCl_3-based dry etching following a hot TMAH treatment for corner rounding [8]. A first oxide spacer was then deposited by PECVD and etched down to near the bottom fin corner. The oxide etching depth was controlled by a timed photoresist (PR) etch (**Fig. 4(a)**). An Al_2O_3 gate dielectric layer was then deposited by ALD followed by a sputtered Molybdenum gate layer. Then the gate metal and dielectrics were etched by the PR-assisted etching technique. A second oxide spacer was then deposited following a PR-assisted etch to expose top GaN surface. Before Ohmic metal deposition, a shallow cap layer recess was used to remove the highly-resistive layer induced by the plasma damage in previous steps and roughen the top GaN surface (**Fig. 4(c)**). This recess etch is key to make Ohmic contact to submicron-fins (**Fig. 4(d)**). Finally, Ti/Al metal stack was sputtered on the top/back side of the wafer for source/drain electrodes, with no need for post annealing. **Fig. 5** shows the cross-section scanning electron microscopy image of the fin region in the fabricated transistor.

III. Experimental Results

Fig. 6 shows the transfer characteristics of a GaN vertical fin FET consisting of 60 fins with 200 nm fin width and 100 μm fin length. The extracted threshold voltage (V_{th}) is ~1 V with almost no hysteresis. The I_{on}/I_{off} ratio is ~10^{10} with extremely low gate leakage current. **Fig. 7** shows the device output characteristics. A R_{on} of 0.2 mΩ·cm^2 was extracted normalized to the total active fin area. If normalized to the total device area, the R_{on} is ~1 mΩ·cm^2 and can be further reduced by shrinking the lateral distance between fins.

Fig. 8 plots the transfer curves and V_{th} of transistors with different fin width (W). A smaller W provides better gate control and smaller subthreshold swing. The V_{th} of our vertical fin transistor can be analytically estimated by [9]:

$$V_{th} \approx V_{bi} - qQ_{ox}/\epsilon_{ox} - qN_D W^2/8\epsilon_{GaN} \qquad (1)$$

The experimental V_{th} is lower than the V_{th} calculated by considering the barrier height (V_{bi}) and W. This indicates the existence of positive charges at Al_2O_3/GaN interfaces (Q_{ox}). This charge was also reported in GaN lateral transistors [10].

Fig. 9 shows the representative off-state characteristics of a GaN vertical fin FET consisting of 60 fins. A BV over 1200 V was demonstrated with extremely low drain and gate leakage current (<1 nA, close to measurement limit) at high drain bias. The breakdown was destructive and occured at the gate edge. This breakdown behavior can be well explained by the simulated E-field distribution at 1200 V (**Fig. 10**). As shown, the peak E-field happens at the gate edges instead of the bottom of the fins thanks to two key field engineering structures: (a) tapered-fin-bottom [8] with rounded corners, and (b) the oxide spacer layer between the gate electrode and fin corner, which forms a field-plate structure. Compared to the peak E-field at the fin corners, the peak E-field at the gate edge would be much easier to manage and can be further suppressed by adding additional gate and source field plates.

Fig. 11 shows the representative device transfer characteristics at 150 °C and 25 °C, respectively. As shown, a small V_{th} decrease (<0.15 V) was observed, demonstrating good thermal stability for normally-off operation.

Fig. 12 and **13** shows the demonstration of large-area GaN vertical fin power transistors with current rating of 10 A. The transistor consists of over 600 fins with a fin width of 250 nm in each fin. The total device size is 0.8 mm × 0.55 mm, which is significantly smaller than other 10 A-class GaN vertical and lateral transistors [5][11]. The gate drive for 10 A current is 5~6 V, which is smaller than that in vertical trench MOSFET (~10 V [5]). A BV over 800 V was demonstrated in these large-size GaN vertical fin power transistors.

Fig. 14 benchmarks the R_{on} *v.s.* BV for our GaN vertical fin power FETs with other normally-off lateral and vertical GaN transistors. With a BV of 1200 V and R_{on} of 0.2 mΩ·cm^2 (normalized to total fin area) or 1.0 mΩ·cm^2 (normalized to total device area), our device demonstrated a Baliga's figure of merit up to 7.2 GW/cm^2 (1.44 GW/cm^2 if normalized to total device area), which is among the best in all reported normally-off GaN transistors. The R_{on} of our vertical fin power FETs normalized to total device area can be further reduced by reducing the lateral distance between fins and increasing the fin aspect ratio, while the BV can be further improved by incorporating multiple gate and source field plates to smoothen the peak E-field at the gate edge.

Table I summarizes the key device metrics of our vertical fin power FETs, including R_{on}, BV, V_{th}, on-state drain-to-source saturation current density ($I_{ON, SAT}$), off-state leakage current density (I_{OFF}) at 1200 V and large device performance, benchmarked with other reported normally-off lateral and vertical transistors with high-current ratings. As shown, our vertical fin power FETs show the highest current density and the second lowest I_{OFF} at 1200 V. Considering the significant reduction in epitaxy cost and complexity compared to other vertical GaN transistors, our GaN vertical fin power FETs are highly competitive for 1200-V level high power applications.

IV. Conclusion

This work demonstrates a novel GaN vertical fin power FETs with a BV over 1200 V and a R_{on} of 0.2 mΩ·cm^2, as well as extremely high ON current density and low OFF current. This device can achieve normally-off operation, with a stable V_{th} up to 150 °C. In addition, this device can greatly reduce the epitaxy cost and complexity compared to other GaN vertical power transistors. This performance demonstrates the great potential of GaN vertical fin FETs for high-power applications.

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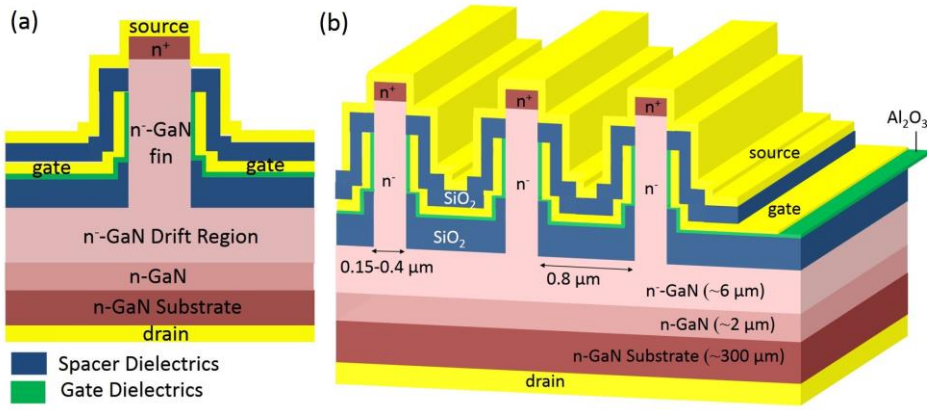

Fig. 1. (a) Cross-sectional schematic of a device fin unit-cell and (b) side-view three-dimensional schematic of the proposed vertical GaN fin power field-effect transistors (FETs) with multiple fins. The fin length is ~1μm in the vertical direction.

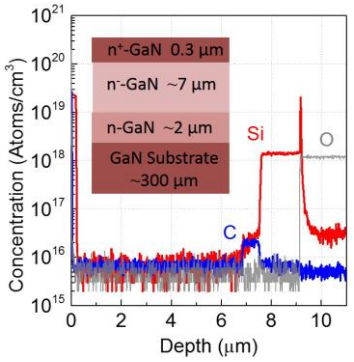

Fig. 2. GaN-on-GaN wafer epi-structure used in this work, and the Si, C and O ion profiles in the top layers of the wafer structure revealed by Secondary-ion mass spectrometry measurements.

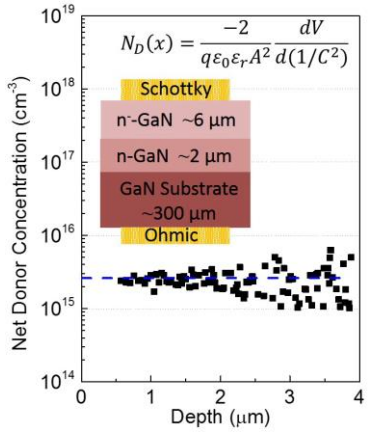

Fig. 3. Net donor concentration as a function of depth in n$^-$-GaN drift region, revealed by *C-V* measurement. (Inset I) Vertical Schottky barrier diodes fabricated for the *C-V* measurement. The top ~1 μm GaN layer was etched before the diode fabrication. (Inset II) Formula used for the donor concentration derivation from *C-V* measurement.

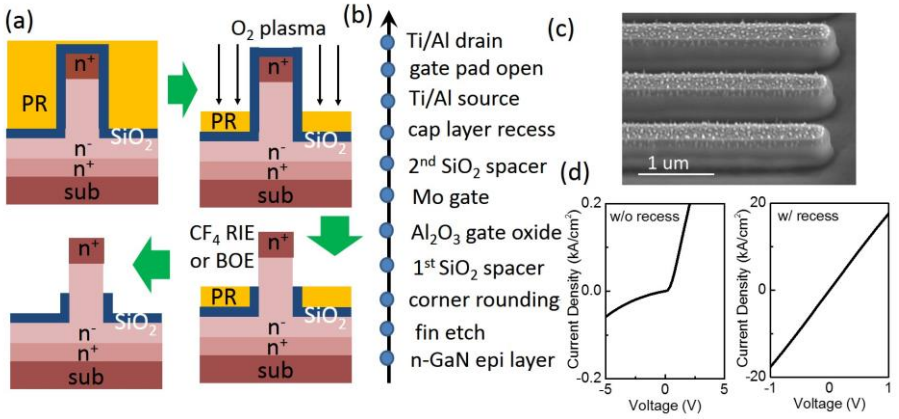

Fig. 4. (a) Illustrative process for the formation of first SiO_2 spacer in the fin structure, enabled by the timed etch and thickness control of the photoresist (PR) layer. (b) Key process steps to fabricate GaN vertical fin power FETs. (c) Scanning electron microscopy (SEM) images of the fins after the cap layer recess and surface roughening. (d) *I-V* characteristics of two Ohmic test structures, one with cap layer recess and the other without. The front and back sides of the Ohmic test structures are both covered by Ti/Al. The test device area is 100×25 μm^2. No post-deposition annealing was implemented for either structures.

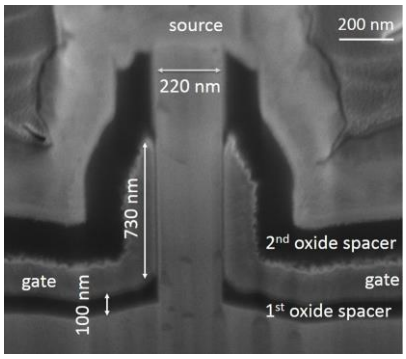

Fig. 5. SEM cross section view of the fin area in a fabricated GaN vertical fin power FET with ~220 nm channel width.

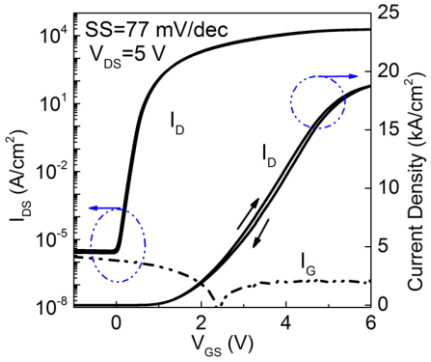

Fig. 6. Double-sweep transfer curves of the fabricated vertical fin power FET with 200 nm channel width, with the V_{DS} at 5 V. The left *y*-axis is in log scale with the right *y*-axis in linear scale. A threshold voltage of ~ 1 V can be extracted from linear extrapolation or defined at I_{on}/I_{off}=10^5.

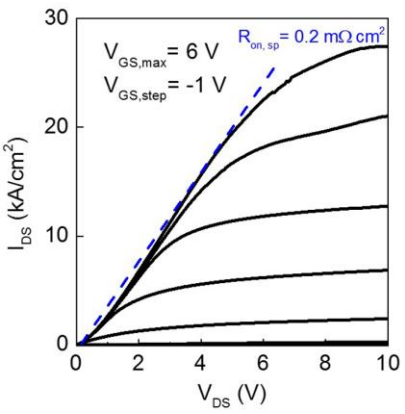

Fig. 7. Output characteristics of the fabricated fin power FET with channel width of 200 nm.

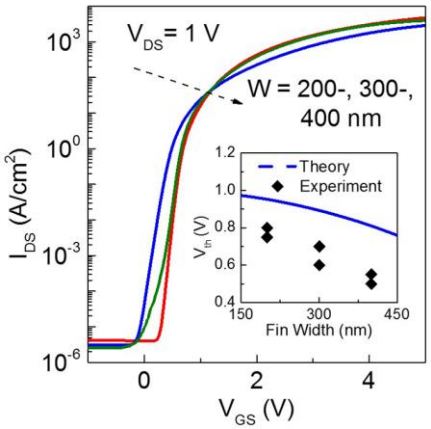

Fig. 8. Transfer curves of the fabricated GaN vertical fin power FETs with the fin widths of 200, 300 and 400 nm. (Inset) Threshold voltage (V_{th}) as a function of fin width from experiment and analytical calculation. The V_{th} was extracted at a current level of 1 A/cm^2.

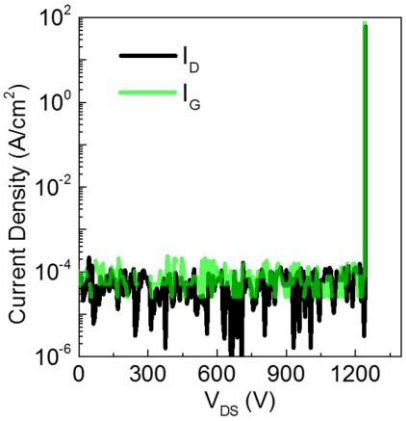

Fig. 9. Off-state *I-V* characteristics for drain and gate leakage in the fabricated GaN vertical fin power FET, at a V_{GS} of 0 V. The breakdown is destructive in the oxide spacer layer at the gate edge. The leakage current is noisy as it is close to the measurement limit.

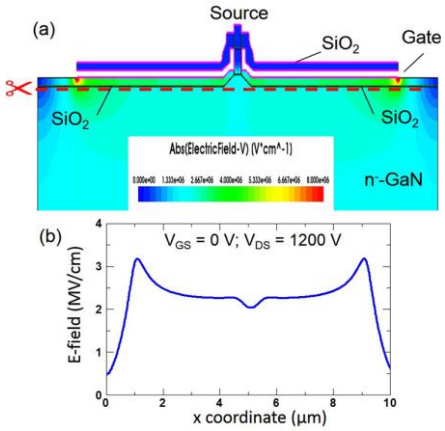

Fig. 10. (a) Simulated E-field distribution in the fin region when the vertical fin FET is biased at 1200 V in the off-state. (b) E-field distribution in GaN along the cutline shown in (a). The peak E-field is at the gate edge rather than near the fin bottom.

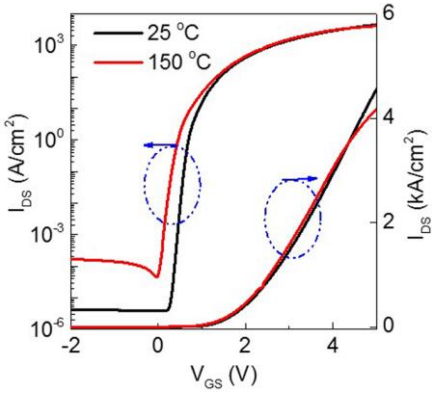

Fig. 11. Transfer curves of the fabricated vertical fin power FET with 200 nm channel width, at 25 ºC and 150 ºC. The left *y*-axis is in log scale with the right *y*-axis in linear scale. The drain bias is 1.5 V for this measurement.

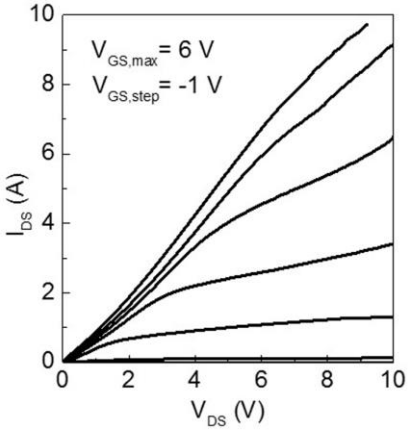

Fig. 12. Output characteristics of a 10 A large fin FETs. The device consists of over 600 fins with a channel width of ~250 nm in each fin.

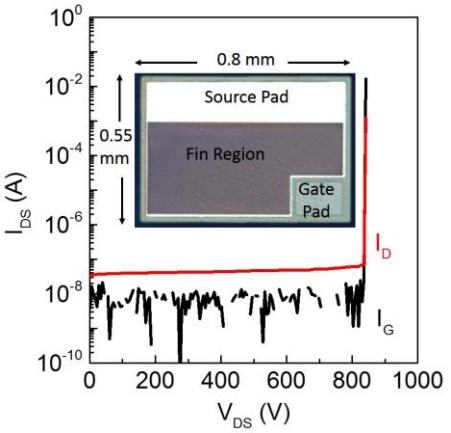

Fig. 13. Off-state *I-V* characteristics of a 10-A-level large fin FET, with a breakdown voltage over 800 V. (Inset) Photo of the fabricated large device consisting of over 600 fins.

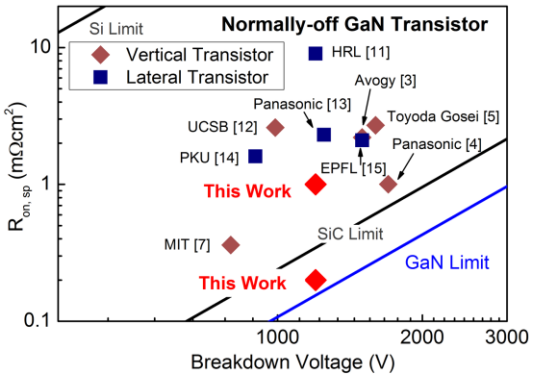

Fig. 14. Specific R_{on} *versus BV* of the GaN vertical fin power FET, benchmarked with other normally-off lateral and vertical GaN transistors. Top point of this work represents the R_{on} normalized with the total device area and the other point represents the R_{on} normalized with the total fin area.

TABLE I. Summary and benchmark of device structures and key device metrics for the GaN vertical and lateral transistors with high current ratings reported.

	Device Structure	R_{on} (mΩcm^2)	BV (V)	V_{th} (V)	$I_{ON, SAT}$ (A/cm^2)	I_{OFF} @1200 V (A/cm^2)	Large Device
V	**Fin FET (This work)**	**0.2 (1.0)**	**1200**	**1**	**25000**	**<10^{-4}**	**10 A / 800 V**
	CAVET [3]	2.2	1500	0.5	1500	0.02	2.3 A / 1400 V
	Trench CAVET [4]	1.0	1700	2.5	3500	0.01	15 A / 400 V
	Trench MOSFET [5]	2.7	1600	2	~1100	<10^{-8}	23.2 A / 1200 V
L	Gate Injector Transistor [13]	2.3	1250	3	0.4 A/mm	10^{-7} A/mm	10 A / 600 V
	Gate-recess HEMT [11]	9	1200	0.64	255	0.005	5.5 A / 1200 V

Note: 'V' represent 'Vertical' and 'L' represent 'Lateral'.