10

Optimization and Comparison of Power Devices

10.1 Blocking Voltage and Edge Terminations for SiC Power Devices

An essential requirement of all semiconductor power devices is the ability to withstand a large terminal voltage with minimal leakage current in the off state. The maximum terminal voltage a device can withstand is called the *blocking voltage*. The blocking voltage is generally determined by material properties as well as device design. The limiting mechanism may be any of the following: (i) punch-through of the base region in a MOSFET (metal-oxide-semiconductor field effect transistor), BJT (bipolar junction transistor), IGBT (insulated-gate bipolar transistor), or thyristor; (ii) avalanche breakdown in a reverse-biased pn or Schottky junction, either as a discrete rectifier or as a part of a switching transistor or thyristor; (iii) excessive leakage current in a reverse-biased pn or Schottky junction; or (iv) excessive electric field in the oxide of an MOS-based power device such as a MOSFET or IGBT.

Punch-through can be avoided by making the doping-thickness product of the base region large enough that the base cannot be completely depleted before the onset of avalanche breakdown. This requires

$$N \cdot W > \varepsilon_S E_C / q \tag{10.1}$$

where N and W represent the doping and width of the base region and E_C is the critical field for avalanche breakdown, to be discussed below. Since this restriction is typically observed for all power switching devices, punch-through will not be considered further.

In an MOS-based device such as a power MOSFET or IGBT, the blocking voltage is often limited by the oxide field. As discussed in Sections 8.2.6 and 8.2.11, the oxide field must be kept below about 4 MV cm^{-1} for long-term device reliability. Care must be exercised in the design of MOSFETs and IGBTs to make sure the oxide field does not exceed this value prior to avalanche breakdown of the blocking junction. This typically requires numerical simulations due to the two-dimensional nature of the fields, particularly in trench-gate or UMOS structures.

In well-designed devices, the blocking voltage is ultimately limited by avalanche breakdown of the reverse-biased blocking junction. The blocking voltage is reduced by two-dimensional field crowding at the edges of the device, which can be mitigated by the use of special edge terminations. In the sections below, we will first consider avalanche breakdown in planar SiC junctions using a one-dimensional analysis. We will then discuss two-dimensional field crowding and show how it can be minimized by different edge termination techniques.

Fundamentals of Silicon Carbide Technology: Growth, Characterization, Devices, and Applications, First Edition. Tsunenobu Kimoto and James A. Cooper.

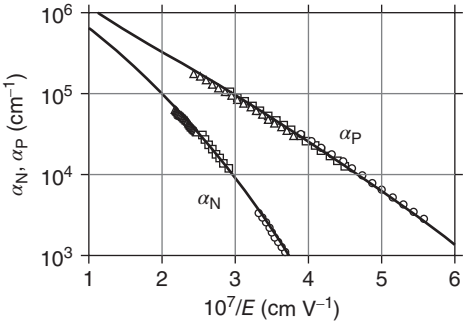


Figure 10.1 Ionization rate coefficients in 4H-SiC measured at room temperature ([1] reproduced with permission from AIP Publishing LLC).

10.1.1 Impact Ionization and Avalanche Breakdown

Avalanche breakdown is caused by the impact ionization of electrons and holes in a high-field region. The impact ionization process can be understood by considering the behavior of electrons and holes as they move through the crystal. As charged entities, electrons and holes are accelerated by the electric field, and their kinetic energy increases until they undergo a collision. The collision is a scattering event that takes the electron (or hole) into a lower energy state, with its energy typically transferred to the crystal lattice as heat. Immediately following the scattering event, the electron or hole is again accelerated, and the process is repeated as holes and electrons transit the high-field region. If the field is sufficiently high, the electron or hole may acquire enough kinetic energy between collisions that the energy liberated is sufficient to break a covalent bond, creating a new hole–electron pair. This process is called *impact ionization*.

The number of impact ionization events initiated by an electron (or hole) per unit length traveled is known as the *ionization rate for electrons* α_N or the *ionization rate for holes* α_P. α_N and α_P are strong functions of the electric field. Figure 10.1 shows the ionization rates for transport along the *c*-axis in 4H-SiC at room temperature, measured by Konstantinov *et al.* [1] This data can be represented by the empirical expressions [2]

$$\alpha_N(E) \approx 1.69 \times 10^6 \ (\text{cm}^{-1}) \exp\left[-\left(\frac{9.69 \times 10^6 \ (\text{V cm}^{-1})}{E}\right)^{1.6}\right] \tag{10.2}$$

and

$$\alpha_P(E) \approx 3.32 \times 10^6 (\text{cm}^{-1}) \exp\left[-\left(\frac{1.07 \times 10^7 \ (\text{V cm}^{-1})}{E}\right)^{1.1}\right] \tag{10.3}$$

Figure 10.2 compares the ionization rates for silicon and 4H-SiC. The ionization rates for 4H-SiC at a given field are orders-of-magnitude lower than for silicon.

Avalanche breakdown in 4H-SiC is typically initiated by holes, since the ionization rates are higher for holes than for electrons. Figure 10.3 shows the ionization rates for holes in 4H-SiC for several temperatures [3]. The lines represent the empirical equation

$$\alpha_P(E) \approx (6.09 \times 10^6 - 9.2310^3 T) \ (\text{cm}^{-1}) \exp\left[-\left(\frac{8.90 \times 10^6 - 4.95 \times 10^3 T}{E}\right)^{1.09}\right] \tag{10.4}$$

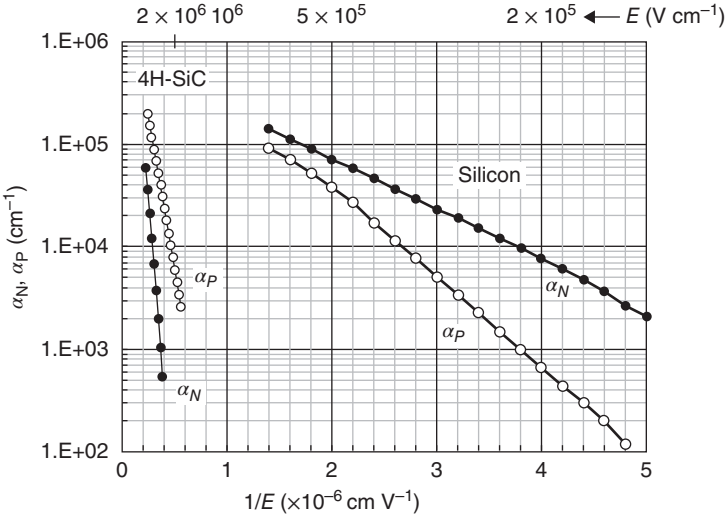


Figure 10.2 Comparison of ionization rates in silicon and 4H-SiC at room temperature. At a given field, the rates for SiC are orders-of-magnitude below those of silicon.

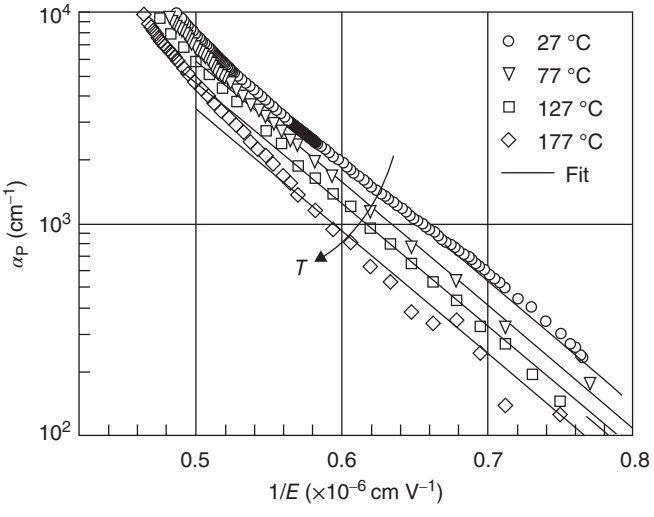


Figure 10.3 Temperature dependence of the hole ionization rate in 4H-SiC. The lines are generated using empirical Equation 10.4 ([3] reproduced with permission from Trans Tech Publications).

where T is the absolute temperature. The decrease in ionization rates with temperature occurs because of increased phonon scattering, making it less likely that a hole can acquire enough kinetic energy between collisions to create a hole–electron pair.

We will now apply the ionization rate expressions to calculate the breakdown voltage of a reverse-biased p + n one-sided step junction, such as shown in Figure 7.1. The depletion region extends

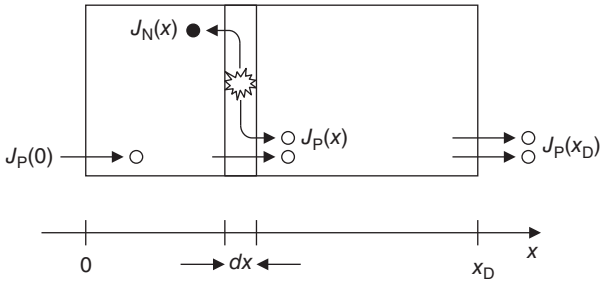


Figure 10.4 One-dimensional cross-section of a high-field region, illustrating generation of new electron–hole pairs by impact ionization.

from $x = 0$ to x_D and the electric field decreases from a peak value at $x = 0$ to zero at $x = x_D$. Any electrons and holes in the depletion region are subject to an electric field and can potentially initiate impact ionization events. Consider the cross-section of the depletion region shown in Figure 10.4. We assume hole current $J_P(0)$ is entering at $x = 0$ and hole current $J_P(x)$ is flowing at point x. Impact ionization in the differential slice at x creates additional holes and electrons, and the increase in hole current across the dx region is

$$dJ_P = \alpha_P J_P(x)dx + \alpha_N J_N(x)dx \tag{10.5}$$

which we can write as

$$\frac{dJ_P}{dx} = \alpha_P J_P(x) + \alpha_N J_N(x) \tag{10.6}$$

Since $J_P(x) + J_N(x) = J_{TOTAL}$ is not a function of x, we can write Equation 10.6 as

$$\frac{dJ_P}{dx} = (\alpha_P - \alpha_N)J_P(x) + \alpha_N J_{TOTAL} \tag{10.7}$$

Since α_P and α_N are functions of electric field and the electric field is a function of position, Equation 10.7 can be written in the form

$$\frac{df}{dx} = P(x)f(x) + Q(x) \tag{10.8}$$

where $f(x)$, $P(x)$, and $Q(x)$ are functions of x. The differential Equation 10.8 has the formal solution

$$f(x) = \frac{\displaystyle\int_0^x Q(x) \exp\left[-\int_0^x P\left(x'\right) dx'\right] dx + f(0)}{\displaystyle\exp\left[-\int_0^x P\left(x\right) dx\right]} \tag{10.9}$$

Substituting for $f(x)$, $P(x)$, and $Q(x)$ in Equation 10.9 yields

$$J_P(x) = \frac{\displaystyle\int_0^x \alpha_N(x) J_{TOTAL} \exp\left[\int_0^x \left(\alpha_N\left(x'\right) - \alpha_P(x')\right) dx'\right] dx + J_P(0)}{\displaystyle\exp\left[\int_0^x \left(\alpha_N\left(x\right) - \alpha_P(x)\right) dx\right]} \tag{10.10}$$

We define the *hole multiplication factor* M_P as the fractional increase in hole current across the depletion region due to impact ionization, $M_P = J_P(x_D)/J_P(0)$. Since we assumed no electron current at

$x = x_D, J_N(x_D) = 0$ and we can set $J_P(x_D) = J_{TOTAL}$. Under these assumptions, if we now evaluate Equation 10.10 at $x = x_D$ we can write

$$J_{TOTAL} = J_P(x_D) = J_{TOTAL} \frac{\displaystyle\int_0^{x_D} \alpha_N(x) \exp\left[\int_0^x \left(\alpha_N\left(x'\right) - \alpha_P(x')\right) dx'\right] dx + 1/M_P}{\displaystyle\exp\left[\int_0^{x_D} \left(\alpha_N(x) - \alpha_P(x)\right) dx\right]} \tag{10.11}$$

The complicated fraction on the right-hand side must be equal to 1, so M_P is given by

$$M_P = \frac{1}{\displaystyle\exp\left[\int_0^{x_D} \left(\alpha_N(x) - \alpha_P(x)\right) dx\right] - \int_0^{x_D} \alpha_N(x) \exp\left[\int_0^x \left(\alpha_N\left(x'\right) - \alpha_P(x')\right) dx'\right] dx} \tag{10.12}$$

The exponential factor in the second term in the denominator can be rewritten using the identity

$$\exp\left[\int_0^{x_D} g(x)\, dx\right] = \exp\left[\int_0^x g(x)\, dx\right] \exp\left[\int_x^{x_D} g(x)\, dx\right] \tag{10.13}$$

resulting in

$$\boxed{M_P = \frac{\displaystyle\exp\left[\int_0^{x_D} \left(\alpha_P(x) - \alpha_N(x)\right) dx\right]}{\displaystyle 1 - \int_0^{x_D} \alpha_N(x) \exp\left[\int_x^{x_D} \left(\alpha_P\left(x'\right) - \alpha_N(x')\right) dx'\right] dx}} \tag{10.14}$$

Avalanche breakdown occurs when the multiplication factor M_P goes to infinity, or when

$$\boxed{\int_0^{x_D} \alpha_N(x) \exp\left[\int_x^{x_D} \left(\alpha_P\left(x'\right) - \alpha_N(x')\right) dx'\right] dx \to 1} \tag{10.15}$$

Equation 10.15 is known as the *ionization integral for holes*. The above analysis could also have been conducted assuming only an electron current entering at $x = x_D$. In this case we would have defined an electron multiplication factor M_N, and avalanche breakdown would occur when M_N goes to infinity, or when

$$\boxed{\int_0^{x_D} \alpha_P(x) \exp\left[\int_0^x \left(\alpha_N\left(x'\right) - \alpha_P(x')\right) dx'\right] dx \to 1} \tag{10.16}$$

Considering that both holes and electrons are present in the device, avalanche breakdown will occur at the lowest voltage where either Equation 10.15 or 10.16 is satisfied.

It is customary to designate the peak field E_M at the onset of breakdown as the *critical field* for avalanche breakdown, E_C. E_C can be computed from the ionization integrals by an iterative procedure, as follows: For a given doping of the n− layer, select a value of reverse voltage and calculate the ionization integrals using Equations 10.15 and 10.16. If both integrals are less than 1, chose a slightly higher voltage and repeat the calculation. The lowest voltage for which either Equation 10.15 or 10.16 is satisfied is the breakdown voltage for that doping, and the peak field at the junction is the critical field for that doping. The critical field for a one-sided step junction in 4H-SiC at room temperature can be approximated using an empirical expression given by Konstantinov *et al.* [1],

$$\boxed{E_C \approx \frac{2.49 \times 10^6 V\,(\text{cm})}{1 - 0.25 \log_{10}(N\,(10^{16}\text{cm}^{-3}))}} \tag{10.17}$$

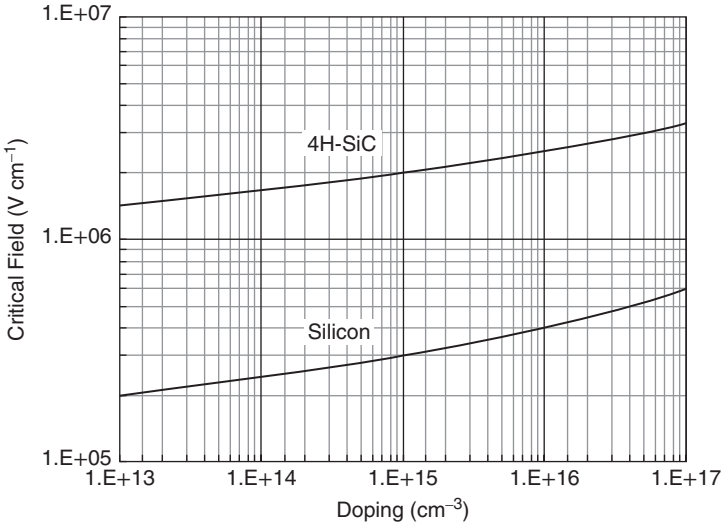


Figure 10.5 Critical field for room temperature avalanche breakdown in a 4H-SiC one-sided step junction, as given by Equation 10.17. Also shown for comparison is the critical field for silicon.

where N is the doping of the lightly-doped side of the junction. Figure 10.5 shows the critical field in silicon and 4H-SiC as a function of doping. The critical field is only a weak function of doping, and at doping levels below 10^{15} cm^{-3} the critical field in 4H-SiC is approximately seven times higher than in silicon. Since the power-device figure of merit scales inversely as the *cube* of critical field (see Section 7.1), this represents about a 350 × advantage for 4H-SiC.

As might be expected from the temperature dependence of the ionization rates, the avalanche breakdown voltage in 4H-SiC increases with temperature, as shown in Figure 10.6 [4]. A positive temperature

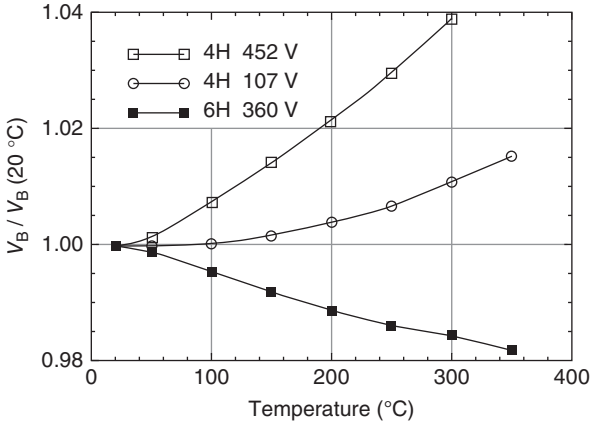


Figure 10.6 Temperature dependence of avalanche breakdown voltage in 4H and 6H-SiC. The temperature coefficient of breakdown is positive in 4H-SiC and negative in 6H-SiC ([4] reproduced with permission from AIP Publishing LLC).

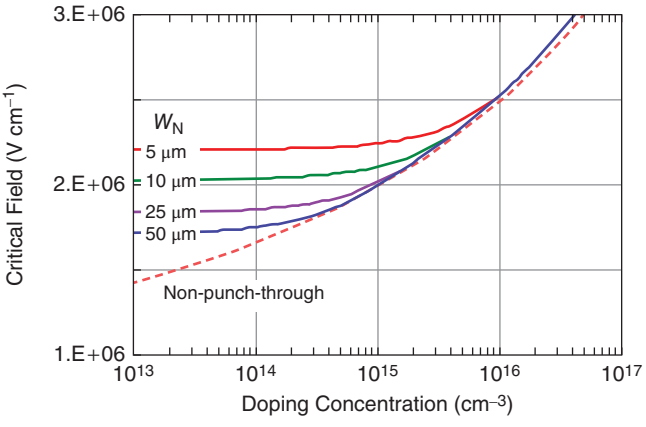


Figure 10.7 Critical field for room temperature avalanche breakdown in a 4H-SiC one-sided step junction with a punch-through structure. The critical field for a non-punch-through structure, given by Equation 10.17, is shown as a dashed line ([2] reproduced with permission from Dallas T. Morisette).

coefficient of breakdown is desirable, since devices with negative temperature coefficient of breakdown are potentially unstable.

It is important to recognize that the critical field in Equation 10.17 was calculated assuming a *non-punch-through* structure such as in Figure 7.1. In the *punch-through* structure of Figure 7.2, evaluation of the ionization integral yields a critical field that depends not only on doping, but also on the thickness of the lightly-doped region. Figure 10.7 shows the critical field in 4H-SiC calculated using the ionization integrals for both punch-through and non-punch-through structures [2]. The dashed line is the non-punch-through critical field given by Equation 10.17. In punch-through designs, the critical field for breakdown is higher than the value given by Equation 10.17.

10.1.2 Two-Dimensional Field Crowding and Junction Curvature

In most of our discussions to this point, we have considered only one-dimensional slices within our devices. This allows us to calculate carrier densities, current flows, and electrostatic potentials using one-dimensional analyses. In some cases this approach gives quantitatively accurate answers, but it often happens that the two-dimensional (or three-dimensional) nature of real devices necessitates a computer simulation. This is certainly true in the calculation of blocking voltage. The results in the preceding subsection were obtained using a one-dimensional analysis, but in real devices the blocking voltage is invariably limited by two-dimensional field crowding at the periphery of the device. Next, we will discuss how to evaluate the field crowding and consider techniques to mitigate it.

Consider the cylindrical p + /n− one-sided step junction illustrated in Figure 10.8. The p+ region has radius r_J and the depletion edge has radius r_D. Poisson's equation in cylindrical coordinates is

$$\frac{1}{r}\frac{\partial}{\partial r}\left(r\frac{\partial \psi}{\partial r}\right) = \frac{\rho}{\varepsilon_S} = -\frac{qN_D}{\varepsilon_S} \tag{10.18}$$

where r is the radial coordinate, $r_J \le r \le r_D$, and ρ is the charge per unit volume in the depletion region. Integration with respect to r yields

$$r\frac{\partial \psi}{\partial r} = -\frac{qN_D}{2\varepsilon_S}r^2 + C \tag{10.19}$$

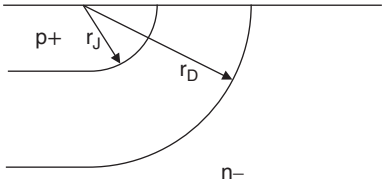


Figure 10.8 Cross-section of a p + /n− one-sided step junction with cylindrical geometry, such as occurs at the edges of real structures. r_J is the radius of the junction and r_D is the radius of the depletion region edge.

Noting that $\partial\psi/\partial r = -E(r)$ and choosing the constant of integration such that $E(r_D) = 0$, we can write

$$E(r) = \left(-\frac{qN_D}{2\varepsilon_S}\right)\left(\frac{r_D^2 - r^2}{r}\right) \tag{10.20}$$

The peak field occurs at the metallurgical junction at $r = r_J$,

$$E_M = E(r_J) = \left(-\frac{qN_D}{2\varepsilon_S}\right)\left(\frac{r_D^2 - r_J^2}{r_J}\right) \tag{10.21}$$

Integrating Equation 10.20 with respect to r to calculate the potential $\psi\ (r)$, and setting $\psi(r_J) = 0$, we obtain

$$\psi(r) = \left(\frac{qN_D}{2\varepsilon_S}\right)\left[\left(\frac{r_J^2 - r^2}{2}\right) + r_D^2 \ln\left(\frac{r}{r_J}\right)\right] \tag{10.22}$$

The total voltage across the depletion region is the potential difference $\psi(r_D) - \psi(r_J)$,

$$V_R = \psi(r_D) = \left(\frac{qN_D}{2\varepsilon_S}\right)\left[\left(\frac{r_J^2 - r_D^2}{2}\right) + r_D^2 \ln\left(\frac{r_D}{r_J}\right)\right] \tag{10.23}$$

The peak field can be plotted as a function of reverse voltage by choosing successively larger values of r_D and evaluating Equations 10.21 and 10.23. Figure 10.9 shows the effect of junction curvature on the peak field for several values of r_J at an assumed doping of 2×10^{15} cm^{-3}. The peak field of a planar junction of the same doping is also shown for comparison. Reducing the junction radius r_J increases the peak field at a given reverse voltage, and this will significantly reduce the breakdown voltage. Because of this effect, the blocking voltage of practical devices is normally limited by edge breakdown unless special edge termination techniques are employed.

Edge terminations used in SiC devices fall into five general classes: trench isolation, beveled junctions, junction termination extension (JTE), floating field rings (FFRs), and multiple floating zone (MFZ-) or space-modulated (SM-) JTE. We will discuss each of these below.

10.1.3 Trench Edge Terminations

Trench isolation is useful when the reverse voltage is below about 2 kV and the depletion width at breakdown is on the order of 10 μm or less. Under these conditions it is possible to etch an isolation trench extending ~15–20% through the lightly-doped drift region, as illustrated in Figure 10.10. This simple technique is often sufficient because it tends to linearize field lines near the p + /n− junction where the field is highest. Although field crowding occurs at the corner of the trench, the field here is considerably

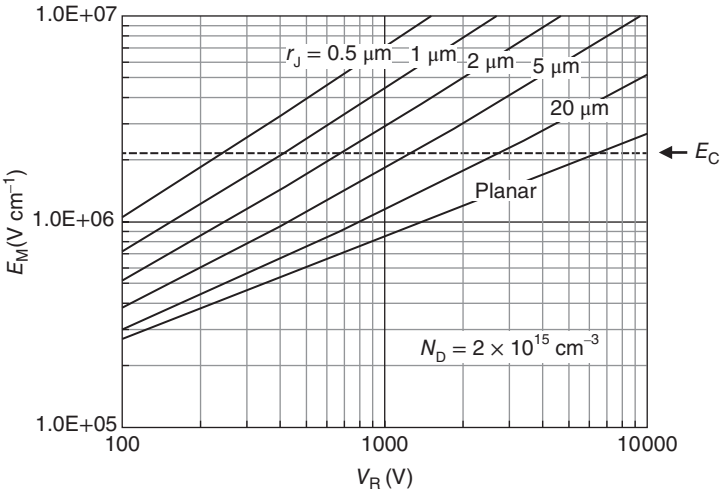


Figure 10.9 Peak field at the cylindrical junction as a function of reverse voltage, with junction radius as a parameter.

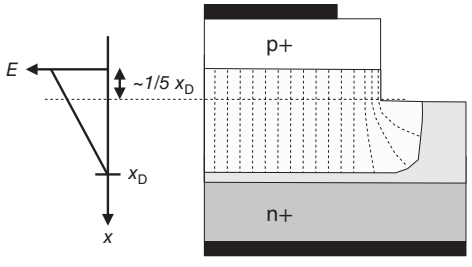


Figure 10.10 Cross-section of a p + /n− one-sided step junction terminated by trench isolation.

lower than the peak field, reducing the negative impact of field crowding. A high-quality passivation layer is required to control surface charges and prevent surface leakage.

10.1.4 Beveled Edge Terminations

At higher blocking voltages, an effective way to provide edge termination is the use of a beveled junction profile. A *positive bevel* is one in which the junction area decreases with distance into the lightly-doped side, as illustrated in Figure 10.11 for a p + /n− junction. The requirement for charge balance on either side of the junction causes an increase in the depletion width on the lightly-doped side near the beveled surface. In this case, the charge balance is restored by replacing the positive charge missing from area Q_1 by a roughly equal additional charge Q_2. As a result, the depletion width along the beveled surface W_S is larger than the depletion width W in the bulk. Since the potential drop across the junction is the same everywhere, the electric field along the surface is reduced relative to that in the bulk. Numerical simulations confirm that the surface field is reduced below the bulk field for all bevel angles $0 < \theta < 90°$ [5]. In practice, most SiC power devices are fabricated with the heavily-doped layer on top, making it difficult to achieve a positive bevel in real devices.

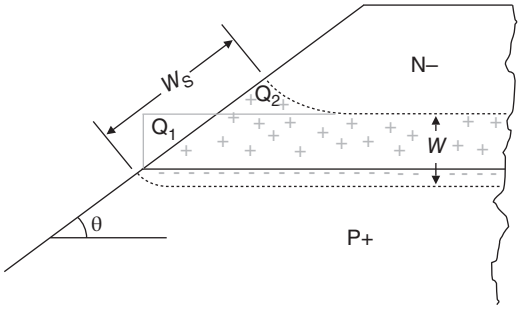
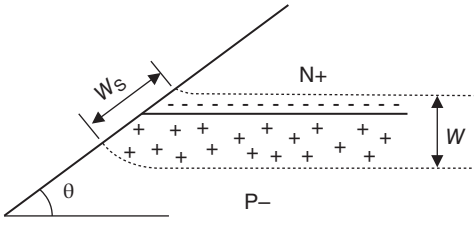
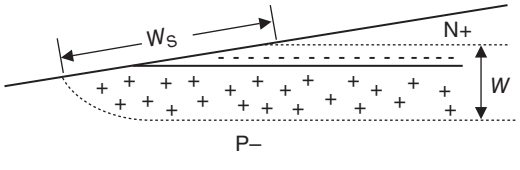


Figure 10.11 Charge distribution in a p + /n− junction with a positive bevel.



Negative Bevel, Large Bevel Angle



Negative Bevel, Small Bevel Angle

Figure 10.12 Charge distribution in an n + /p− junction with a negative bevel.

A *negative bevel* is one in which the junction area increases with distance into the lightly-doped side, as illustrated in Figure 10.12 for an n + /p− junction. In this case the depletion region on the lightly-doped side shrinks near the surface to balance the missing charge in the heavily-doped side. This tends to make the depletion width along the surface W_S smaller than the depletion width W in the bulk, increasing the surface field above the bulk field. However, at very small bevel angles the shallow slope makes the increase in depletion width on the heavily-doped side exceed the decrease in depletion width on the lightly-doped side, as illustrated in the lower part of Figure 10.12. When this occurs, the peak surface field is once again lower than the peak field in the bulk.

The exact conditions under which a negative bevel reduces the surface field can be predicted by a two-dimensional numerical solution of Poisson's equation. Adler and Temple have studied negative bevels in silicon junctions where the heavily-doped layer is formed by diffusion [6]. After extensive simulations, they found that for negative beveled junctions the normalized breakdown voltage (as a fraction of the ideal breakdown voltage) can be represented by a universal curve that depends on an *effective* bevel angle θ_{EFF} given by

$$\theta_{EFF} = 0.04\theta(x_{DB}^{-}/x_{DB}^{+})^2 \tag{10.24}$$

Here θ is the actual bevel angle, $x_{DB}{}^{-}$ is the depletion width on the lightly-doped side at breakdown, and $x_{DB}{}^{+}$ is the depletion width on the heavily-doped side at breakdown. Figure 10.13 shows normalized

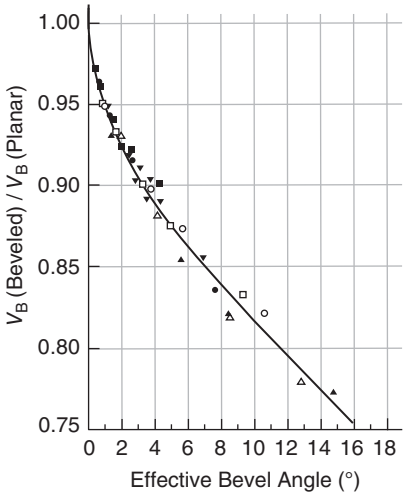


Figure 10.13 Normalized breakdown voltage as a function of effective bevel angle θ_{EFF} for a negatively-beveled silicon junction with a graded doping profile ([6] reproduced with permission from IEEE).

breakdown voltage as a function of effective bevel angle. For sufficiently small angles the breakdown approaches the ideal planar-junction value. However, these simulations were carried out for graded, diffused junctions with a complementary error function doping profile, and the results may not be accurate for the abrupt junctions typically formed in SiC.

Figure 10.14 shows the maximum field at the surface and the maximum field in the bulk material, normalized to the ideal breakdown field, as a function of effective bevel angle [6]. At small bevel angles the maximum surface field is well below the ideal (planar) breakdown field, but the maximum field in the bulk is slightly higher than the ideal breakdown field. This means that avalanche breakdown first occurs in the bulk near the surface, rather than at the surface itself, and the breakdown voltage is therefore lower than the ideal (planar) value. As the effective bevel angle is increased, both the maximum surface field and the maximum bulk field increase and the breakdown voltage is further reduced.

10.1.5 Junction Termination Extensions (JTEs)

The third form of edge termination used in SiC is junction termination extension (JTE) [7]. This termination consists of one or more concentric p-type rings of carefully-controlled dopant concentration surrounding the main junction, as shown in Figure 10.15. The key requirement is that the total dopant concentration per unit area in each ring be low enough that the ring will be completely depleted before avalanche breakdown occurs at the edge of the ring. The exposed acceptor atoms in the depleted rings then terminate field lines that otherwise would crowd into the corner of the main junction. The field lines in this situation are illustrated schematically in Figure 10.16.

Because of the two-dimensional nature of the fields, optimization of JTE ring design is best performed by computer simulations. Figure 10.17 shows breakdown voltage as a function of dose for single-zone JTE terminations of various widths on a 100 μm n− SiC drift region doped 6×10^{14} cm^{-3} [8]. The breakdown voltage peaks at the dose where the ring becomes depleted just before reaching breakdown. For higher doses, the ring does not fully deplete and breakdown occurs at the outer edge of the ring. For lower doses, the ring depletes without breaking down, and breakdown occurs at the edge of the main junction.

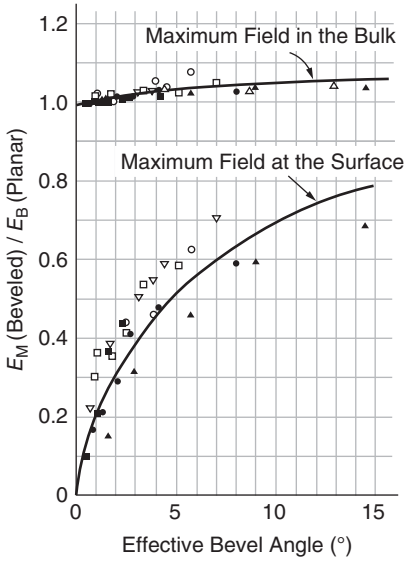


Figure 10.14 Maximum field at the surface and maximum field in the bulk material as a function of effective bevel angle for negatively-beveled silicon junctions with a graded doping profile ([6] reproduced with permission from IEEE).

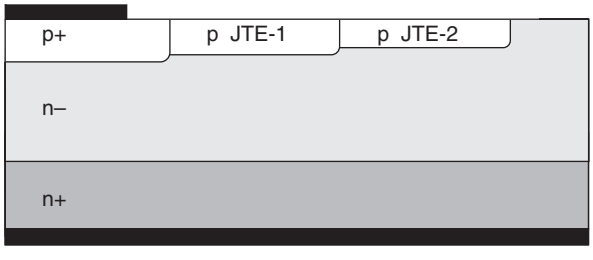


Figure 10.15 Cross-section of a p + /n− one-sided step junction protected by a two-zone junction termination extension (JTE).

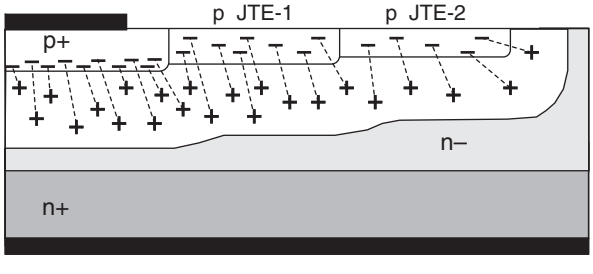


Figure 10.16 Illustration of field lines in a two-zone JTE termination under reverse bias.

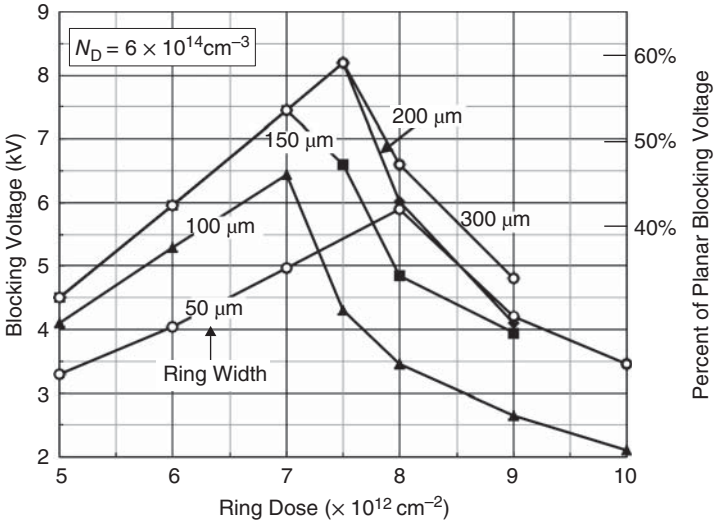


Figure 10.17 Blocking voltage as a function of ring dose (dopant concentration per unit area) for single-zone JTE terminations with ring width as a parameter. The n− drift region has a theoretical planar breakdown voltage of 13.8 kV ([8] reproduced with permission from Imran A. Khan).

For a given ring width, the breakdown voltage falls rapidly for doses higher than the optimum dose. For this reason, it is customary to select a dose that is approximately 75% of the optimum, to allow for variation in implant activation percentage during processing. The maximum breakdown voltage increases with ring width until the width is about twice the thickness of the depletion region at breakdown.

The narrow dose window to achieve a high breakdown voltage can be mitigated by the use of multiple JTE rings. Figure 10.18 shows the breakdown voltage for a three-zone JTE system on a 100 μm n− drift region doped 8×10^{14} cm^{-3} [9]. The dose of the inner ring is fixed at three times that of the outer ring, and the dose of the middle ring is twice that of the outer ring. The breakdown voltage exhibits three peaks as a function of dose. These correspond to transitions in the location of the breakdown point within the structure. At high doses, none of the rings deplete and breakdown occurs at the edge of the outer ring. As the outer ring dose falls below 1.1×10^{13} cm^{-2}, this ring becomes completely depleted before breaking down and the breakdown point shifts to the edge of the middle ring. When the outer ring dose falls below 7×10^{12} cm^{-2}, corresponding to a middle ring dose of 1.4×10^{13} cm^{-2}, the middle ring also depletes before breaking down and breakdown shifts to the edge of the inner ring. When the outer ring dose falls below 4.5×10^{12} cm^{-2}, corresponding to an inner ring dose of 1.3×10^{13} cm^{-2}, the inner ring depletes and breakdown moves to the edge of the main junction. By including multiple rings, the range of dose over which a high breakdown voltage is achieved is widened considerably.

Simulations indicate that the depth and dopant profile of the JTE implant have little effect on performance [9], but surface charge can play an important role and should be controlled by the use of a high-quality oxide passivation layer.

10.1.6 Floating Field-Ring (FFR) Terminations

Floating field-ring (FFR) terminations consist of a series of isolated concentric p+ rings surrounding the main junction, and are usually formed in the same processing step as the main junction so that no additional processing is required. Since the rings are heavily doped, the performance of a floating field-ring system does not require precise control of activated implant dose.

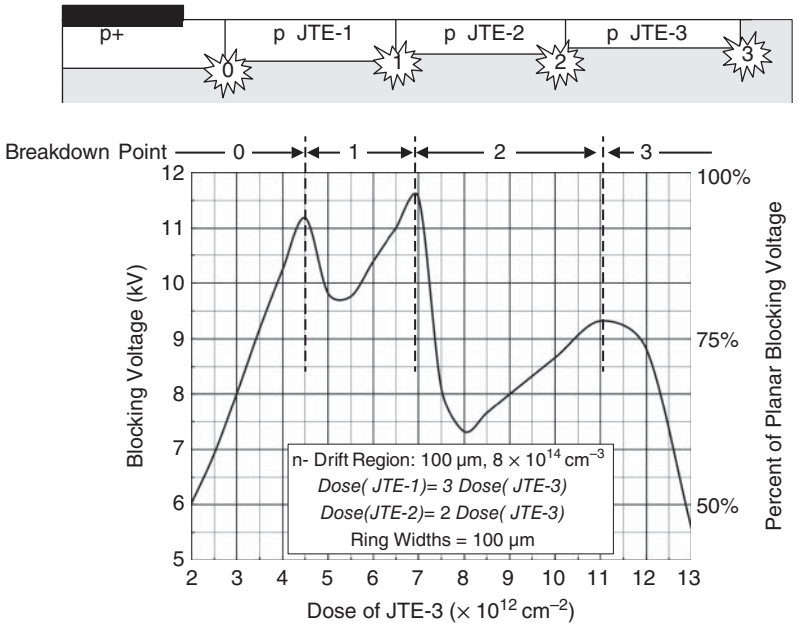


Figure 10.18 Blocking voltage as a function of ring dose for a three-zone JTE termination. The n− drift region is 100 µm thick, doped 8×10^{14} cm^{-3}, with a theoretical planar breakdown voltage of 12 kV ([9] reproduced with permission from Trans Tech Publications).

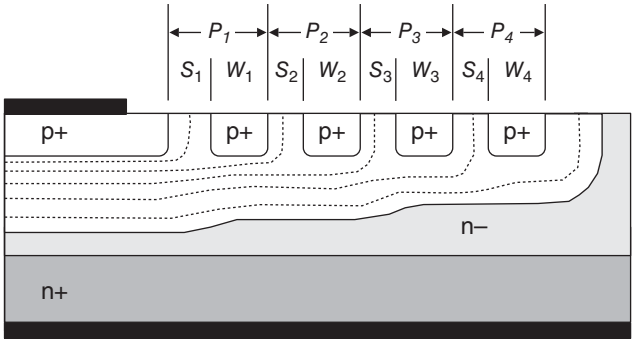


Figure 10.19 Cross-section of a p + /n− one-sided step junction protected by four floating field rings (FFRs). Several equipotential lines under reverse bias are illustrated.

Figure 10.19 illustrates a four-ring FFR termination along with equipotential lines under reverse bias. As the reverse voltage is increased from zero, the depletion region of the main junction gradually expands until it reaches the first field ring. This ring then acts as an equipotential region and the depletion region continues to expand outward from this ring. The equipotential lines in the figure may be taken as representative of the successive positions of the depletion edge as the reverse voltage is gradually increased. The effect of the FFRs is to spread out the potential distribution laterally along

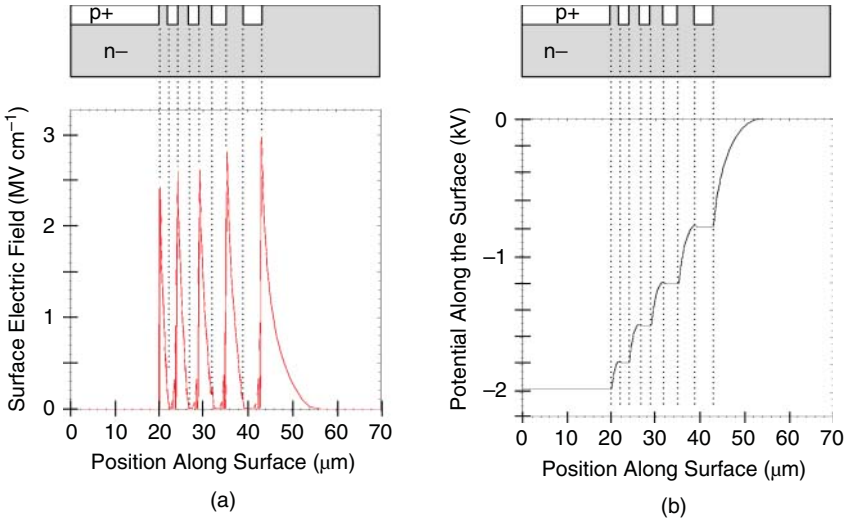


Figure 10.20 Electric field (a) and electrostatic potential (b) at the surface of a four-ring FFR termination on a 25 μm n− drift region doped 3.4×10^{15} cm^{-3}. The reverse voltage is 1.975 kV and the ring parameters are $S_1 = 2$ μm, $W/S = 1$, and $X_{FFR} = 1.25$ ([10], reproduced with permission from James A. Cooper).

the surface, reducing the lateral electric field that would otherwise initiate avalanche breakdown at the main junction.

Figure 10.20 shows electric field and potential along the surface under 1975 V reverse bias for a four-ring FFR termination on a 25 μm drift region doped 3.4×10^{15} cm^{-3} [10]. The highest field values occur at the outer edges of the field rings. The ring system spreads the potential laterally along the surface, as seen from the potential plot.

Since the field rings are all heavily doped, doping is not a design variable, but the number of rings, the width of each ring, and the spacing of each ring from the next inner ring are all design parameters. To be effective, the ring system should extend laterally at least twice the depth of the depletion region at breakdown. For high-voltage devices it is not unusual to incorporate several tens of concentric rings, and this introduces an inordinate number of free design parameters. Therefore, it is helpful to adopt a systematic method of specifying ring widths and spacings. For example, one approach is to require that the width and spacing of every ring have the same ratio W/S, and that the width (and spacing) increase with successive rings by a fixed *expansion ratio* defined as

$$X_{FFR} = W_{i+1}/W_i = S_{i+1}/S_i \tag{10.25}$$

In this implementation, the period $P_i = W_i + S_i$ also increases with successive rings by the expansion ratio X_{FFR}. Under these constraints, one can evaluate FFR system performance as a function of the initial spacing of the first ring S_1, the W/S ratio, the expansion ratio X_{FFR}, and the total number of rings in the system. Figure 10.21 shows breakdown voltage obtained by numerical simulation for a number of different ring systems on a 25 μm SiC n-type drift layer doped 3.5×10^{15} cm^{-3} [10]. This layer has a theoretical planar breakdown voltage of 3.5 kV. In the plot, each point denotes a specific number of rings and total width of the ring system for a particular design, and the expressions in parentheses give the initial spacing S_1, expansion ratio X_{FFR}, and width-to-spacing ratio W/S.

Although no specific algorithm for optimum design emerges, we can make some general observations. First, increasing the total width of the ring system increases the breakdown voltage, but the improvement

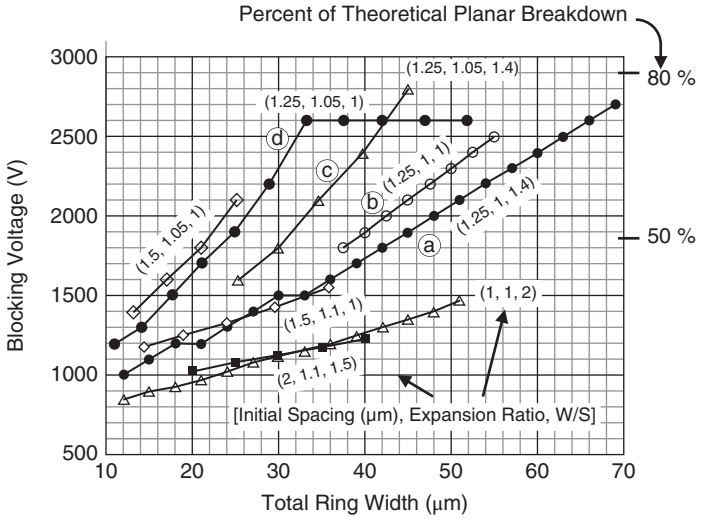


Figure 10.21 Blocking voltage versus total ring width for a variety of FFR terminations on a 25 μm n− drift region doped 3.5×10^{15} cm^{-3} [9]. Each point represents a possible ring system, with the total width of the ring system given on the horizontal axis ([10], reproduced with permission from James A. Cooper).

saturates when the ring system extends beyond the lateral depletion width at breakdown. Second, comparing curve (a) to (c) and curve (b) to (d) we conclude that an expansion ratio of 5% (1.05) gives a higher blocking voltage than a uniform ring spacing at a given total FFR width. Third, comparing (a) to (b) and (c) to (d) we see that in the regime where breakdown voltage is increasing with ring width, a W/S ratio of 1 gives a higher blocking voltage at a given total FFR width than a W/S ratio of 1.4. Finally, comparing (c) to (d) we conclude that a W/S ratio of 1.4 may allow a higher saturation value of blocking voltage than a W/S ratio of 1.0.

To summarize, floating field rings can provide blocking voltages of 75–80% of the ideal planar breakdown. They are not sensitive to the activated dopant concentration, and can be fabricated without any additional processing steps. High-voltage SiC devices have been fabricated with as many as 50 concentric rings in their edge termination structure.

10.1.7 Multiple-Floating-Zone (MFZ) JTE and Space-Modulated (SM) JTE

As discussed above, single-zone JTE is sensitive to the activated dopant concentration, and the tight processing tolerance is a challenge in manufacturing. Multi-zone JTE reduces the sensitivity to activated dopant concentration, but brings added processing complexity and cost. The tight processing tolerance of JTE can be avoided with floating field rings, since they are insensitive to the activated dopant concentration. However, it is difficult to identify an algorithm for optimizing FFR terminations.

A fifth termination method combines concepts from both JTE and FFR terminations. Multiple floating zone (MFZ) JTE [11] and space-modulated (SM) JTE [12] are closely-related techniques that achieve the broad dose window of multi-zone JTE with a single implant step. MFZ-JTE employs a series of concentric floating rings having a dose that allows each ring to fully deplete before reaching breakdown. The structure, shown in Figure 10.22, is similar to the FFR structure in Figure 10.19, but the rings are

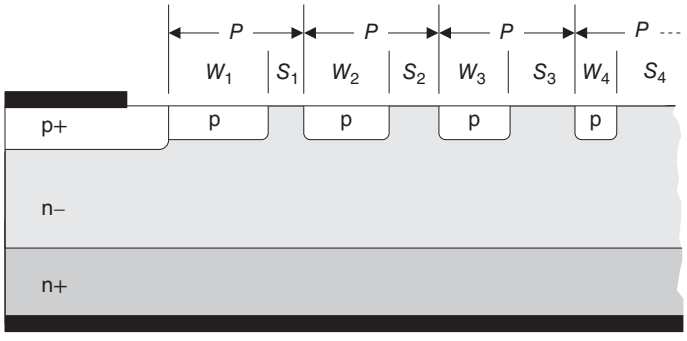


Figure 10.22 Cross-section of a p + /n− one-sided step junction protected by multiple-floating-zone JTE termination. The period of each zone is the same, but the W/S ratio decreases from the inner to the outer ring.

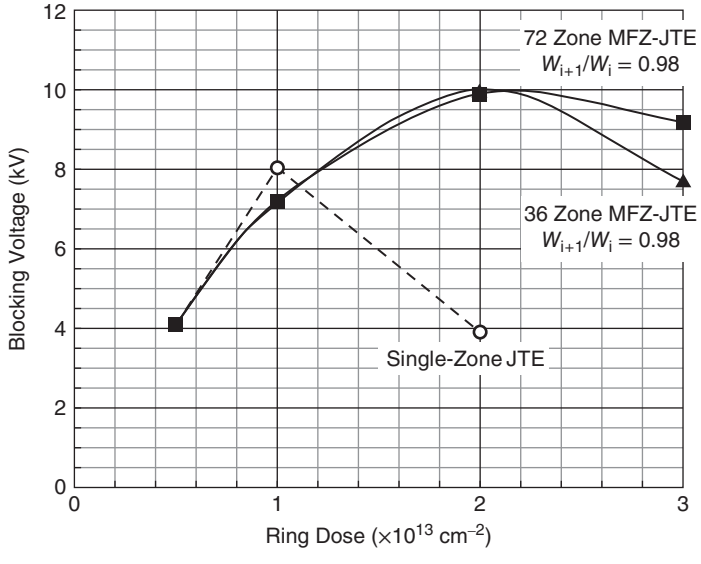


Figure 10.23 Blocking voltage as a function of ring dose for single-zone JTE and two MFZ-JTE terminations on a 120 μm n− drift region doped 8.9×10^{14} cm^{-3} ([11] reproduced with permission from IEEE).

more lightly doped. A careful examination will also reveal that each zone has the same period $P = W_i + S_i$, but the W/S ratio of successive zones decreases as we move away from the main junction. In this way the effective termination charge in each zone can be tapered smoothly from the full dose at the main junction to zero at the edge of the ring system. Figure 10.23 shows the breakdown voltage on a 120 μm, 8.9×10^{14} cm^{-3} n-type drift layer for single-zone JTE, a 36-zone MFZ-JTE and a 72-zone MFZ-JTE, as a function of ring dose [11]. All three terminations have a total width of 450 μm. The MFZ-JTE system provides a much broader range of acceptable doses than the single-zone JTE.

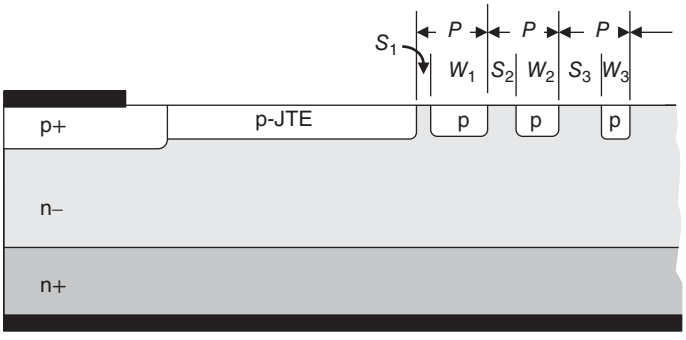


Figure 10.24 Cross-section of a p + /n− one-sided step junction protected by a space-modulated JTE termination, consisting of a single JTE ring whose outer edge is split into a number of concentric floating rings.

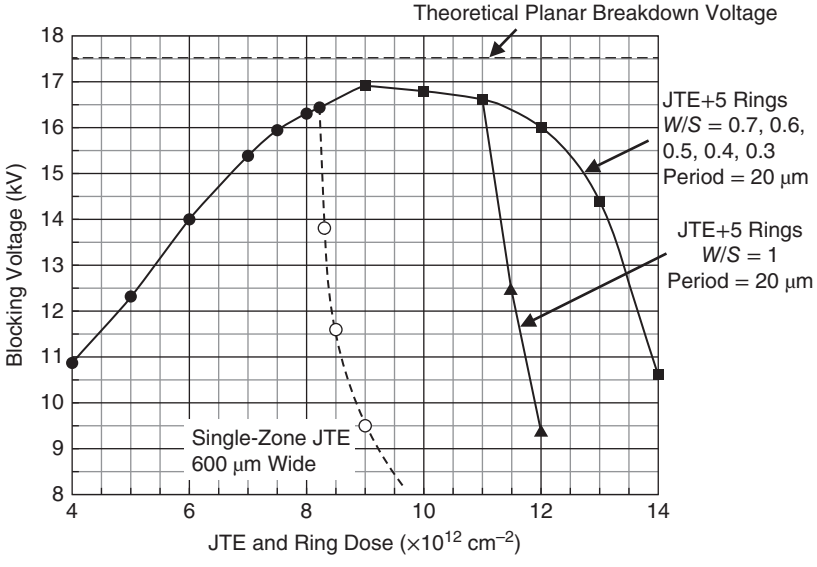


Figure 10.25 Blocking voltage as a function of ring dose for a single-zone JTE and two SM-JTE terminations on a 120 μm n− drift region doped 1×10^{14} cm^{-3} ([11] reproduced with permission from IEEE). The theoretical planar breakdown voltage for this drift layer is 17.5 kV.

Space-modulated (SM) JTE consists of a single broad JTE ring whose outer edge is broken into a number of isolated concentric rings of the same dose, as shown in Figure 10.24. Figure 10.25 shows the breakdown voltage on a 120 μm, 1×10^{14} cm^{-3} n-type drift layer for a single-zone JTE, a five-ring SM-JTE with constant W/S ratio, and a five-ring SM-JTE with a decreasing W/S ratio [12]. Both SM-JTE terminations have a constant ring period $P = W_i + S_i = 20$ μm, and all three terminations have a total width of 600 μm. The five-ring SM-JTE with decreasing W/S ratio provides the broadest range of acceptable doses.

The termination techniques discussed above can be applied with only minor modifications to all the SiC power devices discussed in this book.

10.2 Optimum Design of Unipolar Drift Regions

Unipolar devices such as the Schottky diode, JFET and MOSFET have negligible stored charge, and their switching loss is small compared to their on-state power dissipation. The on-state power dissipation of a unipolar device was given in Equation 7.5 as

$$P_{ON} = R_{ON,SP} J_{ON}^2 \tag{7.5}$$

where $R_{ON,SP}$ is the specific on-resistance and J_{ON} is the on-state current density. The unipolar device figure of merit was defined in Equation 7.9 as

$$FOM = A\sqrt{P_{MAX} V_B^2 / R_{ON,SP}} \tag{7.9}$$

where A is the area of the device, P_{MAX} the maximum allowable power dissipation, and V_B the blocking voltage. The area A is limited by material, yield, and cost considerations, and the maximum power dissipation P_{MAX} is limited by the thermal capability of the device and package. The remaining quantity ${V_B}^2/R_{ON,SP}$ is the figure of merit for the device, and it is the goal of the designer to maximize this quantity.

10.2.1 Vertical Drift Regions

All power devices support the terminal voltage in the blocking state by a reverse-biased junction, and for most vertical SiC power devices this is a p + /n− one-sided step junction, such as shown in Figure 7.1. If we neglect field crowding and assume uniform doping in the n− region, the blocking voltage can be written

$$V_B = \begin{cases} \left(\varepsilon_S E_C^2\right)/\left(2qN_D\right), & x_{DB} \le W_N \\ \left(E_C^* - \dfrac{qN_D W_N}{2\varepsilon_S}\right) W_N, & x_{DB} > W_N \end{cases} \tag{10.26}$$

Here x_{DB} is the depletion width at breakdown for a p + /n− one-sided step junction with an infinitely wide n− region, such as shown in Figure 7.1, and ${E_C}^*$ will be defined below. Assuming a triangular field profile, x_{DB} is given by

$$x_{DB} = \varepsilon_S E_C / (qN_D) \tag{10.27}$$

The critical field E_C is given as a function of doping in Equation 10.17 and is plotted in Figure 10.5. We define ${E_C}^*$ as the effective critical field in a truncated p + /n − /n+ junction with a trapezoidal field profile, such as shown in Figure 7.2, and its dependence on doping and width of the drift region is shown in Figure 10.7. The resulting dependence of V_B on doping and width of the drift region is given by Equation 10.26 and is plotted in Figure 7.3.

The specific on-resistance of a unipolar device is the sum of all the resistance elements between the terminals, but if the blocking voltage is high the on-resistance is dominated by the resistance of the drift region. The specific on-resistance of the drift region can be written

$$R_{ON,SP} = W_N / (q\mu_N N_D^+) \tag{10.28}$$

where ${N_D}^+$ is the *ionized* dopant density in the drift region. The mobility parallel to the *c*-axis in 4H-SiC can be described by the empirical expression [2]

$$\boxed{\mu_N = \frac{1141(T/300)^{-2.8}}{1 + (N_D/1.94 \times 10^{17})^{0.61}}} \tag{10.29}$$

which is plotted in Figure 10.26.

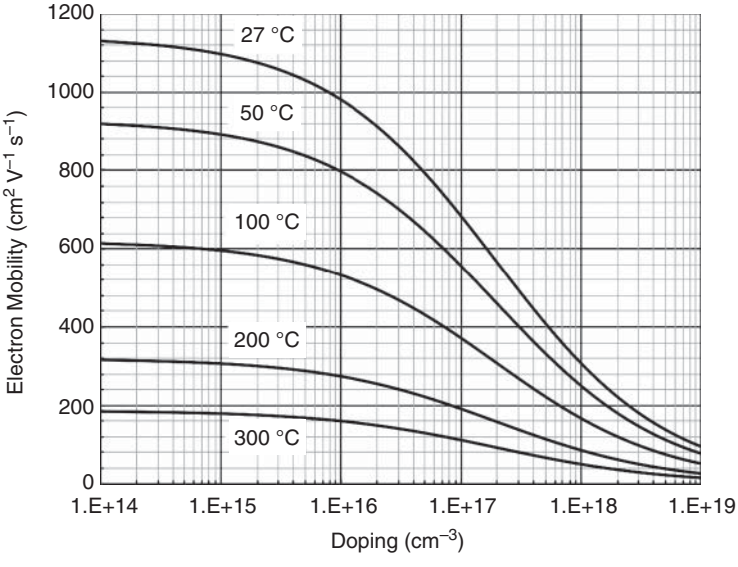


Figure 10.26 Electron mobility parallel to the *c*-axis in 4H-SiC as a function of doping and temperature, as given by Equation 10.29.

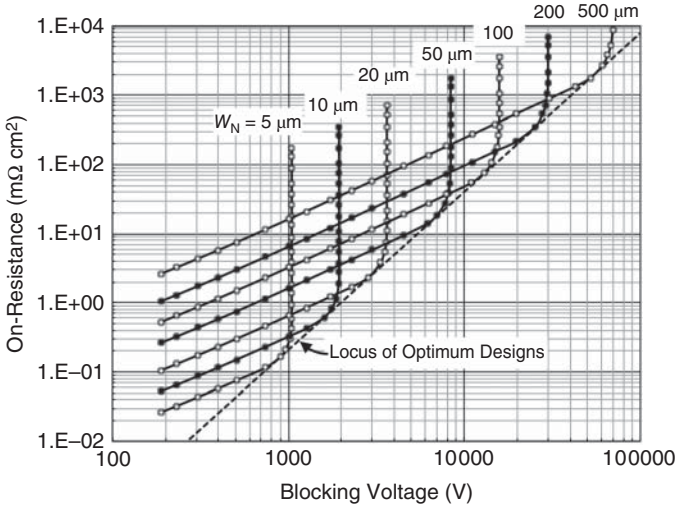


Figure 10.27 Specific on-resistance of an n− drift region in 4H-SiC at room temperature as a function of blocking voltage with drift region width as a parameter.

For the unipolar drift region, Equations 10.26–10.29 establish a relationship between on-resistance and blocking voltage. We can examine this relationship by stepping the doping through a series of values and calculating $R_{ON,SP}$ and V_B at each doping, with the mobility and critical field re-evaluated at each doping. The on-resistance can then be plotted as a function of blocking voltage, as shown in Figure 10.27. The points on each curve correspond to different values of doping, decreasing from 2×10^{17} cm^{-3} on

the left to 1.5×10^{13} cm^{-3} on the right (in the sequence 2.0, 1.5, 1.0, 0.7, 0.5, 0.3, 0.2). As the doping is decreased, the depletion region width at breakdown x_{DB} increases, following Equation 10.27, and the blocking voltage increases according to Equation 10.26. Eventually the depletion region extends through the entire drift region and the blocking voltage increases more slowly, finally saturating at the value $E_C{}^* W_N$, as shown by Equation 10.26. The electric field profiles are illustrated in Figure 7.2. Note that even after the blocking voltage saturates, the on-resistance continues to increase as doping is reduced, as shown by Equation 10.28, and the $R_{ON,SP}-V_B$ characteristic becomes almost vertical.

The optimum design point for the unipolar drift region is the doping – thickness combination that produces the lowest on-resistance at a specified blocking voltage. The dashed line tangent to the curves in Figure 10.27 is the locus of optimum design points and can be described by the empirical equation [2]

$$R_{ON,SP}(\text{opt}) \approx 2.8 \times 10^{-8} (T/300)^{2.8} V_B^{2.29} \ (\text{m}\Omega\ \text{cm}^2) \tag{10.30}$$

To illustrate the use of these curves, suppose the specified blocking voltage is 3 kV. Then Figure 10.27 tells us the optimum design has a drift region width of 20 μm and a doping of about 5×10^{15} cm^{-3} (the doping can be found by counting points on the 20 μm curve from 2×10^{17} cm^{-3} on the left to 5×10^{15} cm^{-3} at the optimum point, in the sequence 2.0, 1.5, 1.0, etc.). To facilitate identification of the optimum doping, Figure 10.28 plots the figure of merit as a function of doping, with drift region width as a parameter. For a 20 μm drift region, the optimum doping is very close to 5×10^{15} cm^{-3}. The optimum doping and drift region width for a desired blocking voltage are independent of temperature and are given by the empirical equations [2]

$$N_D(\text{opt}) \approx 1.1 \times 10^{20} V_B^{-1.27} \ (\text{cm}^{-3}) \tag{10.31}$$

$$W_N(\text{opt}) \approx 2.62 \times 10^{-3} V_B^{1.12} \ (\mu\text{m}) \tag{10.32}$$

For easy reference, Figure 10.29 plots the optimum doping and drift region width from Equations 10.31 and 10.32 as a function of blocking voltage.

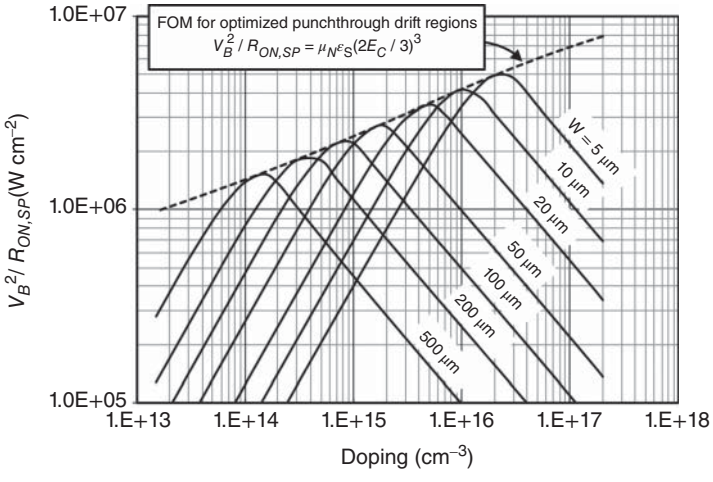


Figure 10.28 Unipolar device figure of merit $V_B{}^2/R_{ON,SP}$, evaluated at room temperature as a function of doping with drift region width as a parameter. For a given width, the optimum doping is the doping for which the FOM is a maximum.

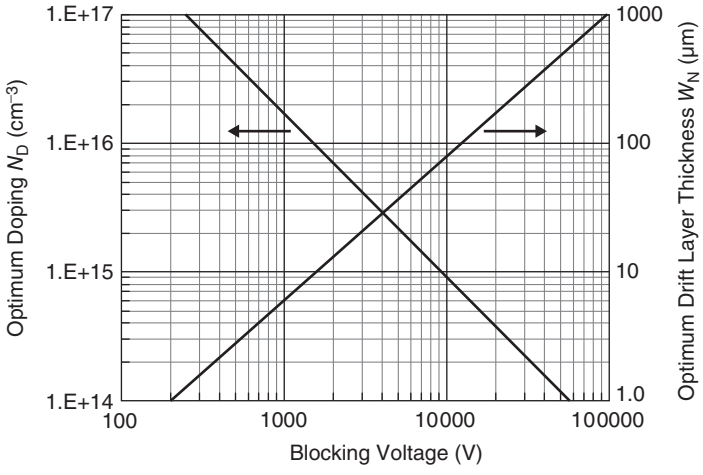


Figure 10.29 Optimum drift region doping and width as a function of blocking voltage for n-type drift regions in 4H-SiC.

10.2.2 Lateral Drift Regions

When the blocking voltage is not too high, it is feasible to implement power devices using a lateral structure rather than a vertical structure. This places all electrical terminals, the source, gate, and drain, on the top surface. The lateral structure is particularly suited to *power integrated circuits,* where the power transistor is monolithically integrated with control electronics on the same chip.

Figure 10.30 shows the cross-section of a lateral MOSFET that employs the reduced-surface-field (RESURF) concept [13]. The lightly-doped drain (LDD) extends laterally a distance L along the surface and has thickness T. In the blocking state, a reverse bias exists between the n-type drain and the grounded p-type body layer underneath, and the LDD is designed so that it completely depletes before the field at the junction reaches the critical field for avalanche breakdown. This requires

$$qN_D T < \varepsilon_S E_C \tag{10.33}$$

where N_D is the LDD doping and E_C is the critical field. The significant feature of this structure is that when the LDD is fully depleted, all the field lines from donor charges in the LDD extend vertically, terminating on acceptor charges in the base layer below, as illustrated in Figure 10.31. Since all the

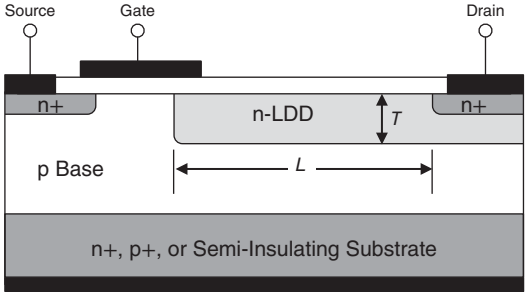


Figure 10.30 Cross-section of a lateral power MOSFET using the reduced-surface-field (RESURF) concept. The p-type base layer is at ground potential.

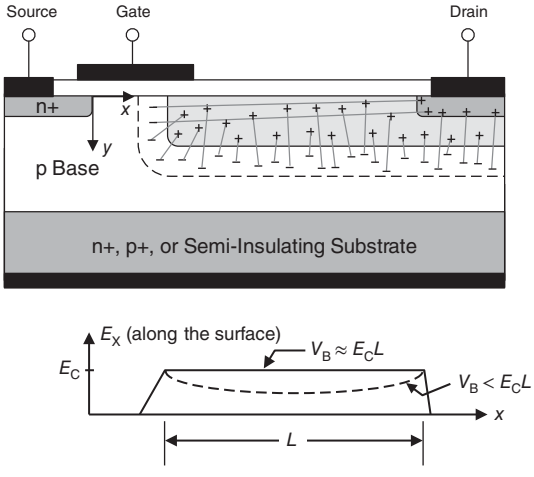


Figure 10.31 Illustration of electric field lines in a lateral RESURF MOSFET in the blocking state. The surface electric field is plotted below the figure, and the dashed line indicates the approximate field when two-dimensional effects are included.

donor charges in the LDD are terminated on acceptors in the base layer, x-directed field lines do not terminate on charges in the LDD layer, and there is no field taper in the x-direction, as indicated in the plot. This means that we can increase the drain voltage until E_X reaches the critical field E_C, at which point the blocking voltage is given by

$$V_B \approx E_C L \tag{10.34}$$

The specific on-resistance of the LDD is

$$R_{ON,SP} = R \cdot A = \left(\frac{\rho L}{WT}\right)(WL) = \frac{L^2}{q\mu_N N_D T} \tag{10.35}$$

where ρ is the resistivity of the LDD layer and W is the width of the device. Note that the on-resistance depends only on the doping-thickness product $N_D T$ and the length of the LDD region.

We can calculate the figure of merit for the RESURF structure, assuming the LDD resistance dominates the device resistance. Using Equations 10.33–10.35 we can write

$$\frac{V_B^2}{R_{ON,SP}} = V_B^2\left(\frac{q\mu_N N_D T}{L^2}\right) = V_B^2\left(\frac{\mu_N \epsilon_S E_C}{V_B^2/E_C^2}\right) = \mu_N \epsilon_S E_C^3 \tag{10.36}$$

Comparing Equation 10.36 to Equation 7.13, we find that the theoretical limit of a RESURF device is actually four times larger than that of a comparable vertical unipolar power device. However, the situation is not as simple as our analysis would indicate, since we have neglected two-dimensional effects. In practice, field crowding at the ends of the LDD produces field spikes, and the true field is like the dashed line in Figure 10.31. Nevertheless, lateral RESURF devices are a viable alternative to vertical devices in cases where the blocking voltage is not too high.

Although Figures 10.30 and 10.31 illustrate a lateral MOSFET, the same discussion applies to any unipolar device with a lateral drift region, such as a lateral JFET. A modified version of the RESURF principle is also utilized in silicon super-junction MOSFETs, where the drift regions are vertical. To date, no vertical super-junction devices have been reported in SiC.

10.3 Comparison of Device Performance

We conclude this chapter by considering how the different types of power devices may be compared in terms of performance. A fair comparison requires that we evaluate all devices as a function of both blocking voltage and switching frequency, since switching loss is a major limitation on device performance. As discussed in Section 7.1, our figure of merit is the on-state current density J_{ON} that each device can carry at a specified switching frequency and blocking voltage, subject to the requirement that the total power dissipation in the device be less than the package limit, which we will arbitrarily take as 300 W cm^{-2}. We designate this current density as J_{300}, and the device with the highest J_{300} at a given blocking voltage and switching frequency is the preferred device for that application.

The above relationships can be visualized using the construction of Figure 10.32, which compares a power MOSFET and an IGBT in a three-dimensional $J_{ON}-V_B-f$ parameter space. The two surfaces represent the loci of constant power dissipation equal to 300 W cm^{-2}. Let's first examine how these surfaces depend on blocking voltage and frequency.

To achieve a higher blocking voltage, it is necessary to use a thicker and more lightly-doped drift region. This increases the on-resistance of the device, and hence the on-state power dissipation. To keep the total power below the assumed package limit of 300 W cm^{-2}, we must reduce the current density as the blocking voltage is increased. This explains why the surfaces slope downward as V_B is increased.

Frequency enters the picture through the switching loss. The switching power dissipation is directly proportional to switching frequency. If we are required to operate at a higher frequency where the switching loss is higher, we must again decrease the current to keep the total power dissipation below 300 W cm^{-2}. This explains the slope of the surfaces downward as frequency is increased. The effect is stronger for bipolar devices such as the IGBT, since they dissipate more energy per switching event.

The constant-power surfaces of the MOSFET and the IGBT intersect along a line that can be projected down to the V_B-f plane. This line represents the design points where the two devices have equal performance, in that they permit the same maximum on-state current for operating points along this line. In this example, the IGBT carries higher current at low switching frequencies, while the MOSFET carries higher current at high frequencies. Constructions such as this enable us to visualize the relative performance of different devices in the full current–voltage–frequency parameter space.

The above visualization can be made quantitative as follows. For unipolar devices we can usually assume (i) the I–V characteristics near the origin are linear, and hence can be described by an

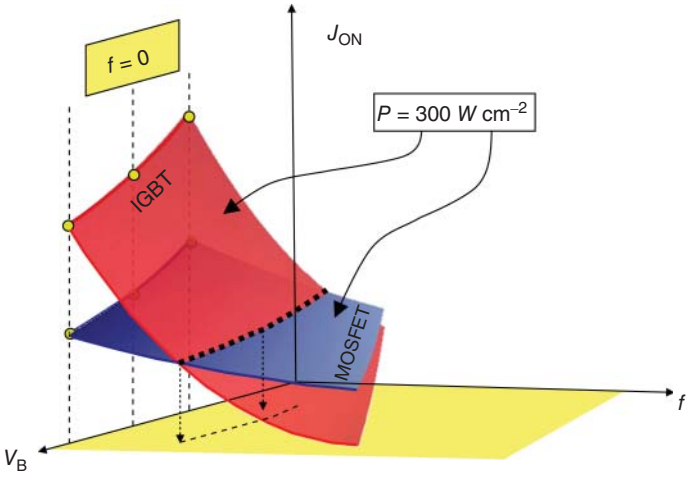


Figure 10.32 Surfaces of constant power dissipation of a MOSFET and an IGBT in three-dimensional $J_{ON}-V_B-f$ parameter space ([15] reproduced with permission from Trans Tech Publications).

on-resistance, and (ii) the switching power is small compared to the on-state power dissipation. These assumptions led to Equations 7.8 and 7.9, and the figure of merit for unipolar devices was taken to be $V_B{}^2/R_{ON,SP}$. However, in bipolar devices the current passes through one or more forward-biased pn junctions, and these inject minority carriers that must be removed during the turn-off transient. Hence we must consider the energy dissipated during each switching cycle E_{SW}. The switching power dissipation is proportional to the switching energy and the frequency, as given in Equation 7.15. Moreover, since the current path in bipolar devices goes through forward-biased diodes whose I–V characteristics are nonlinear, the on-state I–V characteristics often cannot be described by a simple resistance. (This statement depends on the *number* of forward-biased junctions in the current path. The pin diode, IGBT, and thyristor have an *odd* number of forward-biased junctions in the current path, and their I–V characteristics are nonlinear near the origin. The BJT has an *even* number of forward-biased junctions, and its I–V characteristics near the origin are linear.)

To account for both the switching loss and the nonlinear I–V characteristics, we use the procedure described in Section 7.1, which is summarized as follows:

1. Determine the dependence of switching energy E_{SW} on on-state current J_{ON} using two-dimensional transient computer simulations. These simulations should include the energy dissipated in the external circuit during switching, and hence a specific load circuit must be assumed.
2. Determine the dependence of on-state power P_{ON} on J_{ON} using two-dimensional steady-state computer simulations and obtain a value for P_{OFF} at the assumed blocking voltage.
3. For a given switching frequency f, adjust J_{ON} using Equation 7.17 until the total power dissipation P_{TOTAL} equals 300 W cm^{-2}. The resulting current is the desired figure of merit J_{300} for that particular blocking voltage and switching frequency.

This procedure has been used to compare the performance of power MOSFETs and IGBTs at blocking voltages of 15 and 20 kV [14, 15] and will serve as an example of the technique. First, an n-channel DMOSFET and a p-channel DMOS IGBT were individually optimized for the desired blocking voltage, 15 or 20 kV, using computer simulations. The on-state I–V characteristics of the 20 kV devices are shown in Figure 10.33 at two temperatures, 27 and 175 °C. The I–V characteristics of the IGBT are

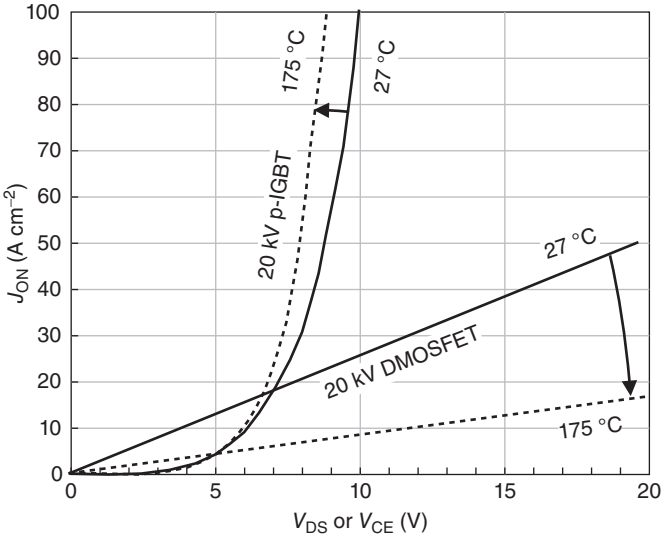


Figure 10.33 Current–voltage characteristics at 27 °C and 175 °C of an optimized DMOSFET and an optimized p-channel IGBT designed to block 20 kV ([15] reproduced with permission from Trans Tech Publications).

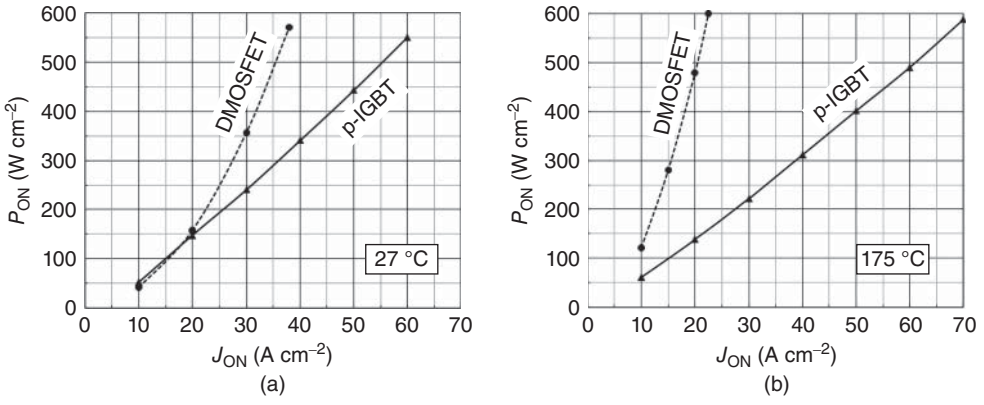


Figure 10.34 On-state power dissipation of the DMOSFET and IGBT of Figure 10.33 as a function of on-state current density, (a) at 27 °C and (b) at 175 °C ([14] reproduced with permission from Tomohiro Tamaki).

nonlinear, and cannot be represented by an on-resistance. The MOSFET I-V characteristics are linear, but the on-resistance degrades with temperature due to the decrease in mobility with temperature shown in Figure 10.26. In contrast, the IGBT is relatively insensitive to temperature. This is because the ambipolar diffusion length depends on both the diffusion coefficient and the lifetime. As shown in Figure 9.26, the lifetime increases faster with temperature than the diffusion coefficient decreases, and the diffusion length increases slightly with temperature, improving device performance.

The on-state power $P_{ON} = J_{ON}V_{DS}$ or $P_{ON} = J_{ON}V_{CE}$ can be calculated at any J_{ON} directly from Figure 10.33, and is plotted as a function of current in Figure 10.34. The switching energy is obtained as a function of on-current from transient simulations using a clamped inductive load (modeled by a current source of magnitude J_{ON}), and the resulting E_{SW} is plotted as a function of current in Figure 10.35. These plots are used in conjunction with Equation 7.17 to determine the J_{ON} that corresponds to a total power dissipation of 300 W cm^{-2}. This is the desired figure of merit J_{300}. Figure 10.36 shows J_{300} for each device as a function of switching frequency. We observe that at low switching frequencies, the IGBT provides higher current than the MOSFET. This is due to conductivity modulation of the drift region,

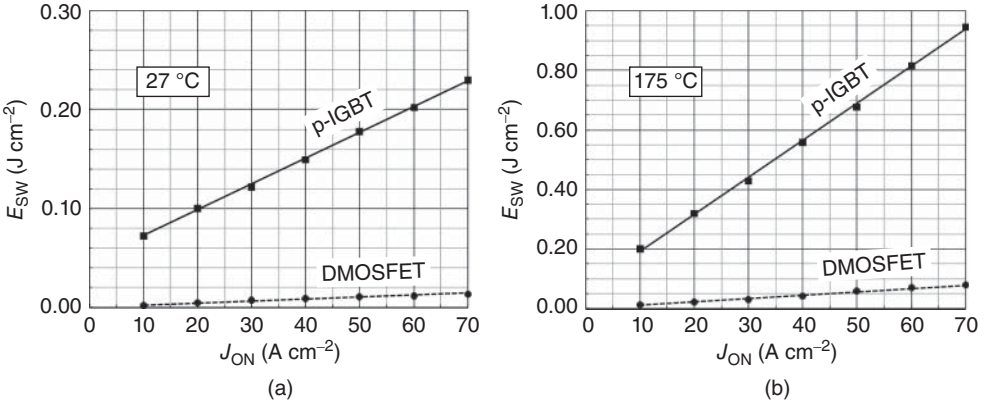


Figure 10.35 Switching energy of the DMOSFET and IGBT of Figure 10.33 as a function of on-state current density, as obtained from two-dimensional transient simulations using a clamped inductive load, (a) at 27 °C and (b) at 175 °C ([14] reproduced with permission from Tomohiro Tamaki).

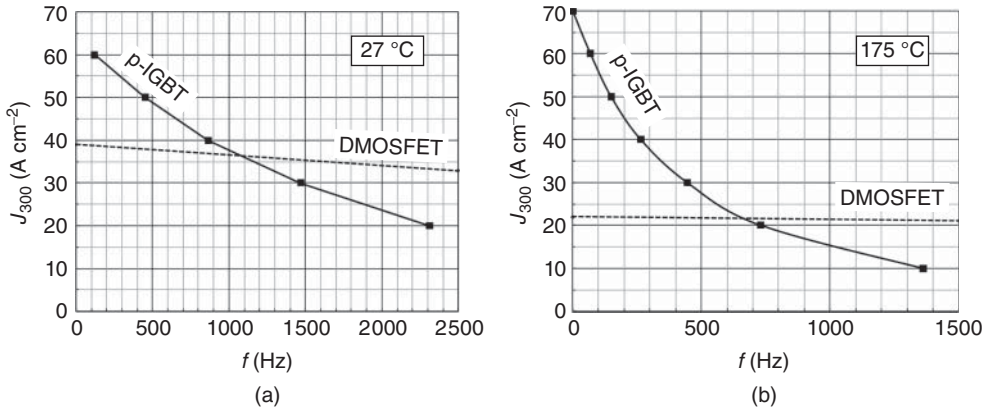


Figure 10.36 Current density of the DMOSFET and IGBT of Figure 10.33 assuming a total power dissipation of 300 W cm^{-2}, plotted as a function of switching frequency, (a) at 27 °C and (b) at 175 °C ([13] reproduced with permission from Tomohiro Tamaki).

which reduces the forward voltage drop at high currents, as seen in Figure 10.33. However, the minority carriers that provide the conductivity modulation must be removed during each turn-off event, and the reverse current transient gives rise to a power dissipation that is proportional to frequency. As frequency is raised, the on-current J_{ON} must be reduced to keep the total power dissipation below 300 W cm^{-2}, and at higher switching frequencies the on-current of the IGBT falls below that of the MOSFET. Thus the MOSFET is the preferred device for high-frequency applications, while the IGBT is superior at low frequencies.

The methodology above can be used to compare bipolar or unipolar devices for any desired blocking voltage and switching frequency. In general, bipolar devices perform better at high blocking voltages and low frequencies, while unipolar devices are superior at low blocking voltages and high frequencies. However, at sufficiently low blocking voltages, MOSFETs and JFETs are superior to IGBTs and thyristors, regardless of the frequency. Why is this? There are two reasons. First, at low blocking voltages the drift region resistance is relatively small, and does not need to be reduced by conductivity modulation. Second, IGBTs and thyristors have an odd number of pn junctions in their current paths. When all junctions are forward biased, a net voltage drop of one forward-biased diode appears in series with the remainder of the device. This adds an additional component to the static power dissipation of the IGBT and thyristor. (In contrast, the BJT has an even number of junctions in its current path, and the voltage drops of two oppositely-directed junctions cancel out.)

At sufficiently high frequencies, unipolar devices are superior at all blocking voltages, as seen in the comparison of pin and Schottky diodes in Figure 7.9. This is because the switching loss of bipolar devices is proportional to frequency and becomes the dominant loss at high frequencies, forcing a continuous reduction in J_{ON} to keep P_{TOTAL} below 300 W cm^{-2}.

In all comparisons involving power devices, it is important to consider both high and low temperature extremes, since device performance is sensitive to temperature. A device dissipating 300 W cm^{-2} will have a junction temperature well above ambient. For this reason, analyses performed only at room temperature provide an incomplete picture of device performance.

References

[1] Konstantinov, A.O., Wahab, Q., Nordell, N. and Lindefelt, U. (1997) Ionization rates and critical fields in 4H silicon carbide. *Appl. Phys. Lett.*, **71** (1), 90–92.

[2] Morisette, D.T. (2001) Development of robust power Schottky barrier diodes in silicon carbide. PhD thesis. Purdue University.
[3] Loh, W.S., David, J.P.R., Ng, B.K. *et al.* (2009) Temperature dependence of hole impact ionization coefficient in 4H-SiC photodiodes. *Mater. Sci. Forum*, **615–617**, 311–314.
[4] Konstantinov, A.O., Nordell, N., Wahab, Q. and Lindefelt, U. (1998) Temperature dependence of avalanche breakdown for epitaxial diodes in 4H-silicon carbide. *Appl. Phys. Lett.*, **73** (13), 1850–1852.
[5] Davies, R.L. and Gentry, F.E. (1964) Control of electric field at the surface of p-n junctions. *IEEE Trans. Electron. Devices*, **11** (7), 313–323.
[6] Adler, M.S. and Temple, V.K. (1978) Maximum surface and bulk electric fields at breakdown for planar and beveled devices. *IEEE Trans. Electron. Devices*, **25** (10), 1266–1270.
[7] Temple, V.A.K. (1977) Junction termination extension (JTE): a new technique for increasing avalanche breakdown voltage and controlling surface electric fields in p-n junctions. International Electron Devices Meeting Technical Digest, pp. 423–426.
[8] Khan, I.A. (2002) High voltage SiC MOSFETs. PhD thesis. Purdue University.
[9] Wang, X. and Cooper, J.A. (2004) Optimization of JTE edge termination for 10 kV power devices in 4H-SiC. *Mater. Sci. Forum*, **457–460**, 1257–1262.
[10] Singh, S., Tjandra, E. and Cooper, J. A. (2003) High-voltage termination of SiC devices using floating field rings. unpublished, reproduced with permission from James A. Cooper.
[11] Sung, W., Van Brunt, E., Baliga, B.J. and Huang, A.Q. (2011) A new edge termination technique for high-voltage devices in 4H-SiC-multiple-floating-zone junction termination extension. *IEEE Electron. Device Lett.*, **32** (7), 880–882.
[12] Feng, G., Suda, J. and Kimoto, T. (2012) Space-modulated junction termination extension for ultra-high voltage p-i-n diodes in 4H-SiC. *IEEE Trans. Electron. Devices*, **59** (2), 414–418.
[13] Appels, J.A. and Vaes, H.M.J. (1979) High voltage thin layer devices (RESURF) devices. IEEE International Electron Devices Meeting Technical Digest, pp. 238–241.
[14] Tamaki, T., Walden, G. G., Sui, Y., and Cooper, J. A. (2007) On-state and switching performance of high-voltage 4H-SiC DMOSFETs and IGBTs. International Conference on Silicon Carbide and Related Materials, Otsu, Japan.
[15] Tamaki, T., Walden, G.G., Sui, Y. and Cooper, J.A. (2009) On-state and switching performance of high-voltage 4H-SiC DMOSFETs and IGBTs. *Mater. Sci. Forum*, **600–603**, 1143–1146.