SiC MOSFET-Based Power Module Design and Analysis for EV Traction Systems

Emre Gurpinar, Randy Wiles,
Burak Ozpineci, and Tsarafidy Raminosoa
Power Electronic and Electric Machinery Group
Oak Ridge National Laboratory
Knoxville, TN 37932 USA
email: gurpinare@ornl.gov

Feng Zhou, Yanghe Liu, and Ercan M. Dede
Toyota Research Institute of North America
Ann Arbor, MI 48105 USA
email: feng.zhou@toyota.com

***Abstract*—Wide bandgap (WBG) power semiconductor devices, specifically silicon carbide (SiC) metal-oxide-semiconductor field-effect transistors (MOSFETs) have gained attention from electric vehicle (EV) system developers due to well-known superior properties in comparison to industry standard silicon (Si) based MOSFETs and insulated-gate bipolar transistors (IGBTs). In this work, a power module design based on SiC MOSFETs in a segmented two-level, three-phase inverter topology with 125 kW peak output power and 30 kHz switching frequency is presented. Three different SiC MOSFET die options are analyzed according to experimentally obtained operating conditions of a commercial EV traction system. Substrate design of the power module for multi-die layout, heat sink design, and integration of a segmented phase leg module are presented. Finite-element electrical and thermal analysis of the proposed system are presented and discussed.**

***Index terms*—** Wide bandgap power devices, electric vehicles, SiC MOSFET, segmented inverter, traction systems.

I. Introduction

Wide bandgap-based power semiconductor devices, specifically SiC MOSFETs and gallium nitride (GaN) high-electron-mobility transistors (HEMTs) have gained attention from the automotive industry due to well-known superior properties in comparison to conventional Si-based MOSFETs and IGBTs. Si-based MOSFETs provide high switching speeds due to a unipolar conduction mechanism, but they suffer from high conduction losses due to an increase in on-state resistance at high blocking voltage class (i.e. above 600 V) from an absence of minority carriers [1], [2]. Consequently, Si IGBTs gained popularity since they exhibit excellent conduction performance through a bipolar conduction mechanism despite the penalty of reduced switching speed due to minority carrier existence in the device channel. The superior performance of SiC MOSFETs and GaN HEMTs at 600 V blocking class, and SiC MOSFETs at 1200 V blocking class, has been discussed thoroughly in literature [3], [4].

SiC MOSFETs have gained attention from EV system developers due to the maturity of the technology in comparison to GaN-based devices, and various papers have been published that show the benefits of using SiC MOSFETs for traction and wireless charging applications [5], [6]. It is shown that SiC devices can provide higher performance in comparison to Si devices over a wide temperature and switching frequency range, which leads to a reduction in system cooling and filtering requirements. The system weight and volume reduction opportunities in EV applications provide significant benefits in terms of range extension, and researchers have been focusing on introducing new power electronic converter topologies, power devices, motor topologies and system architectures to advance EV adoption. As the WBG devices and associated EV systems have not matured yet, the benefits of these devices when coupled with novel topologies for EV systems must be investigated. In this paper, a SiC MOSFET-based power module design and analysis for a segmented two-level three-phase inverter is presented.

II. Segmented Two-Level Three-Phase Inverter and System Overview

The standard two-level, three-phase inverter architecture, which is commonly used for permanent magnet (PM) traction motor applications, requires a bulky DC link capacitor to absorb the large ripple current caused by the pulse width modulation (PWM) operation. To reduce the filtering requirements at the DC link, a segmented topology is presented by Su et al. in [7], which can reduce the DC link capacitor up to 60% without increasing the total semiconductor area. The schematic of the proposed segmented three-phase topology with SiC MOSFETs is presented in Fig. 1. The segmented phase legs are modulated with sinusoidal PWM signals, where the same reference signal and 180° phase shifted carrier signals are used for the segmented legs in each phase. While the fundamental voltage waveforms generated by segmented phase legs are identical, and the total phase current is identical to the phase current in a non-segmented configuration. Due to interleaved phase legs, the RMS DC link ripple current in segmented

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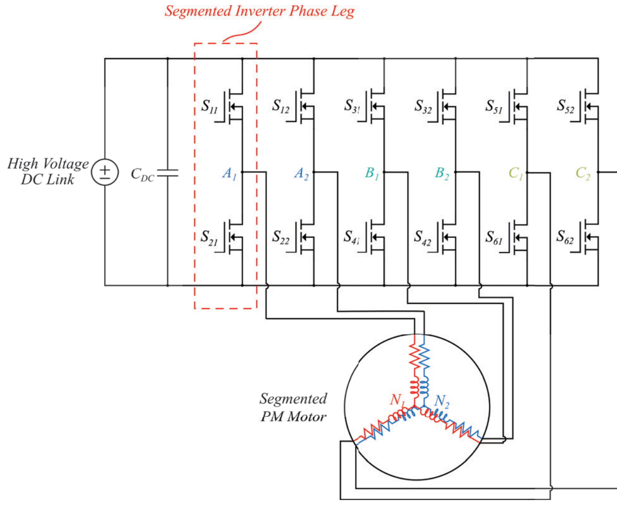


Fig. 1: Segmented two-level three-phase inverter with permanent magnet (PM) traction motor in EV systems.

TABLE I: BEV Traction System Parameters

Peak Power $P_{OUT_{pk}}$	125 kW
DC Link Voltage V_{DC}	360 V
Maximum Torque T_{max}	250 Nm
Inverter Topology	Two-level three-phase
Switching Frequency f_{sw}	5 kHz
Power Module	Infineon FS800R07A2E3
DC Link Capacitor C_{DC}	475 μF, 450 V
IGBT Collector Emitter Voltage V_{CE}	650 V
IGBT Collector Current I_C	550 A @ T_C=75 °C
Diode Forward Current I_F	550 A @ T_C=75 °C
Motor and Inverter Cooling	% 50 water, % 50 ethylene-glycol liquid cooling

configuration is significantly smaller than in the conventional two level system.

Various commercial EVs have been benchmarked over the last years by research institutions, and representative benchmarking results can be found in [8] and [9]. Among the benchmarked systems, one battery EV (BEV) system, which has the highest peak power density [kW/L] and specific power density [kW/kg] for the motor and inverter, is selected as a suitable candidate to evaluate the benefits of a segmented two-level three-phase topology coupled with SiC MOSFETs. The traction system parameters of the selected commercial BEV, which uses a commercial Si IGBT and Si diode based three phase inverter power module, are presented in Table I. The peak power rating of the system is 125 kW, with 250 Nm maximum torque capability. The motor and the inverter are cooled with a series connected liquid cooling system. In the commercial BEV inverter, Si IGBT and Si diodes are used for the inverter and the switching frequency is set to 5 kHz. In the SiC MOSFET based design, the switching frequency is selected as 30 kHz. In [10], it is shown that an increase in switching frequency does not compromise the efficiency of the inverter, can provide improved control bandwidth, and allows higher speed operation of the traction system.

III. Phase Leg Module Design for Segmented Inverter

The system parameters in Table I are used to determine the current and voltage rating of the switches in the designed inverter with a given DC link voltage of 360 V. SiC MOSFET dies without external anti-parallel SiC Schottky barrier diodes (SBDs) from two different manufacturers with 650 V and 900 V drain-source blocking ratings are considered for the segmented phase leg module design. In [11], it is shown that elimination of external anti-parallel diodes leads to a reduction in system complexity and component count in voltage source inverters without compromising efficiency. Potential SiC MOSFET bare dies with key parameters are presented in Table II. The number of parallel dies for each die option has been selected to reach approximately 6 mΩ on-state resistance for each switch at 125 °C case temperature in a segmented leg shown in Fig. 1. To select the optimum die from Table II, a semiconductor loss analysis has been performed to estimate the inverter loss and distinguish the difference in switching versus conduction losses [10]. In this analysis, the dead-time between complementary switches is selected as 1 μs, and the switching frequency of the inverter is selected as 30 kHz.

The experimental data from the characterization of the PM motor such as phase current, motor torque, motor speed, and inverter output power are used as the input parameters for the loss analysis. The loading of the inverter is proportional to the output torque of the motor. To determine the maximum semiconductor power loss in the segmented inverter with the bare die options presented in Table II, the maximum torque region of the traction system is selected as as the maximum loading region of the inverter.

The conduction, switching, and total semiconductor losses with three different dies at 30 kHz switching frequency are presented in Figs. 2 and 3, respectively. In Fig. 2, it is shown that dies A and B provide lower conduction loss in comparison to die C. However, from Fig. 3, it can be seen that the increase in conduction loss with die C may be compensated by lower switching loss in comparison to dies A and B. At given operating conditions, the margin gained by lower switching loss with die C is not enough to compensate the increased conduction losses. According to Fig. 3, die B provides the lowest semiconductor losses, however the number of parallel dies per switch is higher than the die A and die C options.

TABLE II: SiC MOSFET Die Parameters

	Die A	Die B	Die C
V_{DS}	650 V	650 V	900 V
R_{DS} @ T_C=25 ^{o}C	22 mΩ	30 mΩ	10 mΩ
R_{DS} @ T_C=125 ^{o}C	29 mΩ	40 mΩ	12 mΩ
I_{DS} @ T_C=125 ^{o}C	65 A	49 A	140 A
E_{ON} @ T_C=25 ^{o}C	252 μJ @ I_{DS}= 36 A	168 μJ @ I_{DS}= 27 A	1.35 mJ @ I_{DS}= 100 A
E_{OFF} @ T_C=25 ^{o}C	201 μJ @ I_{DS}= 36 A	112 μJ @ I_{DS}= 27 A	0.83 mJ @ I_{DS}= 100 A
Number of parallel dies for $R_{DS_{11,21}} \approx 6$ mΩ @ T_C=125 °C	5	7	2

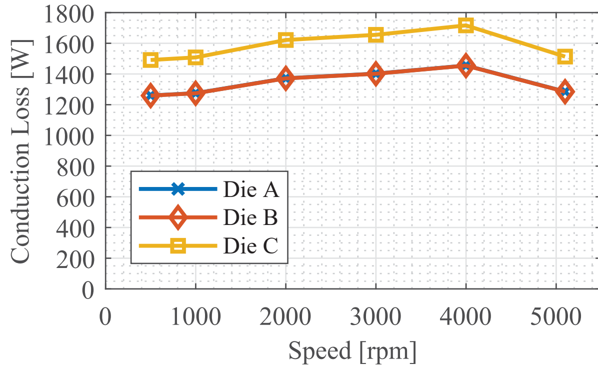


Fig. 2: Conduction loss of the segmented inverter at 30 kHz switching frequency.

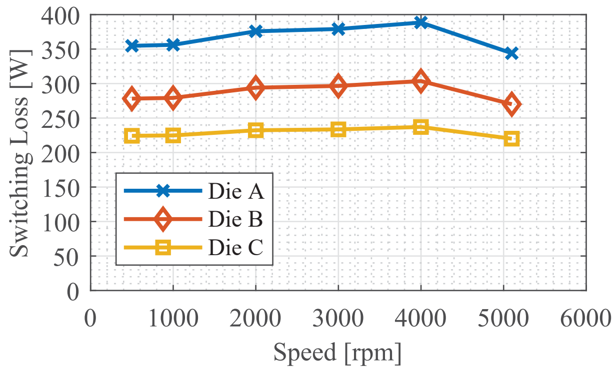


Fig. 3: Switching loss of the segmented inverter at 30 kHz switching frequency.

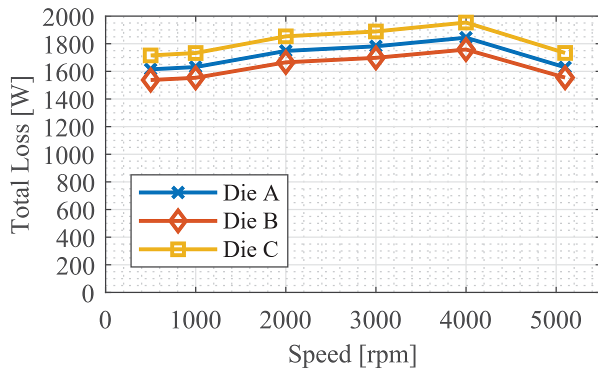


Fig. 4: Total semiconductor loss of the segmented inverter at 30 kHz switching frequency.

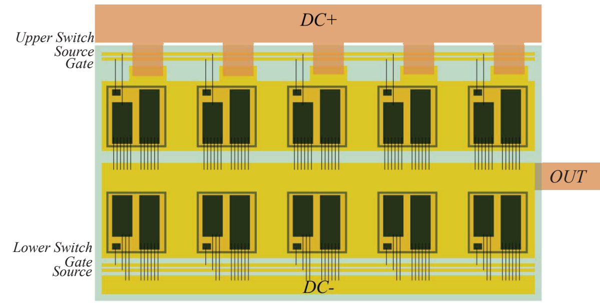


Fig. 5: SiC MOSFET based DBC substrate design for segmented two-level inverter.

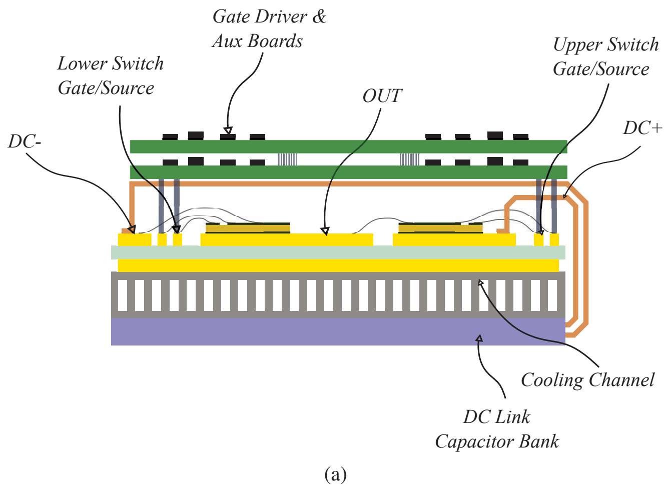
Taking into consideration the number of parallel dies per switch, total semiconductor loss, and distribution of power loss in the module to avoid thermal hot spots, die A is selected as the optimum die for this study.

A. Module Design

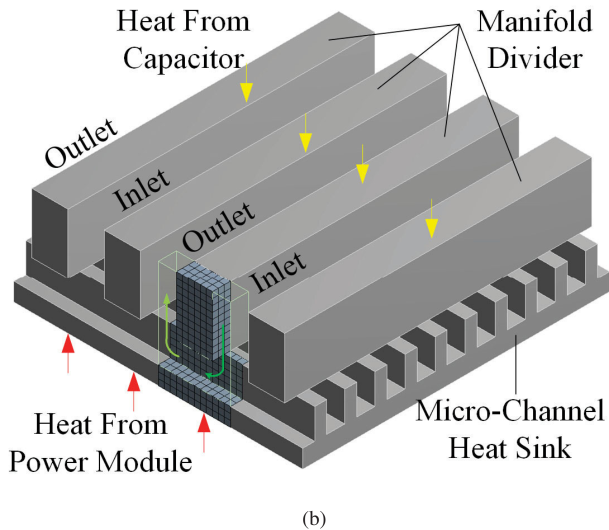
Based on the SiC MOSFET die selection outlined in the previous section, five parallel dies are used for each switch in the segmented inverter to meet the required current rating of the system. The direct bonded copper (DBC) substrate layout of the phase leg with die A is presented in Fig. 5. Parallel dies for each switch are placed symmetrically on the DBC with respect to DC+ and DC- terminals to achieve equal current distribution among dies during fast switching transients. Aluminum wire bonds are used as signal and power interconnects between gate and source pads of the SiC MOSFET dies and copper on DBC. Furthermore, Kelvin connection is used for the upper and lower switches for the gate driver connection for high speed switching capability.

B. Heat Sink Design

Manifold microchannel (MMC) heat sink technology [12] is used to cool both the SiC power module and associated capacitor in a novel double-side configuration. The manifold of a conventional MMC heat sink typically does not participate in the general heat transfer process. However, is this study, the manifold is considered to be made of a high thermal conductivity material and is exploited in the dual-sided heat sink design. As shown in Fig. 6a, the cold plate is sandwiched between the two heat sources, and the internal cooling structure of the MMC structure is shown in Fig. 6b. Here, the micro-channel side of the heat sink has higher cooling performance due to larger surface area that is exploited to cool the power module. The coarser macro-channel structure on the manifold side of the heat sink is then utilized to cool the capacitor, which has relatively low heat density. This unique dual-sided cooling strategy provides a good balance between disparate cooling requirements and system compactness.



(a)



(b)

Fig. 6: (a) Cold plate sandwiched between single sided module and DC link capacitor, (b) Internal cooling structure of manifold micro-channel cold plate; note: the upper cap layer of the manifold side of the heat sink is not shown, for clarity.

IV. Electrical and Thermal Analysis of the Segmented Inverter Phase Leg

Finite-element electrical and thermal analyses of the designed module are conducted to verify the expected performance. The final configuration of the module including DC link busbars, DC link capacitors, heat sink, and substrate is shown in Fig. 7. Two Ceralink capacitors (B58033I5206M001) with solder pin configuration are placed at the bottom (manifold) side of the heat sink. The capacitor terminals are connected to the substrate DC+ and DC- terminals via overlapped copper busbars. The DC- busbar is shown as transparent to show the components underneath the busbar. The overlapped busbar layout for DC link connection creates a vertical commutation loop with magnetic field cancellation throughout the busbar and over the substrate to achieve low commutation loop inductance. The top side of the capacitors are utilized for heat transfer from the capacitors to the heat sink manifold to enhance ripple current capability at increased ambient temperature conditions.

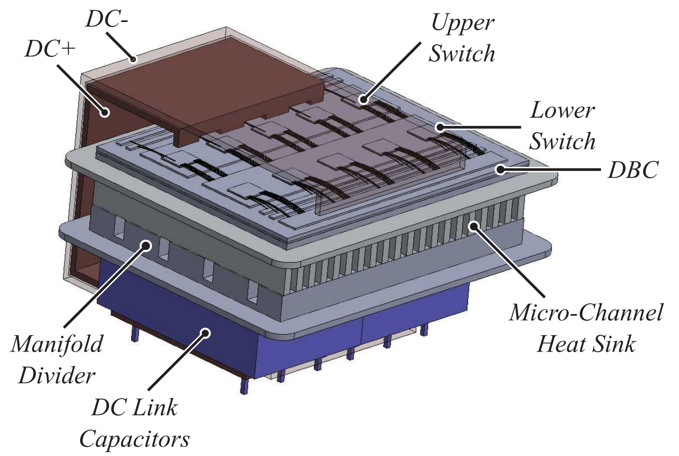


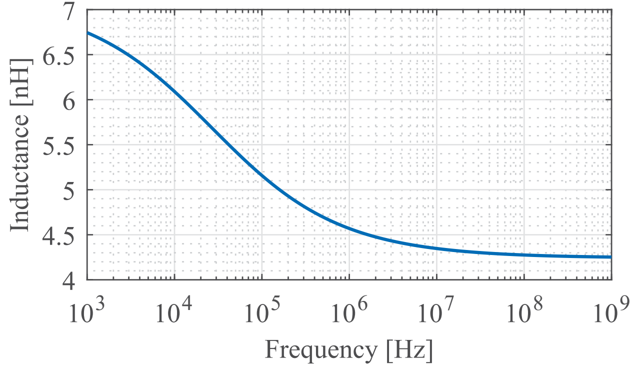
Fig. 7: Segmented inverter phase leg design.

A. Electrical Analysis

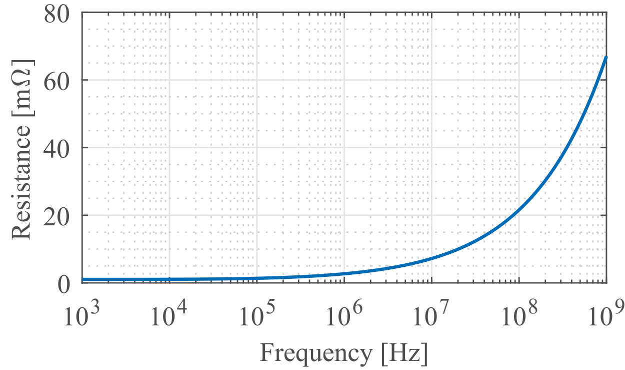
The electrical analysis of the commutation loop in the module is conducted with Ansoft Q3D extractor to solve the parasitic inductance and resistance values, which have significant effects on the switching performance of the power semiconductor devices. The analysis results for stray inductance and resistance of the commutation loop in the module with respect to frequency are presented in Figs. 8a and 8b, respectively. Typical commutation time between SiC MOSFETs is between 100 ns and 10 ns, which correspond to a frequency range between 10 MHz and 100 MHz for the parasitic component analysis, per [3]. Observe in Figs. 8a and 8b that the commutation loop inductance is below 4.5 nH and the resistance is below 20 mΩ in the given frequency range. The inductance value does not include the capacitor package inductance (3.5 nH according to the data sheet), and the resistance value does not include the SiC MOSFET on-state resistance (6 mΩ per switch).

B. Power Module Thermal Analysis

A steady-state conduction heat transfer finite element model is built in ANSYS for the power module with a heat transfer coefficient (HTC), h, value uniformly applied at the back side of the module. Figure 9a depicts the effect of the applied h value on the maximum device temperature with different assumed thermal conductivity values, 40-130 W/mK, assigned to the thermal interface material (TIM) layer between the chip and DBC substrate. The h value is swept from 2,000 to 20,000 W/m^{2}K. It is found that a h value of $\sim$10,000 W/m^{2}K is sufficient to cool the device to a target temperature of 110 °C; see Fig 9a. Following this initial modeling effort, a conjugate heat transfer unit cell model for parametric study,

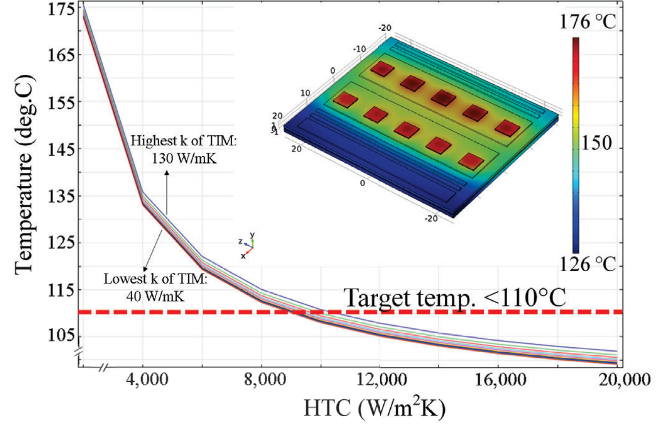


(a)

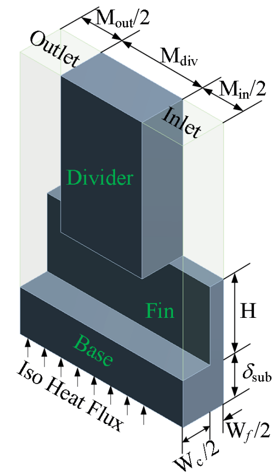


(b)

Fig. 8: Finite element analysis of: (a) stray inductance and (b) resistance of the commutation loop in the designed module.



(a)



(b)

Fig. 9: (a) Power module steady-state conduction heat transfer model, (b) Cooling structure of manifold micro-channel cold plate unit cell model.

see Fig. 9b, is developed using commercial computational fluid dynamics (CFD) software to determine the geometry of the MMC heat sink that satisfies the more stringent power module side cooling requirement. A uniform heat flux, 15.3 W/cm^2, from the power module was assumed and applied to the bottom micro-channel side of the heat sink. The total volumetric flow rate of the coolant (taken as 50/50 water/ethylene-glycol at a 65 °C inlet temperature) is 10 l/min evenly split between six power modules, and a zero-pressure boundary condition is set at the outlet. The investigated parameters include, as shown in Fig. 9b, the heat sink channel width, W_c, channel height, H, fin thickness, W_f, width of the manifold inlet and outlet branch, M_{in} and M_{out}, and width of the manifold divider, M_{div}. With $M_{in} = 2$ mm, $M_{out} = 4$mm and $M_{div} = 10.3$ mm, there are three pairs of inlet/outlet branches in total, and a heat sink with $W_c = W_f = 0.5$ mm, $H = 6$ mm can provide a h value of 12,300 W/m^{2}K, which meets the cooling requirement with ∼20% margin. Halving the heat sink channel width and fin thickness bumps up the h value to 20,500 W/m^{2}K. The pressure drop through the unit cell is negligibly low, less than 200 Pa, due to the advantage of manifold structure; the reader is referred to [12] for additional details. An additional benefit of this design is that the number of manifold inlet/outlet branches may be revised up or down depending on the additional capacitor cooling requirement.

V. Conclusion

In this work, a power module design based on SiC MOSFETs in a segmented two-level, three-phase inverter topology with 125 kW peak output power and 30 kHz switching frequency is presented. Three different SiC MOSFET die options are analyzed according to experimentally obtained operating conditions of a commercial EV traction system. Substrate design of the power module for symmetrical multi-die layout with vertical commutation loop, micro-channel heat sink design for substrate and capacitor cooling, and integration of a segmented phase leg module are presented. Finite-element electrical and thermal analyses of the proposed system are presented and discussed. The analyses results show high electrical and thermal performance have been achieved for maximum utilization of WBG devices. As part of future

work, the designed power module will be constructed and tested under rated operating conductions.

VI. Acknowledgment

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