SiC MOSFET Double Pulse Fixture

This article describes a double pulse test fixture that is suitable for the characterization of SiC MOSFETs. The setup is a text book double pulse tester with all critical components placed on a single printed circuit board to afford repeatable measurements. A photograph of the test fixture is shown in Figure 1.

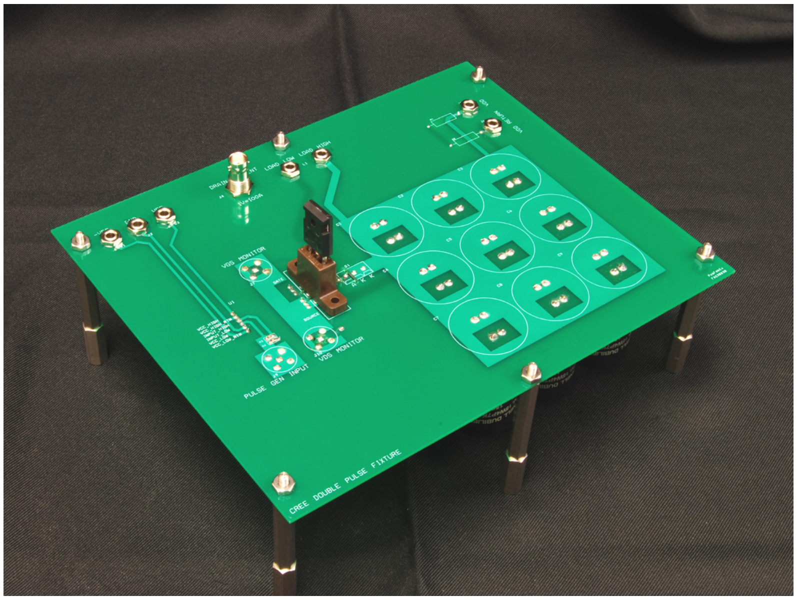

Figure 1: SiC MOSFET Double Pulse Tester

A schematic of the tester is shown in Figure 2. The test fixture contains a test socket for the MOSFET (J6), gate driver (U1), capacitor bank (C1-C9), freewheeling diode (D1), and a tightly integrated two stage current transformer (T1). VDS and VGS can be monitored via BNC connectors (J7 & J10). The intent of these connectors is not to use coaxial cable, but to use a coaxial cable to probe adapter to avoid the need for a probe ground clip. This eliminates the parasitic inductance of the ground clip wire from corrupting the voltage measurement. Drain current is measured using a two stage current transformer consisting of a small 1:10 ferrite first stage transformer and a Pearson Electronics model 2878 current monitor for the second stage. The resulting scale factor is 1V=100A. Nine polypropylene film capacitors (C1-C9) are used to provide a low inductance voltage source for the tester. VCC, GND, and –VEE are the input voltage for the gate driver. VCC sets the value for the gate pulse high voltage and –VEE sets the value for the gate pulse low voltage. Maximum voltage between VCC and –VEE is 30V. The drive pulse is applied to the Pulse Generator Input BNC connector. A pulse of +10 to +12V is recommended to turn on the gate pulse. This input is terminated in 50 Ω to match into a 50 Ω coaxial cable. The termination resistors (R3 and R4) have an overall rating of 0.5W maximum so the input pulse duty cycle must be appropriately limited (~10%) to avoid burning them out. The inductor is connected across the LOAD LOW and LOAD HIGH terminals. A recommended inductor value is about 850 μH. This can be realized as an air core inductor constructed by placing a single layer of 107 turns of AWG 18 magnet wire on a length of 4″ schedule 40 PVC pipe (OD = 4.5″).

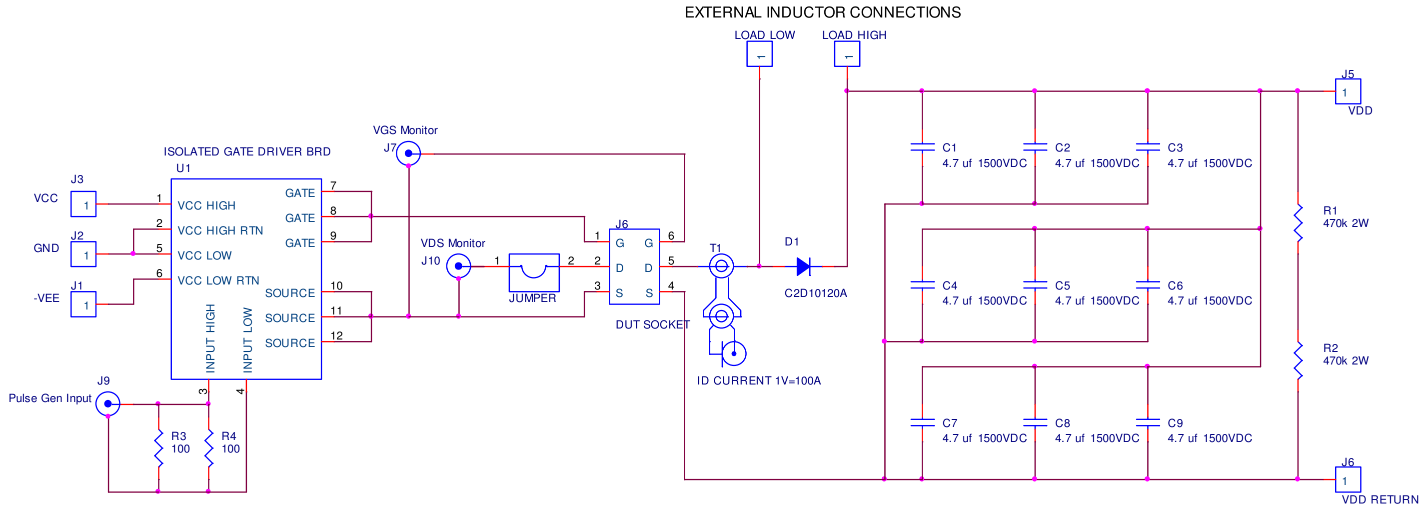

Figure 2: SiC MOSFET Double Pulse Tester Schematic

A photograph of the top of the tester is shown in Figure 3. The option exists of mounting the BNC connectors on the top or the bottom of the board. In this case, the BNC connectors are mounted on the back side to allow a ThermoStream head to be placed over the device under test. (*Please note when installing the BNC connectors on the back side, do not mount the connectors flush to the PCB as a short may result, use a temporary spacer to assist in the installation*). All power connections are made using banana plugs and can be inserted from the top or bottom side of the board.

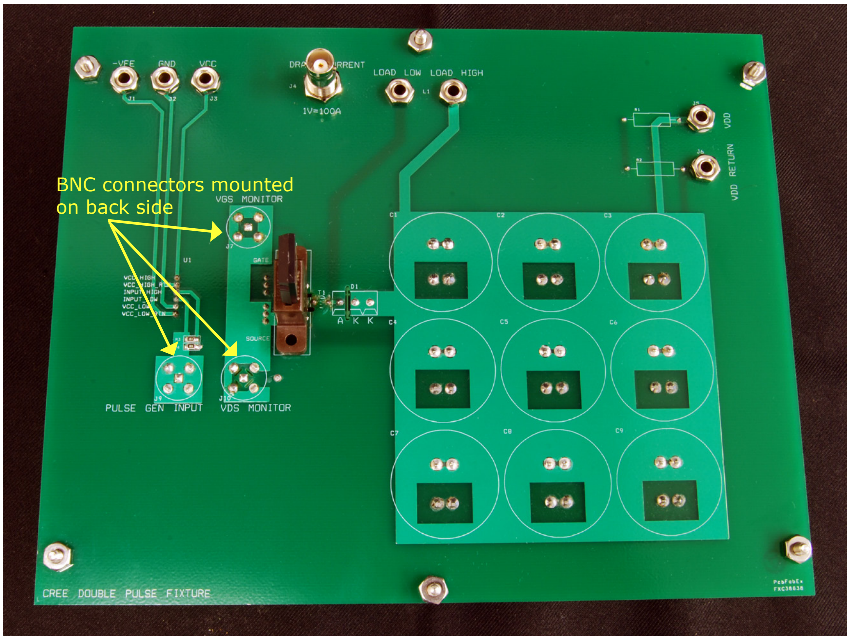

Figure 3: SiC MOSFET Double Pulse Tester Top View

The bottom side of the tester is shown in Figure 4. Most of the board components are mounted on the back of the board. D1 is installed in a terminal block so it can be removed and replaced with a resistor for probe de-skewing. The jumper shown is the jumper identified in the schematic and is used for the center pin of the VDS BNC connector. Notice that the gate driver board is mounted bottom side up. The two stage current transformer (T1) is mounted on the bottom. The output of the Pearson current monitor is connected to a SMA-SMA adapter and then to a SMA to BNC bulkhead adapter that feeds through to the top side.

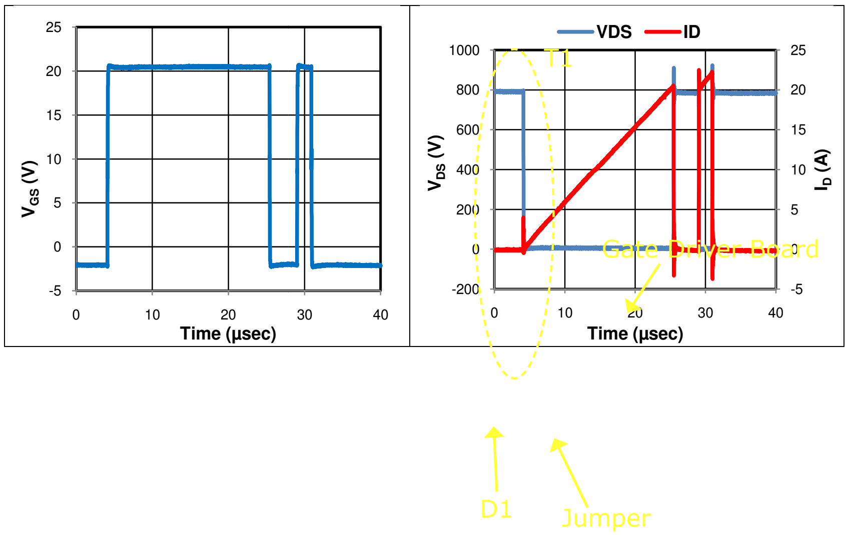

Figure 4: SiC MOSFET Double Pulse Tester Bottom View

A detailed view of the first stage current transformer is shown in Figure 5. The transformer consists of 10 turns of AWG 26 solid copper Teflon insulated wire wound around a Ferroxcube TC9.5/4.8/3.2-3E27 ferrite toroid. The center conductor is heavily insulated AWG 22 bus wire suitable for 1.5 kV tests. Figure 6 shows the gate driver board. This board is a modified version of the isolated gate driver board described in the "SiC Isolated Gate Driver" Application Note CPWR-AN10. The board is modified to bypass the DC-DC converters to allow a direct connection to the gate drive power supplies. Notice that the headers are mounted on the top side of the board to allow the board to be mounted bottom side up.

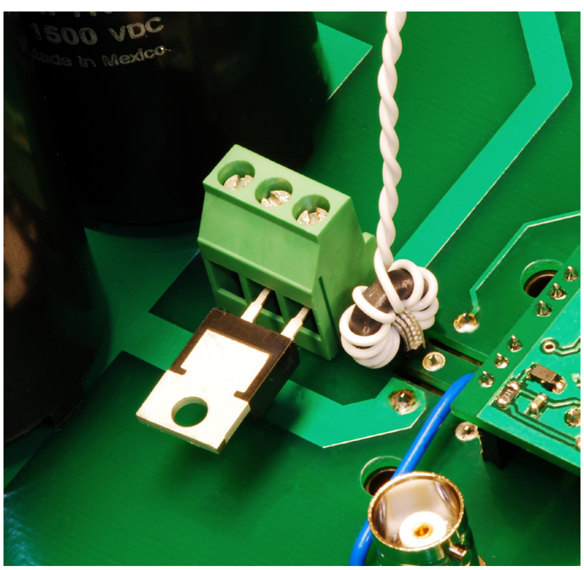

Figure 5: T1 First Stage Detail

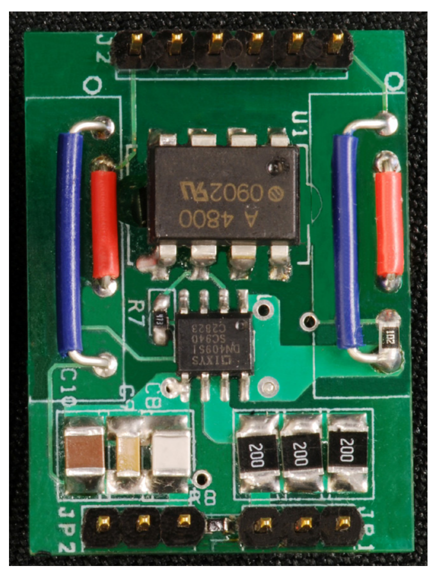

Figure 6: Isolated Gate Driver Board with DC-DC Converters Removed and Bypassed

For accurate measurements, it is very important to de-skew the voltage and current probes to insure that all of the delays are the same. Deskewing the voltage probes is easily done by attaching both probes to a pulse generator output and adjusting the channel deskew on the oscilloscope so that both pulses are time synchronized. Deskewing the VDS and ID probes can be achieved by removing the inductor and replacing diode D1 with a low inductance 100 Ω resistor. A Caddock MP930-100-1% or equivalent resistor is recommended. Care must be taken during the deskew process to insure that VDD is set to a level below the maximum pulse rating of the resistor. The maximum value for the aforementioned resistor is 250V.

A sample waveform of the double pulse gate drive is shown in Figure 7. The corresponding sample waveforms of the MOSFET VDS and ID are shown in Figure 8. The pulse train consists of two pulses with a repetition frequency of about 1-2 Hz. The first pulse (~ 22 µsec) is used to build up the current in the inductor. The width is adjusted for the desired test current. When this pulse is terminated, ID commutates from the MOSFET to the freewheeling diode. This transition is used to measure the MOSFET turn-off characteristics. There is a delay of about 3 µsec between the first and second pulse. The duration of this delay is set long enough for the voltage and currents to settle out and might need to be increased if this test fixture is used to evaluate Si IGBTs to insure adequate time for the tail current to settle out. The second narrow pulse (~ 2 µsec) occurs a few microseconds later. Current is commutated from the freewheeling diode back into the MOSFET during this transition and MOSFET turn-on characteristics are measured at this point.

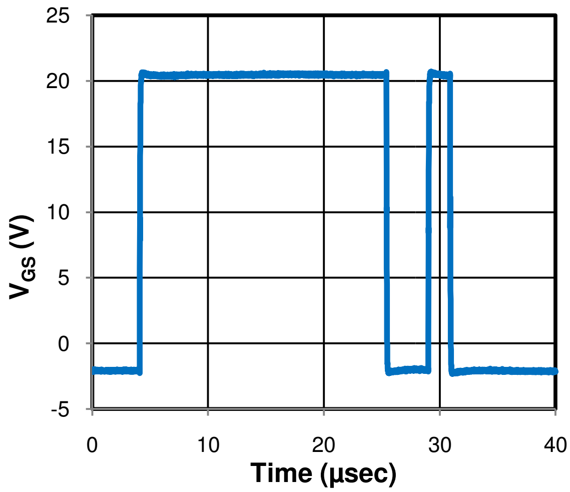

Figure 7: Sample Gate Drive Pulse

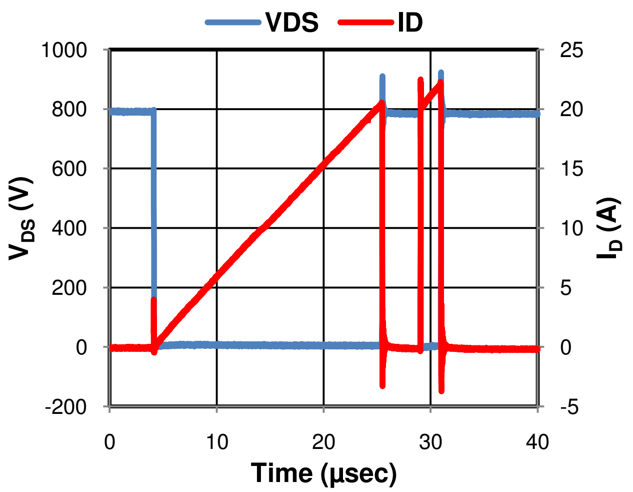

Figure 8: Sample Waveforms

Sample waveforms of VDS and ID at turn-on are shown in Figure 9. Notice the very small amount of current overshoot during turn-on. This is due to the very low amount of stored charge in the SiC JBS diode as compared with a high speed silicon PiN diode. Sample waveforms of VDS and ID at turn-off are shown in Figure 10. Ringing is observed in both VDS and ID that usually is not observed with silicon IGBTs. This is due to the SiC MOSFET's lack of a current tail.

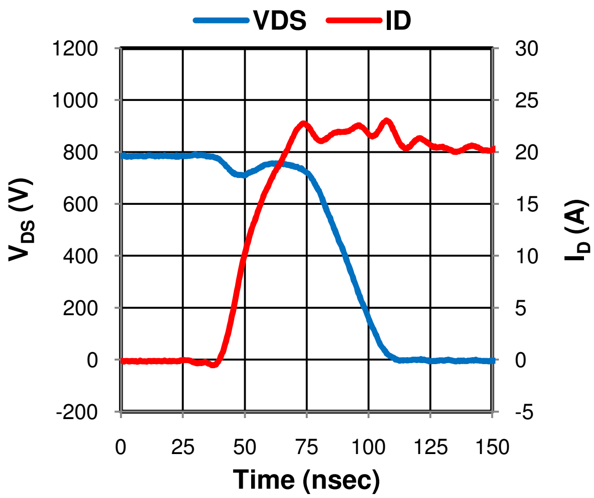

Figure 9: Turn-On Waveforms

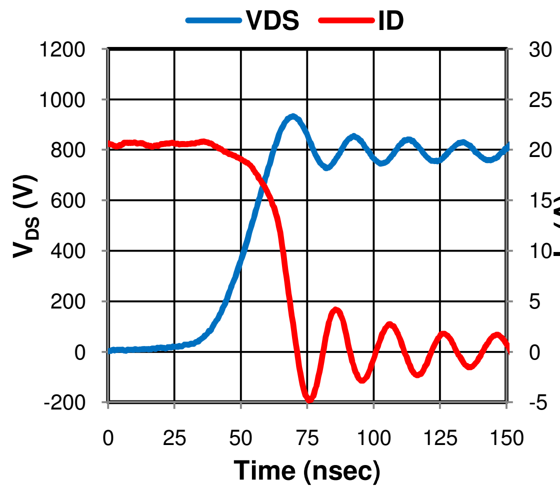

Figure 10: Turn-Off Waveforms

The ringing is caused by the output capacitance of the SiC MOSFET resonating with the stray inductance in the high current path. The current tail in the silicon IGBT tends to dampen out this ringing. Please note that the connector used to measure VGS is for convenience only to set up the gate pulse voltage levels. The actual VGS waveform observed from that particular point will include the voltage drops of gate bond lead inductance and source bond lead inductance along with the actual VGS voltage. Therefore, when high current pulses are being measured, the observed voltage at this test point will have additional over/undershoots caused by voltage drops across the aforementioned bond lead inductances.

The bill of materials for the double pulse tester is shown in Table 1. The Gerber files can be found at http://www.cree.com/products/power/doublepulsefixture.zip.

Item	Qty	Part Reference	Value	Description	Manufacturer	Manufacturer P/N
1	9	C1-C9	4.7 uf 1500VDC	CAP FILM 4.7UF 1500V	Cornell Dubilier	UNL15W4P7K-F
2	1	D1	C2D10120A	10A 1200V Cree Schottky Diode	Cree	C2D10120A
3	3	J7, J9, J10	BNC	BNC Fem Jack PC Mount Straight	Amphenol Connex	112538
4	7	J1-J3, J5, J6, Load Low, Load High	Banana socket	Banana Socket	Emerson	108-0740-001
5	1	J8	CON6	Kelvin Socket	Loranger	2903 032
6	1	J4	ID CURRENT	SMA Jack-BNC Bulkhead Jack	Amphenol Connex	242181
7	1	J12	JUMPER	Jumper wire		
8	2	R1, R2	470K 2W	Res Ceramic Comp 470K Ohm 2W	Ohmite	OY474KE
9	2	R3, R4	100	100 Ohm 1206 SMD Resistor 1/4W	Panasonic - ECG	ERJ-8GEYJ101V
10	1	U1	Isolated Gate Driver Brd	Isolated gate driver board		
11	1	T1	Current Trans First Stage	Ferrite Toroid	Ferroxcube	TC9.5/4.8/3.2-3E27
12	1	T1	Current Trans Second Stage	Current Monitor	Pearson Electronics	Model 2878
13	1	T1	SMA Adapter	Conn SMA Adapter Plug-Plug Straight	Amphenol Connex	132168
14	1	T1	N/A	Wire, solid AWG 26, Teflon insulation	Alpha	2853/1 WH005
15	1	U1(6pin socket header)		Conn Header Female 6Pos .1” Tin	Sullins	PPTC061LFBN-RC
16	2	U1(3pin socket header)		Conn Header Female 3Pos .1” Tin	Sullins	PPTC031LFBN-RC
17	1	D1 (Socket)	3TERMINAL_BLOCK (D1)	Conn Term Block 3Pos 5mm PCB	Phoenix Contact	1711039

Table 1: Bill of Materials

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