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ABSTRACT

Silicon carbide is a wide bandgap semiconductor that is well suited for high power, high temperature electronic devices due to its remarkable electronic and thermal properties. Photosensitive devices in the 6H polytype of SiC have also been demonstrated, showing high sensitivity in ultraviolet wavelengths near 270 nm. Furthermore, the native oxide on SiC is silicon dioxide, meaning that SiC can be thermally oxidized to form a high quality gate dielectric, making metal-oxide-semiconductor (MOS) devices possible. These qualities make silicon carbide ideal for constructing UV sensitive CCD imagers. This work investigates the feasibility for developing imagers in SiC through the fabrication and demonstration of a buried channel CCD linear shift array.

Several elements of the MOS field effect family were studied. With careful surface preparation and device processing techniques, SiC/silicon-dioxide interfaces have been ameliorated to achieve surface state densities below 2e11 per-centimeters-squared and electron surface mobilities above 40 centimeters-squared-per-volt-second. Buried channel MOSFETs were fabricated with ion implantation of nitrogen at elevated temperatures and have functioned with electron mobilities in excess of 180 centimeters-squared-per-volt-second, which shows an advantage of using the buried channel structure. Studies of capacitance characteristics of the buried channel devices hold good agreement with a general one-dimensional depletion model. A double polysilicon level, overlapping gate process was adapted to the SiC/MOS system. A four phase buried channel CCD shift register was built and operated in the pseudo-two phase configuration at room temperature. Device clocking frequencies were limited to 30 kHz by slow charge readout techniques, but higher speeds have been estimated. In this frequency range, charge transfer efficiencies were probably dominated by carrier trapping in bulk states, which may be present due to ion implantation. Recommendations for improvement of device performance and methods of integrating the CCD with UV photodetectors are given.

CHAPTER 1 - RESEARCH OVERVIEW AND MOTIVATION

1.1 Introduction

Recent advances in growth techniques of wide bandgap semiconductors (e.g., silicon carbide, gallium nitride, synthetic diamond) have stimulated much device research in these materials. The interest in refractory semiconductors has been fueled by the need for electronics to operate under extreme conditions such as high temperature or radiation filled environments. Presently, 6H-SiC is foremost among these new materials because of significant improvement in substrate material quality and controlled, repeatable chemical vapor deposition of both n- and p-type single-crystal thin films [1]. The commercial availability of quality 6H-SiC wafers has facilitated new SiC research programs at the university level and in industrial laboratories.

The motivation for the work presented in this thesis is founded in ongoing interests in a higher efficiency UV imager that is naturally insensitive in visible and infrared wavelengths. The useful applications for such a device are widespread, including astronomy and ballistic missile defense. Other wide bandgap materials show good UV responsivities in various types of photodetector configurations, but SiC has the best outlook for realizing a solar blind UV imager because its native oxide is SiO_2, making it possible to fabricate MOS-based CCDs. This thesis investigates the feasibility of developing imagers in SiC by studying the fabrication, design, and operation of an ion implanted buried channel CCD shift register.

This manuscript is divided into five basic parts. After a brief account of SiC research and material properties, Chapter 1 presents the significant attempts at improving UV photodetection in silicon from a historical basis. SiC n+p photodiodes are only sensitive over a narrow wavelength range around 270 nm, so the last part of Chapter 1 postulates a novel photodetector structure that could push the short wavelength cut-off to 150 nm. Chapter 2 outlines the

preliminary work on basic SiC MOS devices that gives a comparison between surface- and buried-channel devices and establishes the implanted channel process for SiC. Chapter 3 offers a brief review of the charge transfer concept using the buried-channel CCD and discusses the pertinent issues of proper device design. In Chapter 4, experimental results primarily show the charge transfer concept in SiC. A four-phase linear CCD is demonstrated, and fundamental information about the performance is provided. Finally, Chapter 5 reviews the research results and offers some information on possible improvement in subsequent work. Some comments are given on possible configurations for integrating this CCD with the UV photosensitive device.

1.2 Backaround

1.2.1 Silicon Carbide

Silicon carbide is a refractory semiconductor that is found in many different close-packed structures called polytypes [1]. The various polytypes consist of stacked planes of the silicon-carbon tetrahedral basis where silicon atoms are close-packed in two-dimensions (silicon is the larger of the two atoms). Two-dimensional close packing of spheres gives a hexagonal net, so stacking along the c-axis can be described in the ABC notation [2], as shown in Figs. 1.1 (a) and 1.1 (b). There are infinitely many possible close-packing arrangements, since each successive layer can be placed in either of two positions. The stacking sequence of 3C silicon carbide shown in Fig. 1.1 (d) is (...ABCABCABC...), which defines the only cubic polytype. It is seen as a zincblende lattice when the c-axis is aligned along the (111) direction. All other polytypes are referred to as alpha-SiC and are hexagonal (wurzite). The most common of the α-SiC polytypes is 6H-SiC with sequence (...ABCACB...) shown in Fig. 1.1 (c). Similar information on other common alpha polytypes can be found in a comprehensive review of SiC properties by von Münch [3].

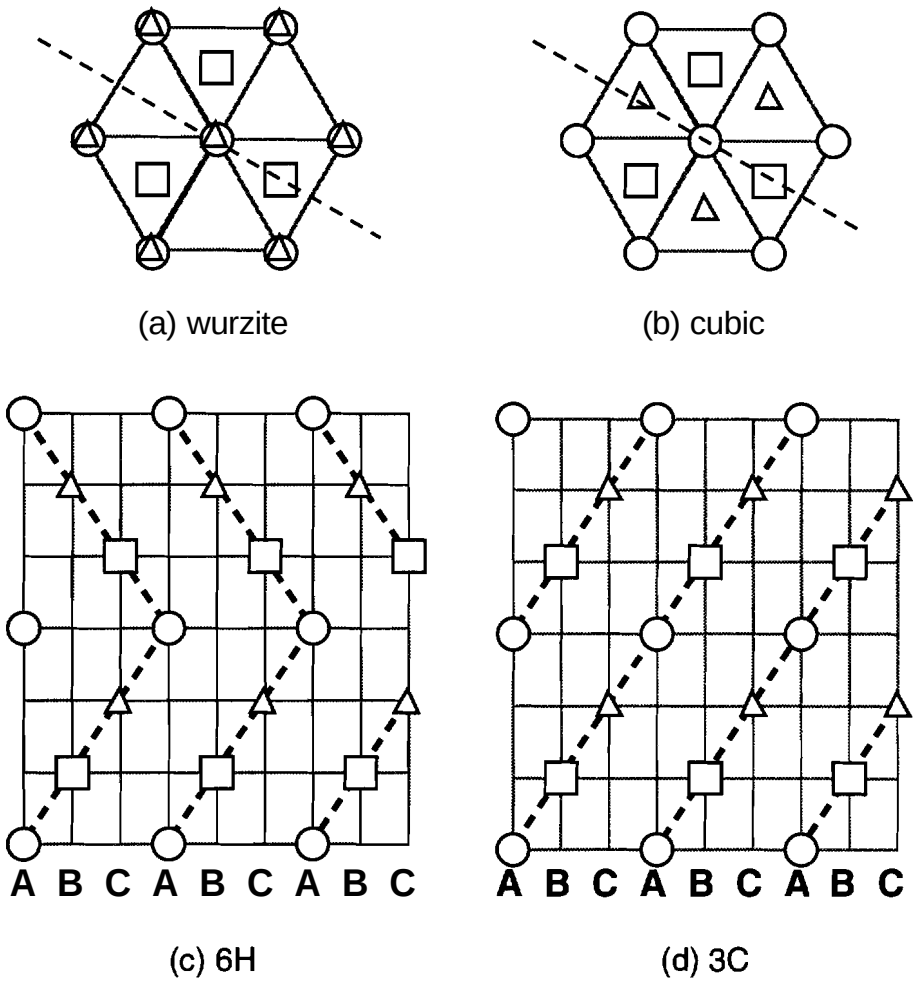


Figure 1.1

Crystal stacking of 2D close packed structures. The "C" layer can go into either of two positions to define either a wurzite (a) or cubic (b) lattice. Slices through the lattice along dashed lines in (a) & (b) show the stacking sequence of the 6H and 3C polytypes. Each square, circular, and triangular symbol represents a silicon-carbon pair in tetrahedra. After von Münch [3].

Forty years of research in bulk crystal growth of SiC has led to the Modified Lely Process [1], commonly called vacuum sublimation. This process yields high quality substrate material of a single polytype. Adapted from the original process developed by Lely in 1955, polycrystalline SiC at 2400 °C sublimes and travels along controlled temperature and pressure gradients to condense onto a mono-crystalline seed crystal at 2200 °C. Single polytype nucleation occurs at the seed, and 25-30 mm diameter boules of single-crystalline 6H-SiC can be achieved [4]. Bulk growth of 3C-SiC has not been

successful with this method, but device quality 4H wafers are now available. The process takes place in a cylindrical graphite container and heating is by RF-induction. Impurity incorporation is accomplished by adding nitrogen for n-type or aluminum chloride for p-type to the ambient during growth [5]. The commercial availability of high quality 6H-SiC 1.18 inch wafers has allowed thin film growth and device research to mature rapidly in recent years.

Homoepitaxial growth of 6H-SiC is accomplished via chemical vapor deposition (CVD) and step controlled *epitaxy*, where growth on off-axis 6H (0001) substrates is carried out at 1200-1400 °C in atmospheric pressure using a SiH_4-C_3H_8-H_2 system. The CVD system typically used is an inductively heated horizontal tube reactor with graphite-coated quartz tube and susceptor. Epilayer doping is accomplished as in bulk crystal growth except that H_2 bubbled through tri-methyl aluminum (TMA) or the addition of diborane (B_2H_6) [6] can also be used for a p-type impurity source. Strict control of n- and p-type impurity concentrations is provided through the method of site competition epitaxy [7], which is based on the preferential occupation of each donor or acceptor in the SiC lattice, depending on the Si/C ratio in the growth ambient. Further information about the bulk growth and CVD epitaxy of SiC can be found in the review articles by Davis [1] and Ivanov [8] and in the references therein.

The remarkable thermal and electronic properties of 6H-SiC allow the number of device applications of this material to be substantial. The large bandgap 3.0 eV [3], high value of saturated electron drift velocity 2.0×10^7 cm/s [3], large breakdown electric field 3×10^6 V/cm [9], and good thermal conductivity 3.5 W/cm°C [3] provide advantages over Si and GaAs for high-power, high-temperature devices. In addition, silicon carbide can be oxidized with techniques similar to those used for silicon to form an electrically insulating native oxide, making metal-oxide-semiconductor (MOS) devices possible. With the promise of duplicating silicon MOS technology for use at high temperatures, a great deal of work has been done to characterize growth rates and quality of SiO_2 on silicon carbide [10]-[12]. Recent advancements in MOS device processing and characterization [13], [14] show a vast improvement of interface characteristics over previous reports [15], [16].

Most of the past and present device research has emphasis on discrete high-power devices capable of operation at elevated temperatures. The types of transistors investigated include BJTs [17], Schottky-gate MESFETs and

buried-gate JFETs [18], and inversion-type MOSFETs that have been demonstrated up to 923K [19]. Several groups have presented UV-photodiodes with peak responsivities near 270 nm [20], [21]. The commercial production of the blue LED by Cree Research, Inc. in the late 1980s has given SiC the most publicity as a new semiconductor material. Although there has been a vast amount of interesting device work in 6H-SiC over the past several years, most of the results are preliminary in nature and represent experiments on devices with non-optimized parameters. As summarized by Neudeck [22], much work is required to improve material quality in both bulk crystals and epitaxial layers of SiC, and production of the high performance devices envisioned for SiC will scale up rapidly as defect densities are reduced and wafer sizes increase.

Despite the adolescence of silicon carbide crystal growth and fabrication technology, device research has recently graduated to the demonstration of both analog and digital integrated circuits that operate up to 300 °C. Work at Purdue University has shown 6H-SiC to be a viable material in which to develop non-volatile memories [23], and various logic functions were implemented using an n-MOSFET enhancement-load topology [24]. An important contribution to the realization of high temperature sensors and control circuits came with the announcement of the first monolithic operational amplifier in 6H-SiC [25]. The demonstration of a charge-coupled device presented in this work also adds to the recent variety of SiC integrated circuits.

1.2.2 UV Photodetection

Detection of electromagnetic radiation in the near UV and below has been a useful application of solid-state sensing since the late 1960s. Astronomers were early proponents of solid-state UV photodetectors for more compact and less expensive characterization of the heavens. Modern health care techniques, food sterility methods, and manufacturing processes (semiconductor fabrication is a good example) use ultraviolet light sources in process, which must be accurately calibrated and maintained by UV-detectors. UV non-destructive testing (NDT) for process monitoring was recently used to control the manufacturing of sterile packaging for medical uses [26]. Other

practical uses include: a personal UV detector for monitoring sun exposure, UV spectroscopy for material characterization, and solid state detection for combustion control.

With the introduction of the CCD in 1970 [27], and it's quick evolution into an optical imaging device, many scientists developed CCD-imaging for UV as well as for the visible and infrared wavelengths. By 1976, CCDs were the detectors of choice for terrestrial astronomical observatories. Scientists working on the Hubble Space Telescope chose a specially designed silicon CCD imager for UV, visible, and infrared observation of space [28]. Although silicon devices have been used in these applications, quantum efficiency has never exceeded 10-15% in the UV, thus requiring long integration times. This necessitates refrigeration to suppress dark current, adding complexity and weight to the imager system design.

The conventional photodetector is the n+p photodiode shown in Figure 1.2 (a). Radiation incident at the n^+ side falls off exponentially with distance according to the absorption constant α as shown in Fig. 1.2 (b). A representative band diagram in Fig. 1.2 (c) shows what happens to photogenerated electron-hole pairs. Signal current I_{ph} arises from e-h pairs created inside or within a diffusion length of the depletion region because the electric field separates the carriers before they recombine. Minority carriers generated elsewhere migrate to the surface to recombine [21] or recombine within the quasi-neutral bulk regions [29]. At shorter wavelengths, the absorption depths become shallower as shown in Fig. 1.2 (b), and most photogeneration occurs near the surface of the device. Responsivity drops because the excess carriers recombine and do not produce terminal current.

As shown in Fig. 1.3 (a), the absorption coefficient for 6H-SiC remains relatively low in the 200-400 nm range, which has prompted many groups to use 6H-SiC for photodiodes [20], [21]. Even the first UV-detector was made of 6H-SiC [30]. Typical photoresponse curves in Fig. 1.3 (b) compare silicon [31] and 6H-SiC [32] photodiodes, the latter showing improved UV response. Brown et al. reported 6H-SiC photodiodes having thinned n^+ epilayers [21] in which typical quantum efficiency (QE) values peaked at 70% around 260-270 nm. Detectors with thinner n^+ emitters showed marginal improvement of short wavelength responsivities, but QE still fell below 10% by 200 nm.

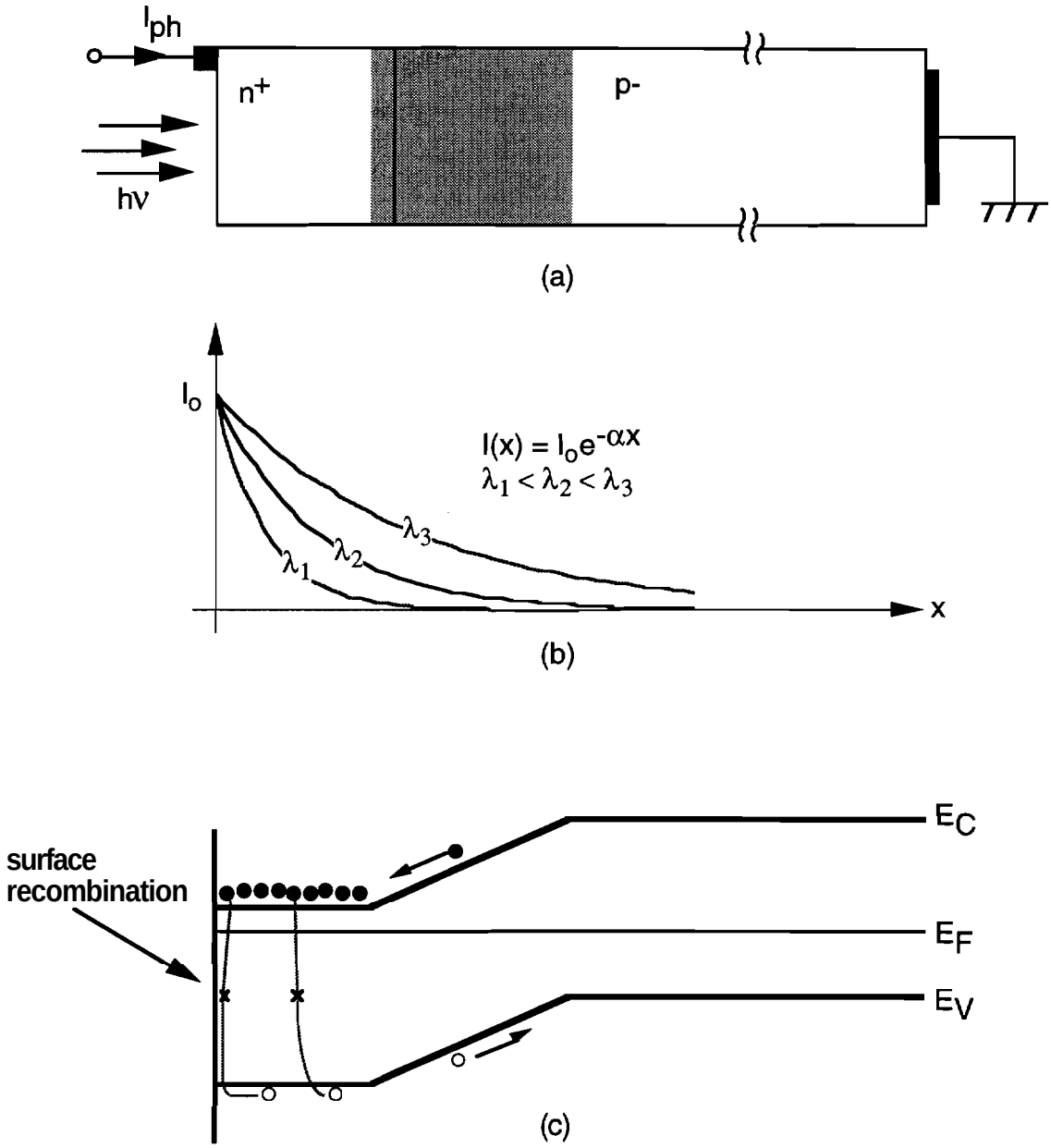


Figure 1.2

Conventional photodiode structure. Terminal current arises from carriers that are separated by the electric field in the depletion region. Other carriers are lost to recombination. The short-wavelength cutoff in responsivity is due to shallow absorption and surface recombination of e-h pairs.

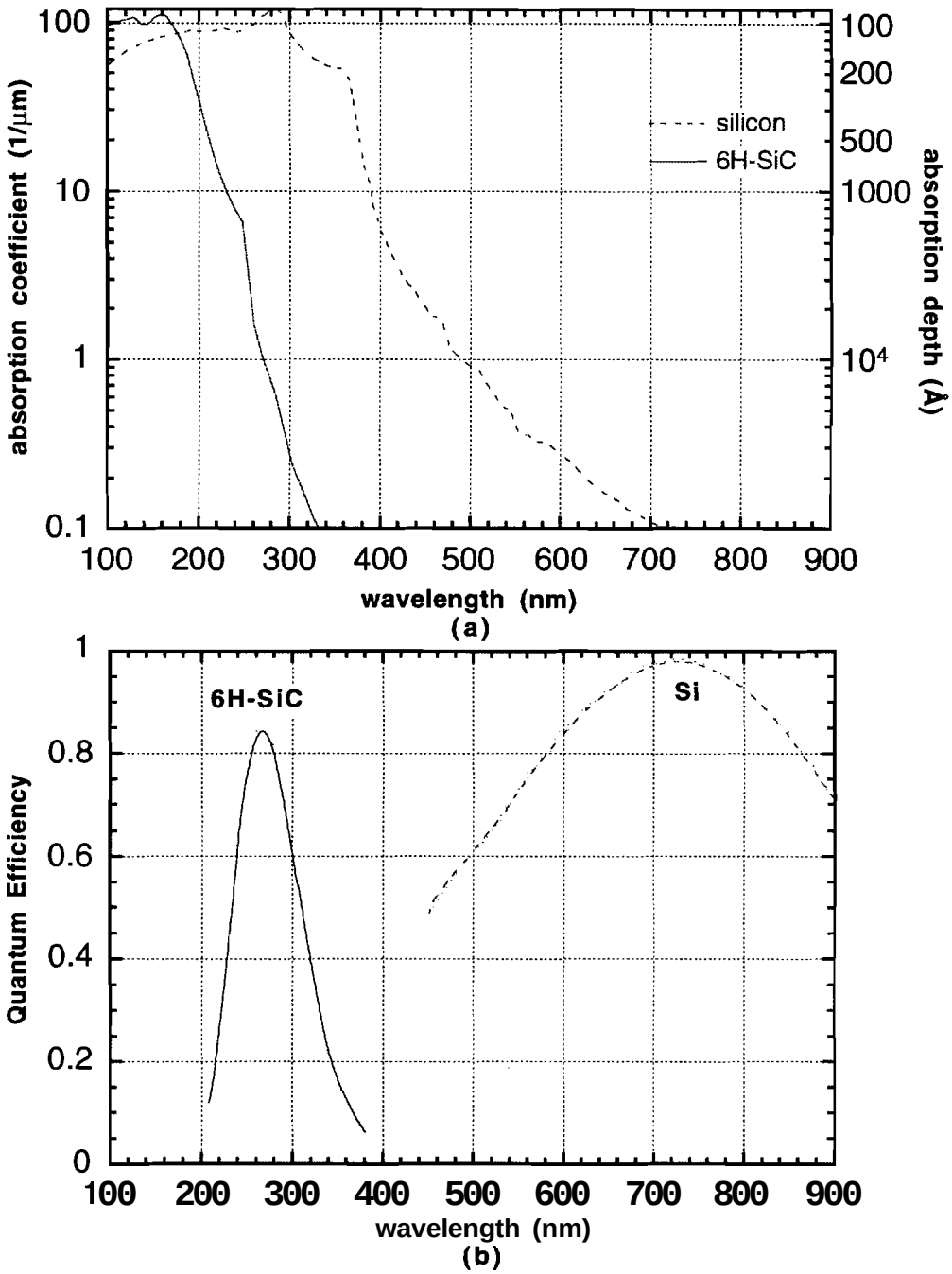


Figure 1.3

(a) Absorption coefficient vs. wavlength for silicon and silicon carbide. (b) Typical quantum efficiencies for p-n photodiodes in these materials. Long wavelength cutoff is due to the bandgap of each material. Short wavelength reduction in QE is due to the increase in absorption coefficient because excess carriers generated near the surface are lost to strong surface recombination. After [43], [31], and [32].

Over the past 20 years, many attempts have been made to improve sensitivity of silicon photodetectors in the 100-400 nm range. The best known of these are listed in Table 1.1 to chronicle the advancement of UV-photosensitivity to date. In 1974, Shortes et al. introduced the idea of a thinned, backside-illuminated CCD imager to overcome absorption in the topside metallization patterns [33]. This structure suffered decreased sensitivity in the blue (420 nm) because of recombination at the back surface. A breakthrough (for color sensitive imaging, at least) was offered by Brown et al. through the use of transparent indium-tin-oxide gates on frontside illuminated, charge-injection device imagers [34]. The new structure showed a 70% quantum efficiency (QE) down to 400 nm, but dropped precipitously low below that because of absorption in the metal-oxide gate.

Two UV-sensing ideas emerged in the late 1970s that are of importance to this work. In 1978, T.E. Hansen presented UV sensitive photodiodes that utilized the positive fixed oxide charge, which is intrinsic to the interface of thermally oxidized p-type silicon [35]. The resultant surface depletion layer prevented surface recombination of photogenerated carriers, and QEs of 50-60% were maintained down to 200 nm. Then, in 1979, J. Hynecek introduced the revolutionary virtual phase CCD technology in which one phase of a 2-phase CCD had a gate electrode built into the surface [36]. This eliminated the overlying metal or polysilicon gate and improved responsivity. Unfortunately, this device suffered from significant surface recombination because of the parasitic p+n photodiode at the virtual gate, and QE fell to 31% by 400 nm. In spite of this, virtual gate CCD technology is a standard feature of modern megapixel color CCD imaging arrays because of higher resolution and simpler operation [37].

Another well-known idea is the use of "downconverting" phosphors that fluoresce in the green when excited by wavelengths below 400 nm [28]. When the UV sensitive coating coronene was used on a backside-illuminated CCD, QE improved to 10% in the 100-400 nm range. Also, Janesick showed that the QE of backside-illuminated CCDs was improved through the use of backside charging. By either "UV flooding" [38] or use of a "flash gate" [39], surplus electrons are supplied to the outer surface to accumulate the p- surface under the native oxide. As a result, signal electrons are rejected from the back surface and driven towards the CCD channel, improving overall QE. Recently, J. Kothe

Table 1.1

List of the various attempts to improve UV response in silicon photodiodes and charge-transfer devices. The three most relevant problems include surface recombination, absorption in metal gates, and destructive interference in the oxide layer. The shaded items have significant contribution to the SiC imager.

Author, Year	How Improved	QE Improvement	Biggest Problem
Shortes, 1974	Backside, Thinned CCDs	10% at 400 nm	surface recombination
Brown, 1976	Transparent Metal Gates	70% at 400 nm	absorption in gates <400 nm
Hansen,1978	Natural Inversion Layers	50-60% to 200 nm	multiple reflections in oxide
Hynecek,1979	Virtual Phase Technology	31% by 400 nm	surface recombination
Blouke,1979	Downconverting Phosphor	10% over 100-400 nm	poor reproducibility
Janesick,'85-'87	Backside Charging	~50% to 300 nm	uniform thinning is difficult
Kothe, 1991	CCD w/ Nat. Inv. Layers	80% at 200 nm	multiple reflections in oxide

and W. von Munch implemented a linear array CCD that is well suited for detecting wavelengths down to 200 nm [40]. Signal charge is integrated at a one-dimensional array of "natural inversion layer" sensing regions and collected under a storage-gate next to each photo-element. At the end of an integration period, all of the collected electrons are fed via transfer gate to an adjacent two-phase CCD for readout. This idea works very well showing near 80% QE at 200 nm.

Overall, it seems that the concept introduced by Hansen and only recently used by Kothe and von Munch is the most elegant and effective. An ungated photosensing element in which a built-in electric field extends all the way to the surface should only be limited in its short wavelength performance by the absorption and reflection properties of the passivating oxide. The speed of this photosensor may be hindered by lateral series resistance of the induced inversion layer, but this potential problem may be reduced with small pixels sizes. The concept of "charge-induced field" photocollection is the main idea that would be the most useful with the 6H-SiC buried-channel CCD imager, so a brief explanation of its principle of operation is given in the following section. A large area photodetector would have to interdigitated.

1.3 Improving UV Photosensitivity in SiC

As mentioned before, n^+ emitter regions thinned to 500 Å have been used to reduce the short wavelength cutoff in 6H-SiC devices [21], [41]. However, Fig. 1.3 (a) indicates absorption depths are less than 200 Å for wavelengths below 200 nm, meaning that most electron-hole pairs are generated much shallower than any practically thinned n+p detector can collect. Other issues such as lateral series resistance in the emitter and non-repeatability of thinning techniques make this structure inappropriate for use with a CCD imager.

A structure in which the depletion region extends to the surface is desirable for shorter wavelengths because the built-in electric field can collect even the shallowest generated e-h pair. A typical MOS device has a depletion region that reaches the surface, but strong absorption in metal or polysilicon gate material prevents most light below the visible range (λ<440 nm) from penetrating into the semiconductor [34]. Surface band bending can be induced in a p-type semiconductor without an overlying gate if fixed positive charges exist at the oxide-semiconductor interface [35], [40]. Figure 1.4 depicts the charge-induced depletion region of a photodetector, where fixed-oxide charge is the cause of band bending at the surface. For sufficient fixed positive charge, an inversion layer exists at the interface, and signal electrons can be extracted by lateral transport to an adjacent CCD potential well [40] or to a reverse bias pn junction [35]. The electrons cannot be lost to surface recombination because of the deficit of holes at the surface. This design has an additional advantage for 6H-SiC because no thermal generation (dark current) is expected due to the wide 3 eV bandgap.

The internal quantum efficiency of this structure is expected to reach 100% due to the expedient separation of e-h pairs. Therefore, the main losses in the total external quantum efficiency are caused by the optical properties of the oxide. Transmissivity (T) is calculated by considering multiple reflections and absorption in the SiO_2 layer [42]. Tables of optical constants for 6H-SiC and SiO_2 are readily available [43]. Two examples of transmissivity of monochromatic light through oxide layers are plotted in Fig. 1.5. The transmission through the 20 nm oxide is flat and remains near 80% down to the

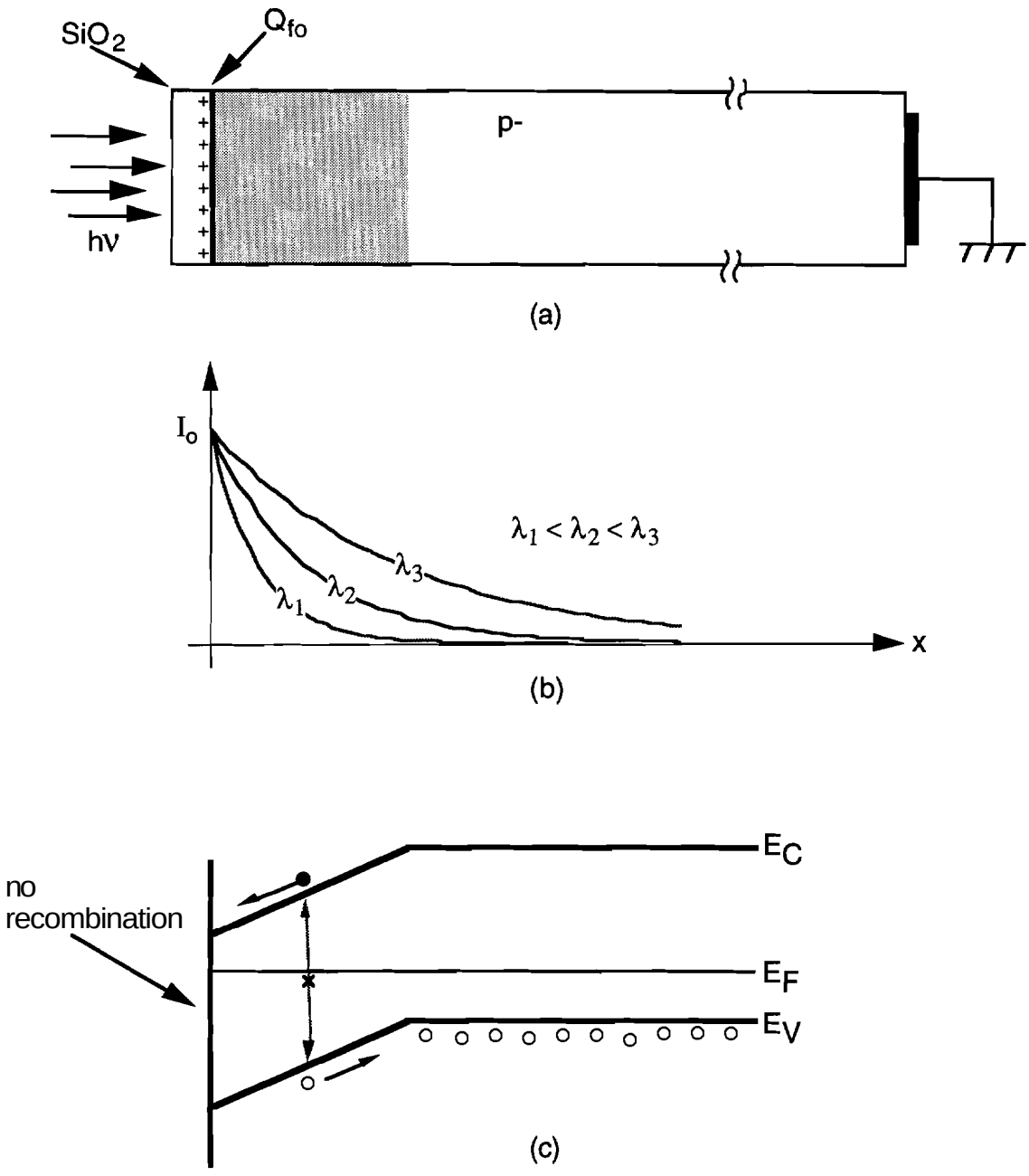


Figure 1.4

Schematic diagram of induced-field photocollection. Positive fixed charge in the oxide causes a natural surface depletion region. Even e-h pairs generated at shallow depths are separated by the built-in field at the surface. Recombination does not occur at the depleted surface, and the wide bandgap of SiC prevents any appreciable thermal generation that might add superfluous signal charge.

absorption edge of the SiO_2. The 10 nm curve is included to demonstrate the effects of interference in the oxide layer. The long-wavelength cutoff of responsivity is estimated from the curve for 6H-SiC in Fig. 1.3 (b) and plotted with short dashes. The combined curves give an estimate of the photoresponse of the induced field structure for SiC. This spectral response spans more of the UV spectrum than any other solid state photodetector in the literature. The development of such a structure is beyond the scope of this thesis, but its integration with a SiC-CCD is given in one possible scenario in Chapter 5.

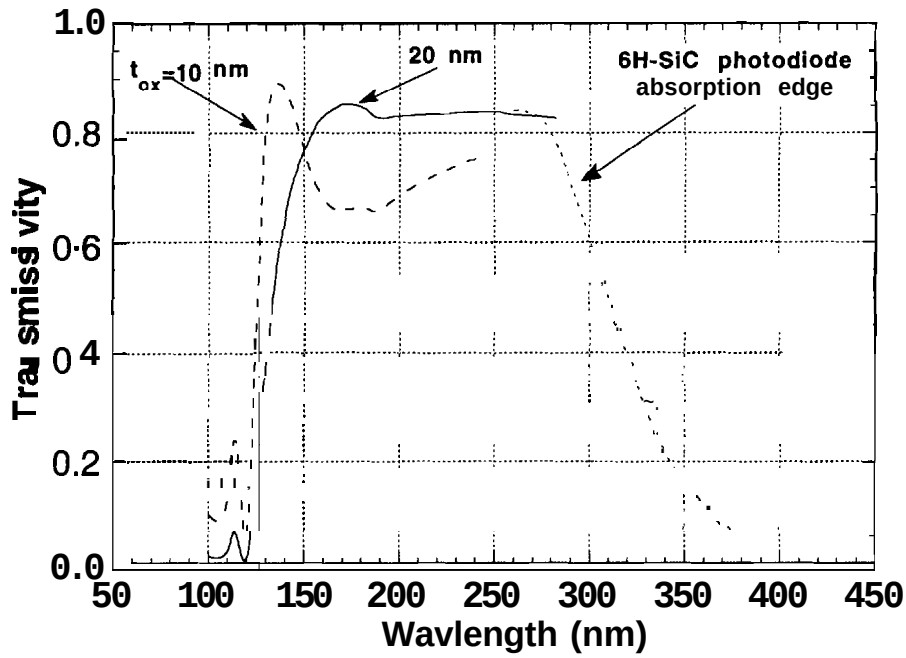


Figure 1.5

Transmissivity of monochromatic light through oxide into 6H-SiC. The short-dashed line is the long-wavelength response of a photodiode. The combined curves give an estimate for the spectral response of the induced field photodiode in Fig. 1.4. The strong cutoff at 125 nm is determined by the bandgap of SiO_2.

CHAPTER 2 - PRELIMINARY WORK

2.1 Introduction

The fabrication and characterization of diagnostic inversion- and buried-channel devices in 6H-SiC were accomplished in the initial stage of this work. As a result, the use of ion implantation to form an n-channel in p-type SiC was established, and some classic MOS-related effects were demonstrated.

Charge-coupled device structures are classified into two general types: surface-channel CCDs (SCCDs) and buried-channel CCDs (BCCDs). Although this research is for the development of a BCCD, the results of both inversion-channel and buried-channel gate-controlled diodes and field-effect transistors in 6H-SiC are presented in this chapter. C-V and I-V measurements of the inversion-channel devices are given in Section 2.2.1 for comparison to the buried-channel devices examined in Section 2.2.2. Well established characterization procedures are used to give important information about the BC structure (i.e., channel mobility, pinchoff voltage, channel doping, and n-layer thickness).

2.2 6H-SiC MOS Test Devices

2.2.1 Inversion-Channel MOS Devices

Historically, the first CCDs were developed as surface channel devices [27], so inversion-channel MOSFETs and gate-controlled diodes were analyzed. The results presented in this section reflect the initial fabrication efforts of this research, and therefore represent non-optimized oxidation procedures. Nevertheless, important information about the room temperature

behavior of the SiO_2-SiC interface and a basis for comparison to improved results in Chapter 5 are established from these measurements.

2.2.1.1 Gate-controlled diode

The minority carrier generation rate in silicon carbide is very low because of its large bandgap and the concomitantly low intrinsic carrier concentration. Consequently, an MOS capacitor at room temperature cannot remain in thermal equilibrium with sweeping DC bias, and the capacitance-voltage ($C\text{-}V_G$) response generally shows a deep-depletion characteristic when measured in the dark [10], [11], [44]. Fig. 2.1 shows a $C\text{-}V_G$ sweep of an Al-SiO_2-SiC capacitor on p-type material measured in the dark at a sweep rate of 0.1 V/sec. During the sweep from accumulation towards inversion, the device is driven into deep-depletion because of the lack of thermally generated carriers. An ideal C-V curve is also plotted, purposely shifted along the voltage axis, to show that it is parallel to the data in depletion and deep-depletion. This indicates that surface states residing deep in the bandgap are not in equilibrium with the DC bias sweep and therefore go undetected during the measurement. In this section, a conventional MOS gate-controlled diode is used as an external source of inversion charge, which allows measurement of deep level surface states at room temperature.

The SiC gate-controlled diode consists of a circular n+p diode of diameter 50 μm surrounded by an arınular gate of area 3.59×10^{-4} cm^2. The p-type 6H-SiC (0001) substrate was doped ~4×10^{18} cm^{-3} and had a 3 μm epilayer doped with Al at 2.8×10^{16} cm^{-3}. The n^+ regions were selectively implanted with nitrogen at an elevated temperature through a 0.9 μm titanium/nickel mask and a 300 Å SiO_2 screen layer. Multiple implant energies were used with a total dose of 5×10^{15} ions/cm^2 to achieve a rectangular profile of approximately 1×10^{20} atoms/cm^3 to a depth of 0.55 μm. The nitrogen activation anneal was performed in a Lindbergh tube furnace under argon with the following thermal cycle: ramp from 900 °C to 1500 °C at 22 °C/min, hold at 1500 °C for 12 minutes, ramp to 1100 °C at 40 °C/min. After this anneal, the ambient was switched to dry O_2 for a 3 hour oxidation. This sacrificial oxide was removed with buffered hydroflouric acid (BHF) prior to a piranha-clean

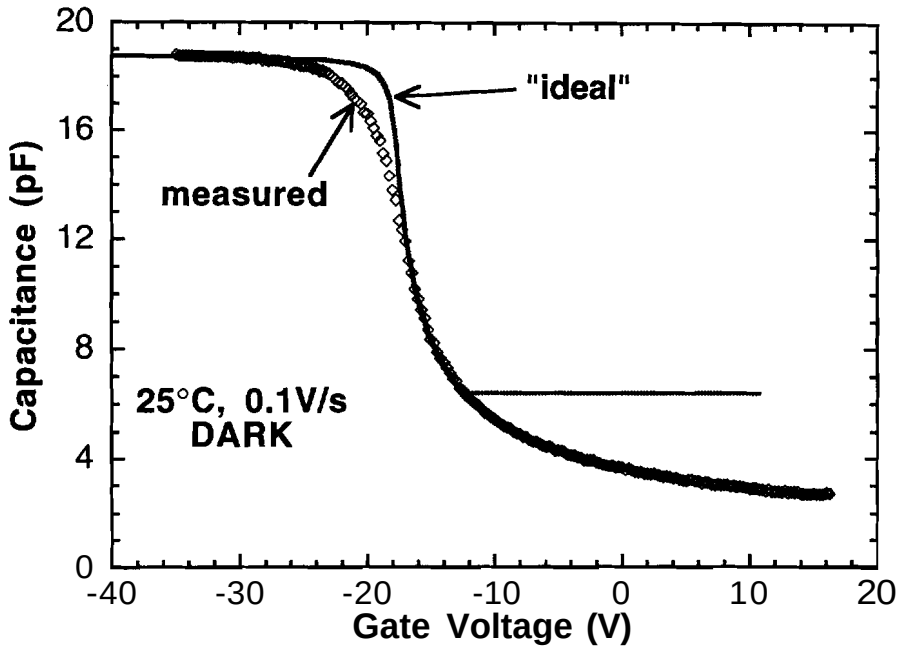


Figure 2.1

C-V_G response of a SiC MOS capacitor with gate area 3.59×10^{-4} cm^2 and oxide thickness 660 Å. The ideal curve is shifted in voltage such that it matches the data in depletion. Deep-depletion occurs because thermal generation creates minority carriers much slower than the 0.1 V/s sweep rate.

($1H_2O_2$:$1H_2SO_4$) and a final BHF prep soak. Next, the gate oxidation was performed in a horizontal hot wall quartz tube furnace under dry O_2 for 21 hours at 1100 °C to yield about 660 Å of SiO_2. After a 30 minute anneal under argon, the sample was removed within 10 seconds and allowed to cool in argon for 10 minutes. A 1 μm layer of aluminum was deposited by thermal evaporation onto the backside and subsequently annealed at 1000 °C for 5 minutes. Windows are wet-etched in the oxide, and nickel ohmic contacts were electron-beam deposited over the n^+ regions. Aluminum gates were thermally evaporated and defined with a standard liftoff procedure.

Capacitance measurements were performed in a grounded dark box with an HP4275 LCR meter via HPIB control. A simple voltage divider circuit was used to bias the n+p diode during the sweeps. The C-V_G characteristic of the SiC gate-controlled diode is shown in Fig. 2.2 for three signal frequencies. This device shows the peculiar "hook and ledge" characteristics that were first reported by Goetzberger and Irvin for silicon MOS devices at 77K [45]. An

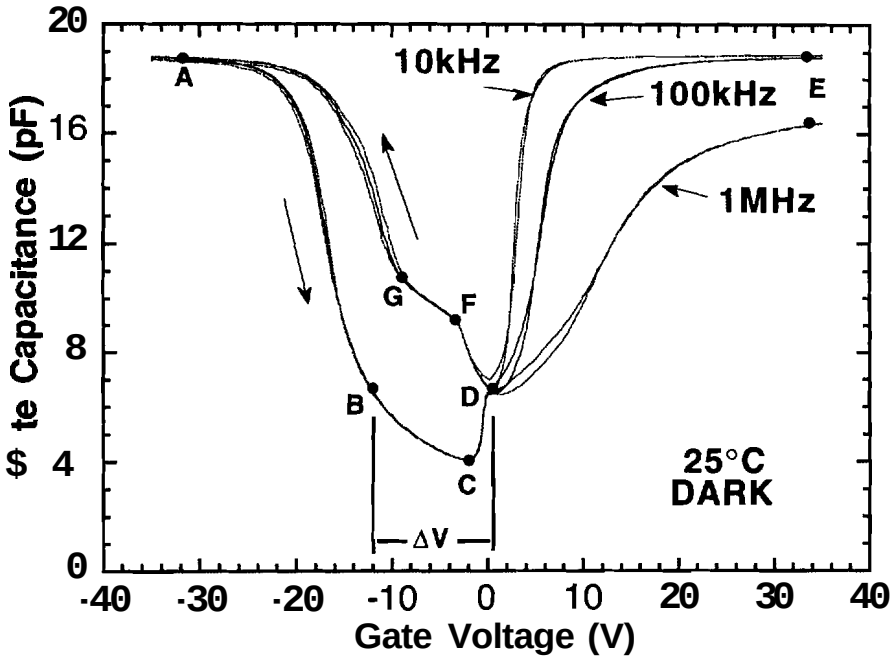


Figure 2.2

C-V_G response of the SiC gate-controlled diode at room temperature in the dark with a drain bias of zero and a sweep rate of 0.1V/s. In inversion, very little hysteresis is present, and frequency dispersion is due to the resistance of the inversion channel. The hysteresis seen in depletion and accumulation is attributed to the non-equilibrium behavior of deep traps.

understanding of these phenomena is achieved by reviewing the non-equilibrium behavior of deep-level surface states.

The surface states are assumed to be in equilibrium with the Fermi level (i.e., filled with holes) in accumulation at point A in Fig. 2.2. Moving towards point B, the empty states are pushed below the semiconductor Fermi level due to the field effect from the gate. Minority carrier electrons are absent in depletion, so electron capture into these levels is not probable. Emission rates for holes are drastically reduced for traps removed from the valence band edge [46], so only states near E_V will equilibrate via hole emission into the valence band, and the rest of the surface states swept out from A to B remain empty.

The deep-depletion "hook" portion between points B and D in Fig. 2.2 is a direct result of surface states. The semiconductor surface reaches strong inversion at point B, but the low-frequency response does not appear because of a barrier to electrons at the edge of the n^+ island [45]. Electrons from the n+p junction are trapped in surface states adjacent to the n^+ island, resulting in a

reduced surface potential near the junction that is a barrier to further electron flow. This disconnects the inversion layer under the center of the gate from the n^+ island, and the center part of the MOS capacitor goes into deep depletion. Finally at point C in Fig. 2.2, the surface states in the barrier region are completely filled, the barrier region inverts, and electrons flow into the region beneath the gate. The total number of surface states can be roughly estimated from the voltage shift from B to D as

$$N_{IT} \cong \frac{\Delta V C_{ox}}{q} \tag{2.1}$$

where C_{ox} is the capacitance per unit area in accumulation. The voltage shift in Fig. 2.2 yields an N_{IT} of about 4×10^{12} cm^{-2}. From D to E, the low-frequency capacitance is observed because the density of inversion electrons varies with the AC signal due to efficient supply from the drain [47]. The frequency dependence in inversion is due to the finite conductivity of the inversion channel and the associated RC time constant.

The sweep from inversion back to accumulation reveals the ledge feature of the C-V_G response. The ledge has also been reported in SiC MOS capacitors where photo-generation is used as a source of minority carriers [10], [12]. As the gate voltage is reduced from E to D, inversion charges exit through the adjacent n^+ island, and the surface remains in equilibrium. Depletion is reached at point D, and the bands begin to unbend back towards flatband. During this time, the occupied surface states move above the Fermi level, but the electrons cannot emit and follow the DC bias sweep. The charge occupancy remains close to the value it had at point D, so the voltage shift (AV) seen in the C-V_G curve is constant from D to F. At point F, the surface hole concentration becomes appreciable, and the surface states begin to equilibrate by hole capture.

Past point G there is a residual voltage shift, which is not present for silicon gate-controlled diodes [45]. The direction of this shift is indicative of charge trapping in slow traps in the bulk oxide near the interface. These have been postulated as due to the incorporation of aluminum into the SiO_2 during oxidation [48], [49], but recent results by Shenoy et al. [13] debunk that assumption and attribute the presence of near-interface oxide traps to improper cleaning and oxidation techniques. Results of improved interfaces are

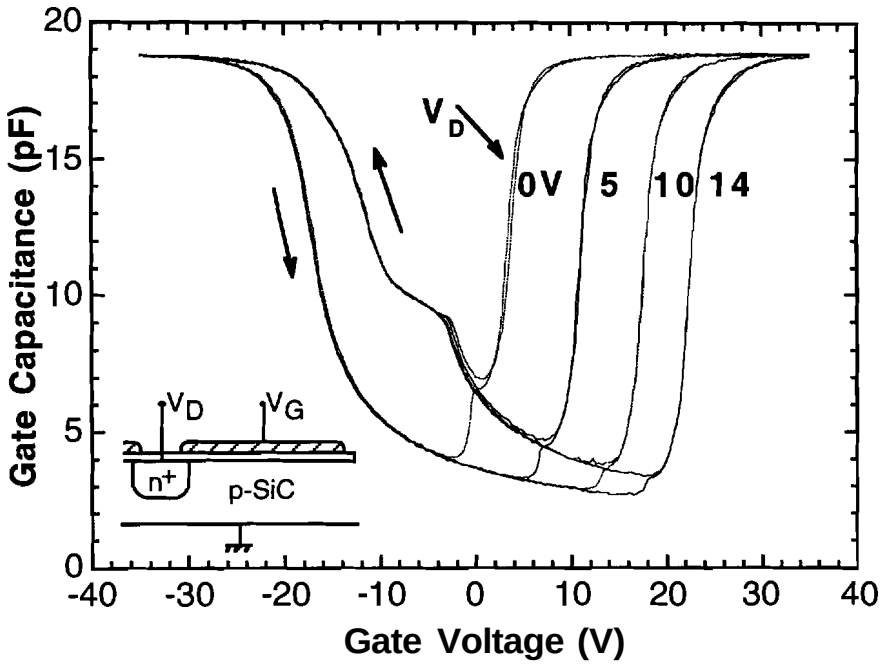


Figure 2.3
Response of the SiC MOS gated diode as a function of drain bias at room temperature in the dark. The sweep rate is 0.1 V/s, and the measurement frequency is 20 kHz. A reverse bias at the n^+p junction causes a delay of inversion, as expected in these devices.

presented in Chapter 5 in a discussion of the proper fabrication of polysilicon-gate field-effect devices in SiC.

Fig. 2.3 shows the C-V_G response of the gate-controlled diode for three additional drain biases. A positive bias V_D at the n^+ island reduces the electron quasi-Fermi level in the depletion region under the gate [47]. As a result, inversion is delayed until the surface potential (in the barrier region) reaches $2\phi_f+V_D$, where ϕ_f is the bulk Fermi potential of the p-SiC. This shows the usefulness of the SGCD for investigating deep depletion characteristics, which are necessary for operation of a surface channel CCD.

2.2.1.2 Inversion-channel MOSFET

Although the MOS capacitor and gate-controlled diode are very useful for analyzing the behavior of the oxide-semiconductor interface, it is the MOS

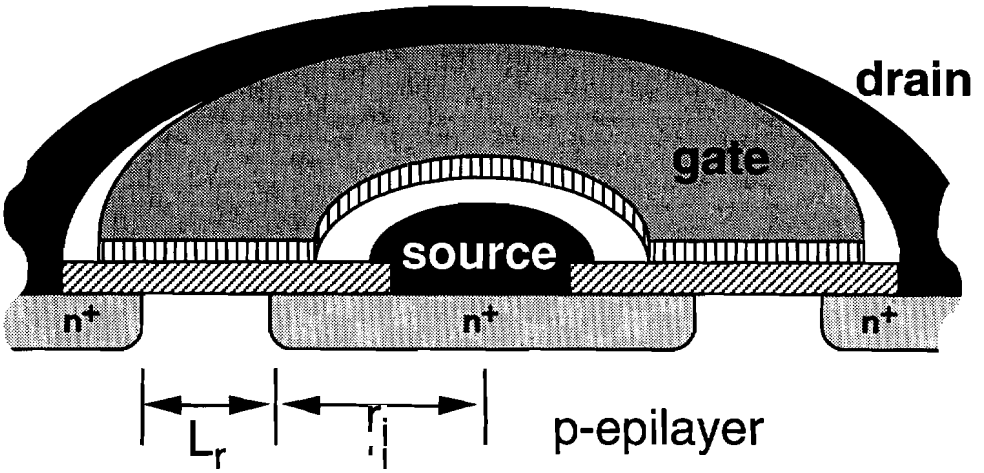


Figure 2.4
Schematic cross-section of a circular inversion-channel MOSFET. This structure is fabricated with the same steps used for the SGCD. The n^+ island is about 0.55 μm deep with doping $N_D > 10^{19}$ cm^{-3}. Oxide thickness is 660 Å.

transistor which has the most practical use. The inversion-channel MOSFET (also known as an enchancement-mode device) is the primary building block in silicon integrated circuit technology. This device is also a useful tool for analyzing transport behavior at the oxide-semiconductor interface, which is of primary concern when considering surface-channel CCDs.

A set of circular enhancement-mode MOS-transistors with gate lengths 5, 10, and 20 μm were fabricated on the same sample that contains the gate-controlled diodes. Fig. 2.4 shows a cross section of the circular transistor where the channel dimensions are defined by an inner radius r_i and a radial channel length L_r. In the usual convention, measurements were performed with the source terminal at ground potential and gate, drain, and backplane voltages referred to the source. Room temperature measurements were taken under probe test and recorded with an HP4145B Semiconductor Parameter Analyzer.

The output characteristics of the enhancement-mode transistor in Fig. 2.5 show good saturation and a positive threshold voltage. The effective mobility of the MOSFET is found from the slope of the I_{DS} vs. V_{GS} plot in Fig. 2.6 to be about 20 cm^2/Vs, which is comparable to values measured for other 6H-SiC inversion-layer devices [50]. The channel transconductance at low drain bias is 10 μS/mm , and the threshold voltage is 4 volts. Note that the current in Fig. 2.6 deviates from the linear model at large gate voltages due to mobility

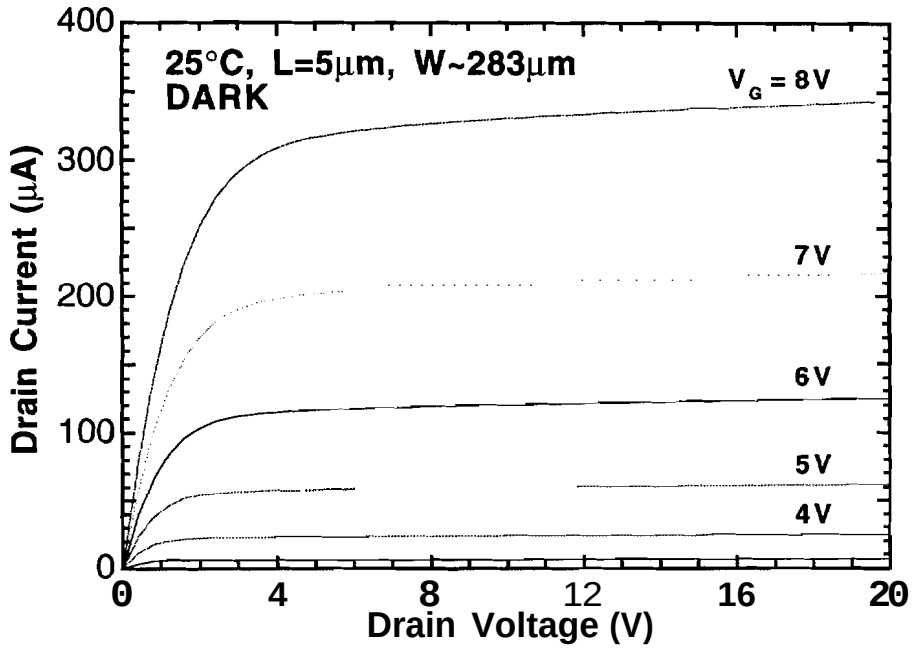


Figure 2.5
Output characteristic for a 5 μm circular enhancement-mode MOSFET at room temperature in the dark. Oxide thickness is 660 Å.

degradation and series resistance [46]. The former effect is a primary problem in SiC surface-channel NMOS devices because of the interfacial fixed oxide charge.

2.2.2 Buried-Channel MOS Devices

Reduced mobility of carriers in an inversion-layer is an inherent limitation on the performance of surface-channel CCDs because the three charge transfer mechanisms of a CCD,

(a) drift due to self-induced field,
(b) drift due to fringing field, and
(c) thermal diffusion

are heavily dependent on mobility [51]. Charge transfer efficiency at higher clock speeds can be adversely affected in a SCCD with poor interface transport qualities. At lower frequencies, trapping at interface states limits transfer

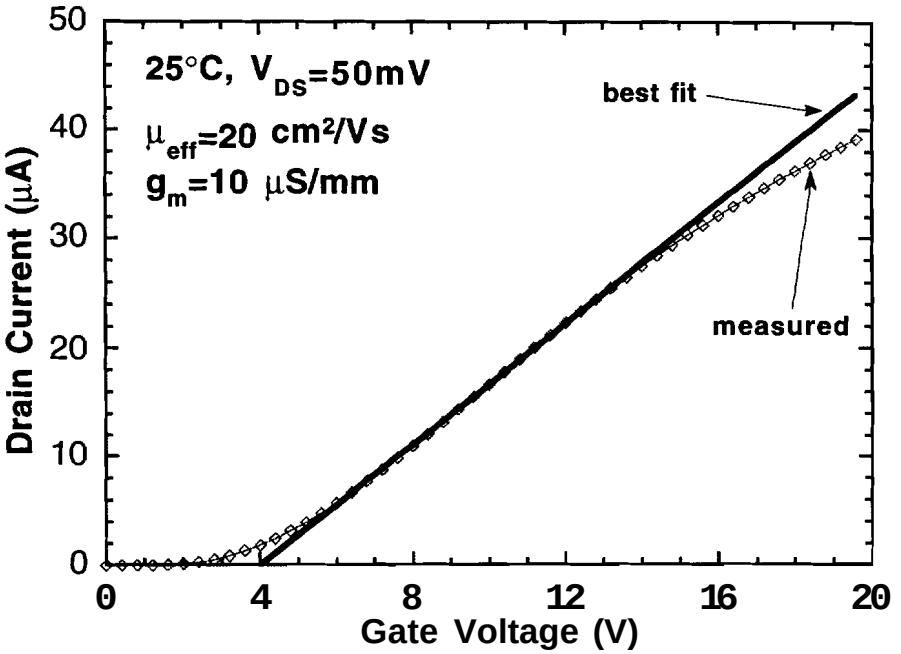


Figure 2.6

Linear region characteristic for the 5 μm circular enhancement-mode MOSFET of Fig. 2.4. Sublinear current at high gate biases is caused by mobility degradation and high series resistance.

efficiency and causes an undesirable image smear [52]. Accepting that surface niobilities must always be lower than bulk mobilities and that surface states are always present, early silicon CCD designers solved the problem with the buried-channel CCD [53] in which carrier action takes place away from the interface. By forniing a channel of doping opposite that of the substrate under the oxide, a potential well inside the bulk is created where carriers congregate. As a result, transport of signal charge is not impeded by surface scattering, and higher transfer efficiency is attained. An additional advantage is lower noise because of the absence of interaction with surface states. For these reasons, the buried-channel structure is used in most charge-transfer applications today, and is the backbone of modern silicon CCD imaging technology.

Iniportant properties of the 6H-SiC bulk transfer device can be investigated using MOS capacitors and field-effect transistors that have a shallow buried n-layer between oxide and p-epilayer. In this section, the buried-channel gate-controlled diode (BCGD) and the buried-channel MOSFET (BC MOSFET) are used to determine the inipurity concentration and thickness of the buried n-channel as well as majority carrier bulk mobility. Additional

information about channel potential minimum and its location is extracted for various applied biases. These parameters are useful for designing, modeling, and selecting proper operating conditions of the BCCD.

2.2.2.1 Buried-Channel Gate-Controlled Diode

The cross-section of the buried-channel gate-controlled diode (BCGD) is shown in Fig. 2.7 (a). Note that the n-type channel extends beyond the gate by 10 μm on all sides. This device was fabricated in 6H-SiC with procedures similar to those used for the inversion-channel devices described previously. The n^+ source/drain regions were implanted into a p-type epilayer with an acceptor concentration of $1x10^{16}$ cm^{-3}. Multiple nitrogen implants were used to produce a nearly uniform channel with an intended doping of $3x10^{17}$ cm3 and a depth of 0.25 pm. Due to the low rates of dopant diffusion in SiC [3], [65], the as-implanted distribution remained essentially constant through subsequent high-temperature steps. Both implants were activated at 1550 °C, after which the gate insulator was grown with a 5.5 hour wet oxidation at 1150 °C and a subsequent 30 minute argon anneal. Surface preparation included a clean in organic solvents, followed by a soak in "piranha" ($1H_2O_2$:$1H_2SO_4$) and a final BHF prep soak. The resultant oxide thickness is 736 Å, determined from the accumulation capacitance of an MOS capacitor. Substrate and n^+ contacts were formed as before. The gate metal was deposited as 500 Å of chromium with a 2000 Å gold overlayer.

The band diagram of the buried-layer structure is shown in Fig. 2.7 (b). In this device, the n^+ contact to the buried layer is used to control the channel potential ϕ_{ch} and monitor the gate-to-channel capacitance. In accumulation and depletion, the gate-to-substrate capacitance of this device can be explained with conventional n-type MOS theory because the pn-junction capacitance is shorted to AC ground through the drain. In the punch-through mode, where the channel becomes completely depleted of carriers, the channel is de-coupled from the AC ground at the drain, and the pn junction capacitance is in series with the MOS capacitor [54].

The measured 10 kHz gate-to-substrate capacitance for different diode voltages is plotted with solid lines in Fig. 2.8 for a 200x200 μm BCGD. These

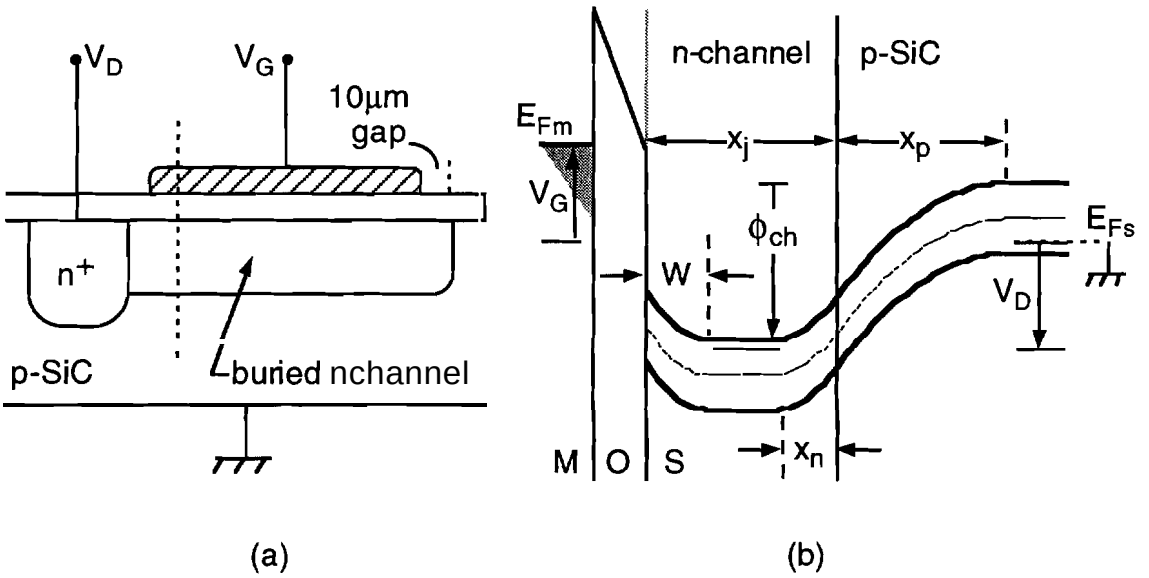


Figure *2.7*

(a) Schematic cross section of the buried-channel gate-controlled diode formed by ion implantation. The 200x200 µm gate extends over the channel region only. (b) Band diagram along the vertical dashed line in (a) showing the potential well created by the n-channel.

room temperature measurements are obtained in the dark at a gate bias ramp rate of 0.25 V/s. The surface is in accumulation for $V_G > V_D + V_{FB}$, where the measured capacitance per unit area is equal to C_{ox}. Decreasing the gate voltage V_G below $V_D + V_{FB}$ creates a surface depletion layer that adds a depletion capacitance in series with the oxide capacitance. A plot of $(A/C)^2$ vs. V_G is linear in the depletion portion of each curve, indicating a uniform doping of 4.9×10^{17} cm^{-3}. The flatband voltage (for $V_D = 0$) is 9.5 V.

If the gate voltage is decreased with $V_D = 0$, the surface goes into deep-depletion before inverting. This behavior is typical of an MOS structure that contains deep-level interface states that cannot stay in equilibrium with the sweeping gate bias [16]. In Fig. 2.8, the reverse and forward sweep is shown for $V_D = 0$ to illustrate the hook and ledge phenomena as seen in Section 2.1.1.1 for the 6H-SiC inversion-channel GCD. The total number of surface states over the majority of the bandgap is again 4×10^{12} cm^{-2}, determined from the magnitude of the voltage shift AV. Evidence of such a large surface state ledge indicates an instability of CCD operation at room temperature, unless bias values are limited to prevent holes at the surface.

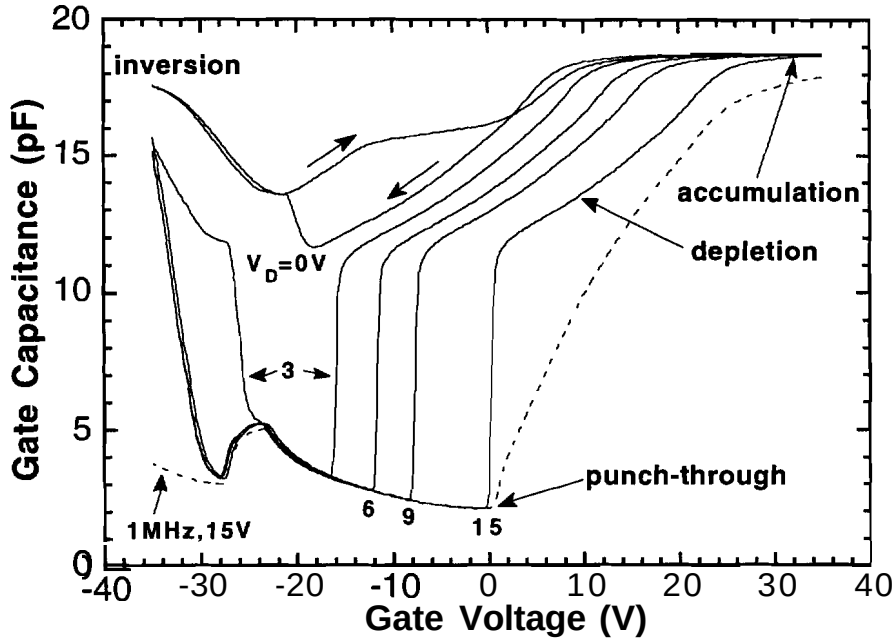


Figure 2.8

Gate capacitance of the buried-channel gate-controlled diode for different diode voltages. The solid curves are taken at room temperature in the dark at a frequency of 10kHz. Gate area is 4×10^{-4} cm^2, channel doping is 4.9×10^{17}cm^{-3}, and oxide thickness is 736 Å

For sufficient positive diode bias, the surface depletion region merges with the junction depletion layer before inversion occurs. The punch-through condition is seen in Fig. 2.8 by a precipitous drop in capacitance. Punch-through isolates the channel from the drain, so the capacitance measurement must include the junction depletion capacitance in series. The total capacitance per unit area just after punch-through is given by

$$\frac{1}{C} = \frac{1}{C_{ox}} + \frac{1}{C_d} + \frac{1}{C_J}, \tag{2.2}$$

where

$$C_d = \frac{K_S \varepsilon_o}{x_j - x_n} \qquad \text{and} \qquad C_J = \frac{K_S \varepsilon_o}{x_p + x_n} \tag{2.3}$$

The channel thickness x_j is the junction depth of the shallow n-layer, and x_n and x_p are the n- and p-side depletion widths of the junction, respectively. With a completely depleted channel, the potential distribution under the gate is

independent of V_D and controlled by the gate voltage only. Further decrease in gate voltage causes a decrease in the p-side depletion width, and the total capacitance increases slowly in punch-through. A plot of $(A/C)^2$ vs. V_G for the data in the punch-through regime is linear and gives a p-epilayer doping of about $1x10^{16}\,cm^{-3}$.

Moving negatively along the gate voltage axis, the capacitance reaches a local maximum. At this point, the potential minimum of the channel becomes sufficiently reduced with respect to the substrate, allowing holes to flow towards the surface. These minority-carrier holes empty the deep-level interface states of their trapped charges. Thus, the device experiences a flatband shift, as in the hook section of the V_D=0 curve. Inversion occurs after all of the surface states are equilibrated, and the capacitance rises towards C_{ox}. The supply and removal of holes in the inversion layer cannot efficiently follow the 10 kHz probe signal, and the capacitance does not saturate before the end of the sweep.

A C-V_G sweep at 1 MHz and V_D=15V is plotted in Fig. 2.8 with a dashed line to demonstrate the effects of test frequency on the measurement. In depletion and accumulation, the capacitance is reduced by the resistance of the channel. After inversion, the HF capacitance saturates even more slowly than at 10 kHz, further demonstrating the inefficient supply of holes from the substrate.

The electrostatic potential minimum ϕ_{min} and its location W_{min} in a depleted channel are important parameters for describing the operation of buried-channel devices. ϕ_{min} is the channel potential at punch-through, which is equal to the diode potential V_D plus the built-in voltage V_{bi} between the channel and substrate. W_{min} is calculated by [54]

$$W_{min} = \frac{K_S t_{ox}}{K_{OX}\left(\frac{C_{OX}}{C_P} - 1\right)}, \qquad (2.4)$$

where C_P is the gate capacitance just before punch-through. Experimental values of W_{min} and ϕ_{min} are found from the knee of each curve in Fig. 2.8 and plotted versus gate voltage in Fig. 2.9. Two sets of data points are plotted for each ordinate in Fig. 2.9 to represent the uncertainty in choosing the punch-through voltage V_P and capacitance C_P. Note that W_{min} does not change significantly over the range of diode voltages used, as expected from the

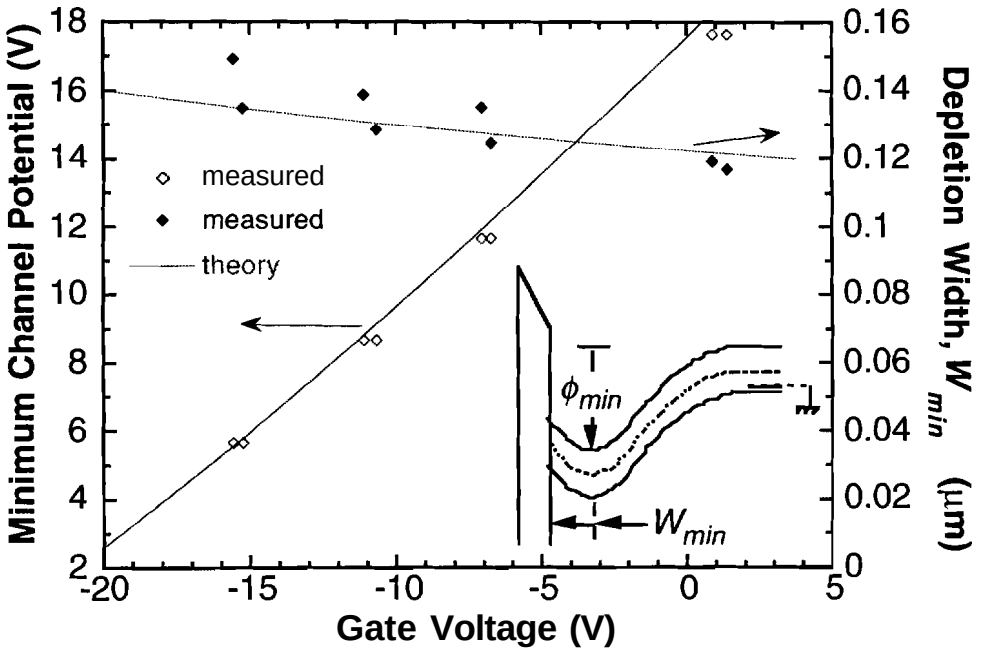


Figure 2.9

Channel potential and surface depletion width versus gate voltage for the device in Fig. 2.7. The duplication of data for each parameter represents the uncertainty introduced when graphically choosing the values for Cp and Vp. The theoretical curves are calculated using V_{FB}=9.5 V, N_D=4.9x10^{17} cm^{-3}, N_A =1x10^{16} cm^{-3}, t_{ox}=736 Å, and x_j=0.16 μm.

relatively high impurity concentration in the channel. Theoretical curves for W_{min} and ϕ_{min} are calculated from a standard potential distribution model [55] and plotted with the data in Fig. 2.9. The relevant device parameters used for the calculations are V_{FB}=9.5 V, t_{ox}=736 Å, x_j=0.16 μm, N_D=4.9x10^{17} cm^{-3}, and N_A=1x10^{16} cm^{-3}. The agreement between measured and calculated data is excellent.

2.2.2.2 Buried-Channel MOSFET

The transport capabilities of a buried-layer structure are of primary interest to the design of buried-channel devices. Electron mobility and transconductance are best investigated with current-voltage measurements of a buried-channel MOSFET. Depending on the bias conditions, four general

operating modes are possible: accumulation, depletion, pinchoff, and inversion. However, the device is normally used only in the depletion and pinchoff modes in CCD applications. Fortunately, the current-voltage models and parameter extraction techniques for these modes have been extensively developed [56]-[59]. In the following section, a SiC BC MOSFET is analyzed to determine electron mobility in the channel μ_n and the channel thickness x_j.

The 6H-SiC BC MOSFET is fabricated during the same processing run as the BCGDs in the previous section. Two n^+ islands on opposite sides of the n-channel are used for source and drain contacts, and test devices of circular geometry are investigated. Figure 2.10 shows a representative cross-section of the circular BC MOSFET. The source is held at the ground potential so that the gate bias V_{GS}, drain bias V_{DS}, and substrate bias V_{BS} are all referenced to the channel potential at the inner radius, $r=r_i$. Note that this configuration is different from that of the BCGD measurement (cf. Figs. 2.7 and 2.10), where the substrate is grounded. From the C-V characterization of the GCD, we know that the doping concentration of the channel N_D is 4.9×10^{17} cm^{-3}, V_{FB} is 9.5 V, and inversion occurs before punch-through unless the channel to substrate junction is reverse biased. The last item indicates that the current of the BC MOSFET is not expected to turn off without the application of a negative backgate bias

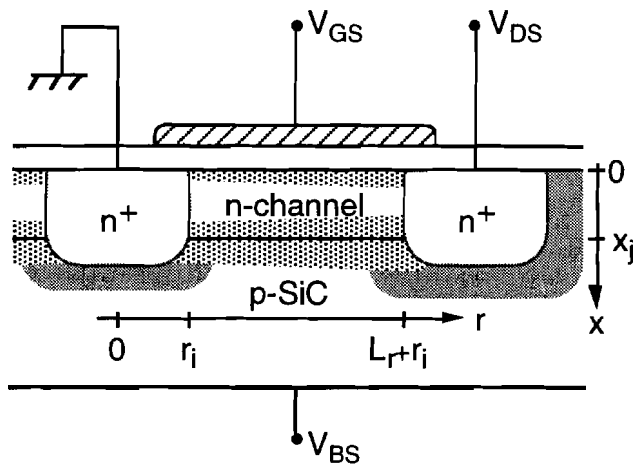


Figure 2.10

Schematic cross section of the circular buried-channel MOSFET. The channel has an inner radius of r_i, radial length L_r, and junction depth x_j. The drain, gate, and backgate biases are referenced to V=0 at $r=r_i$. The channel and substrate have doping concentrations of $N_D=4.9\times10^{17}$ cm^{-3} and $N_A=1\times10^{16}$ cm^{-3}, respectively.

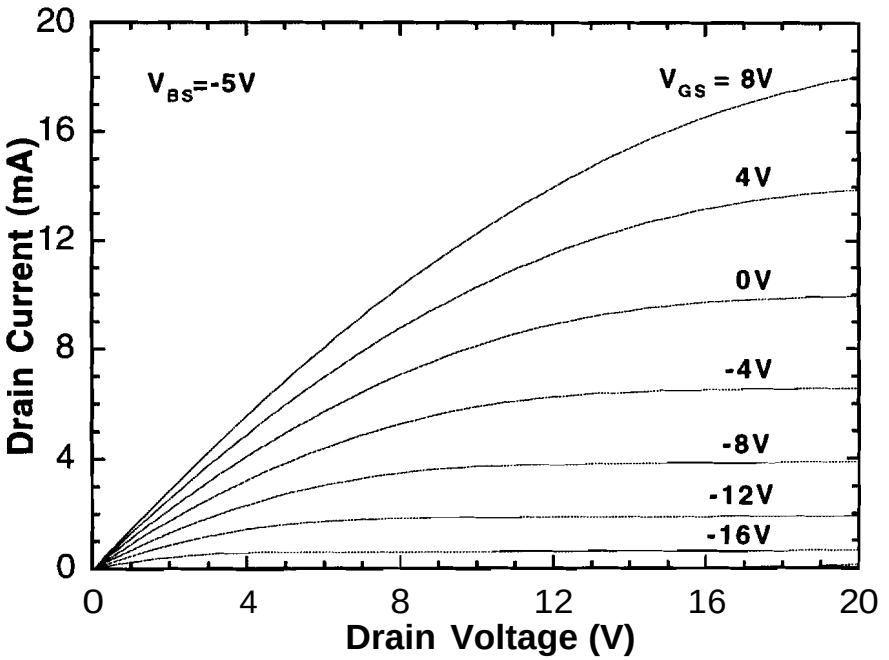


Figure 2.11
Drain current versus drain voltage for a circular BC MOSFET with r_i=45 μm and L_r=20 μm. The effective channel width is 283 pm. The current is measured at room temperature in the dark at a substrate bias V_{BS}=-5 V.

(V_{BS}<0), categorizing this device as a deep-depletion MOSFET [57].

The room temperature output characteristic of a circular transistor with channel inner radius 45 μm and channel length 20 μm is given in Fig. 2.11. Since the C-V data in Fig. 2.8 indicates that a channel-to-substrate bias of at least 3 V is necessary to punch through the buried channel, the data in Fig. 2.11 are measured with a V_{BS}=-5 V. Note that the gate voltages are below V_{FB}, so the current in Fig. 2.11 represents operation in the depletion mode. The transistor shows good saturation characteristics at the more negative gate voltages. At a gate voltage more negative than -16 V, the channel becomes completely depleted of mobile carriers, and the drain current is pinched-off.

The current of the circular MOSFET for V_{DS}=50 mV is plotted versus V_{GS} in Fig. 2.12 for eight values of back-gate bias (ΔV_{BS}=-3 V). As expected, the current cannot be turned off by the gate voltage unless a V_{BS}<0 is applied. In fact, the current increases for V_{BS}=0 and -3 V because the device enters the inversion mode, at which point a shift in flatband voltage occurs as in the hook portion of the C-V curve in Fig. 2.8. The surface depletion width shrinks in

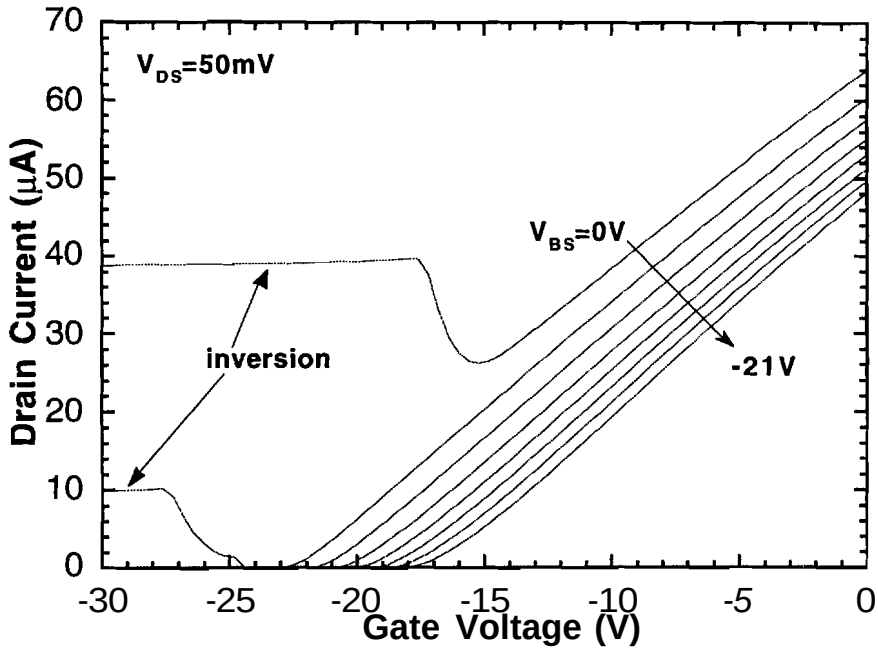


Figure 2.12

Drain current versus gate voltage for the circular BC MOSFET in Fig. 2.10. This device operates as a deep-depletion MOSFET because it cannot be turned off without a backgate bias. Maximum transconductance at low V_{DS} is 10 μS/mm.

response to the change of interface state occupancy, which increases the effective channel thickness and conductance of the channel. Current in the inversion mode remains fairly constant because the gate voltage only modulates the surface depletion width W by a minute amount [60]. The maximum transconductance at low drain bias is 10 μS/mm in this device.

In the buried-channel MOSFET, the active channel thickness varies along the length of the device. In the depletion mode of operation, where $V_P < V_{GS} < V_{FB}$, the channel thickness t_c at a point along the radial direction is equal to the metallurgical junction depth x_j minus the surface depletion width W and the n-side depletion of the channel-to-substrate junction x_n,

$$t_c(r) = x_j - W(r) - x_n(r), \tag{2.5}$$

For sufficiently low drain voltages, however, the channel thickness does not vary appreciably along the radius, and the channel can be simply treated as a cylindrical annular resistor of constant thickness t_c, inner radius r_i, and radial

length L_r. Using the depletion approximation and solving Poisson's equation in one dimension, Wand x_n are expressible as [55]

$$W = \sqrt{(t'_{ox})^2 - \frac{2K_S\varepsilon_o}{qN_D}(V_G - V_{FB})} - t'_{ox} \tag{2.6}$$

$$x_n = \sqrt{\frac{2K_S\varepsilon_o}{qN_D}\left(\frac{N_A}{N_D + N_A}\right)(V_{bi} - V_{BS})}, \tag{2.7}$$

where V_{bi} is the built-in potential of the channel-to-substrate junction, and N_A and N_D are the substrate and channel doping concentrations, respectively. t'_{ox} is an abbreviation for $K_S t_{ox}/K_{OX}$ where K_S=10 [3] and K_{OX}=3.9 [60] are the relative dielectric constants for 6H-SiC and SiO_2, respectively. The resistance of an annular resistor of thickness t_c is [61]

$$R = \frac{ln(1 + L_r/r_i)}{2\pi}\left(\frac{1}{qn_{ch}\mu_n t_c}\right), \tag{2.8}$$

where μ_n is the electron mobility in the n-channel, and n_{ch} is the electron concentration in the undepleted part of the channel. Note that n_{ch} will be less than N_D if the dopant atoms are not completely ionized at the temperature of interest. Finally, the drain current of this circular device is given by the ratio of the drain voltage and the resistance in Eq. (2.8),

$$I_{DS} = \kappa V_{DS}(x_j - W - x_n), \tag{2.9a}$$

$$\kappa = \frac{2\pi q n_{ch}\mu_n}{ln(1 + L_r/r_i)}, \tag{2.9b}$$

Equation (2.9a) is also valid for a linear transistor of length L and width Zfor which κ becomes

$$\kappa = qn_{ch}\mu_n \frac{Z}{L}. \tag{2.9c}$$

An analytical expression for the pinchoff voltage is obtained from (2.5)-(2.7) by setting the channel thickness to zero,

$$V_P = V_{FB} - qN_D x_j\left(\frac{1}{C_{ox}} + \frac{1}{2C_j}\right) - \left(\frac{N_A}{N_D + N_A}\right)(V_{bi} - V_{BS}) + \left(\frac{1}{C_{ox}} + \frac{1}{C_j}\right)\sqrt{2K_S\varepsilon_o q\left(\frac{N_A N_D}{N_D + N_A}\right)(V_{bi} - V_{BS})} \quad (2.10)$$

where C_j is the channel capacitance per unit area given by $K_S\varepsilon_o / x_j$. By assurning $N_D \gg N_A$, (2.10) simplifies to

$$V_P = V_{FB} - qN_D x_j\left(\frac{1}{C_{ox}} + \frac{1}{2C_j}\right) + \left(\frac{1}{C_{ox}} + \frac{1}{C_j}\right)\sqrt{2K_S\varepsilon_o qN_A(V_{bi} - V_{BS})}. \quad (2.11)$$

From Eq. (2.11), a plot of V_P versus $\sqrt{(V_{bi} - V_{BS})}$ is linear, and the slope and y-intercept give the metallurgical junction depth and channel doping, respectively.

For each curve in Fig. 2.12, ***Vp*** occurs where the current drops to zero. These values of ***Vp*** are plotted versus $\sqrt{(V_{bi} - V_{BS})}$ in Fig. 2.13. The slope of a linear fit gives a metallurgical junction depth x_j equal to 0.16 µm. With the previously determined value of V_{FB}=9.5 V and the y-intercept of -27.29 V, the n-channel doping concentration is calculated to be $4.7\text{x}10^{17}$ cm^{-3}. This value of N_D is in good agreement with the differential capacitance result presented in the previous section. The total dose, given by the product $N_D x_j$, is also very close to the intended value of $7.5\text{x}10^{12}$ cm^{-2}.

Evaluation of (2.7) and (2.9) suggests that the mobility-concentration product ($n_{ch}\mu_n$) can be estimated from the slope of an I_{DS} vs. $\sqrt{(V_{bi} - V_{BS})}$ plot. The channel mobility can then be extracted if n_{ch} is known. In 6H-SiC, the nitrogen donor level is 84 meV below the conduction band [62]. Consequently, not all the nitrogen donors are ionized at room temperature, and the bulk carrier concentration is less than the doping concentration, $n_{ch} < N_D$. The electron density can be calculated by employing Fermi statistics and the condition of charge neutrality in the semiconductor bulk [63]. Assuming a donor state degeneracy of two (g_d=2), a six-fold symmetry of conduction band minima (M_C=6), and an electron effective mass of $0.45m_o$ [62], roughly 70% of the nitrogen donors are ionized at a doping concentration of $4.9\text{x}10^{17}$ cm^{-3}. Therefore, the actual number of mobile carriers in the implanted channel is only $3.4\text{x}10^{17}$ cm^{-3}.

A plot of I_{DS} versus $\sqrt{(V_{bi}-V_{BS})}$ is shown for the SiC BC MOSFET in Fig. 2.14 for several values of gate voltage, a drain voltage of 50 mV, and a built-in voltage of 2.65 V. The solid line represents the flatband voltage of 9.5 V. Below this line, the device operates in the depletion mode. Therefore, electron mobility is calculated from (2.9) and the slope of the linear data with

$$\frac{1}{\mu_n} = \frac{V_{DS}}{-m}\frac{n_{ch}}{N_D}\frac{2\pi}{\ln(1+L_r/r_j)}\sqrt{2K_S\varepsilon_o q\left(\frac{N_D N_A}{N_D+N_A}\right)}. \qquad (2.12)$$

Below flatband, the mobility increases monotonically from about 140 to 180 cm^2/Vs with decrease in gate voltage. The simple current model in (2.9) assumes that electrons experience only bulk mobility, even for the smallest surface depletion widths. However, even though the majority carriers are confined from the surface by the built-in electric field of the surface depletion, interaction with fixed charges at the surface is still possible for depletion widths of several hundred angstroms. With increased depletion width, the carriers experience less scattering, and the experimentally measured mobility increases. Another possible reason for the decrease in extracted mobility is the effect of series resistance on the measurement for higher values of drain current. The largest value of mobility is comparable to electron mobilities previously quoted for SiC epitaxial JFETs [8], [18] of the same doping concentration. However, 180 cm^2/Vs is 30% lower than recently reported Hall mobilities on epitaxial 6H-SiC [64], also for the same donor concentration. Since Hall mobilities are consistently higher than values extracted from FET current measurements, it is unclear whether the channel mobility extracted above is lower because of implantation or because of an artifact of the two different measurements.

2.3 Summary and Conclusions

In order to compare surface-channel and buried-channel structures in 6H-SiC, inversion-channel and buried-channel MOS devices have been fabricated by ion implantation and thermal oxidation. Gate-controlled diodes and MOSFETs are used to determine mobility, doping, and surface state charge

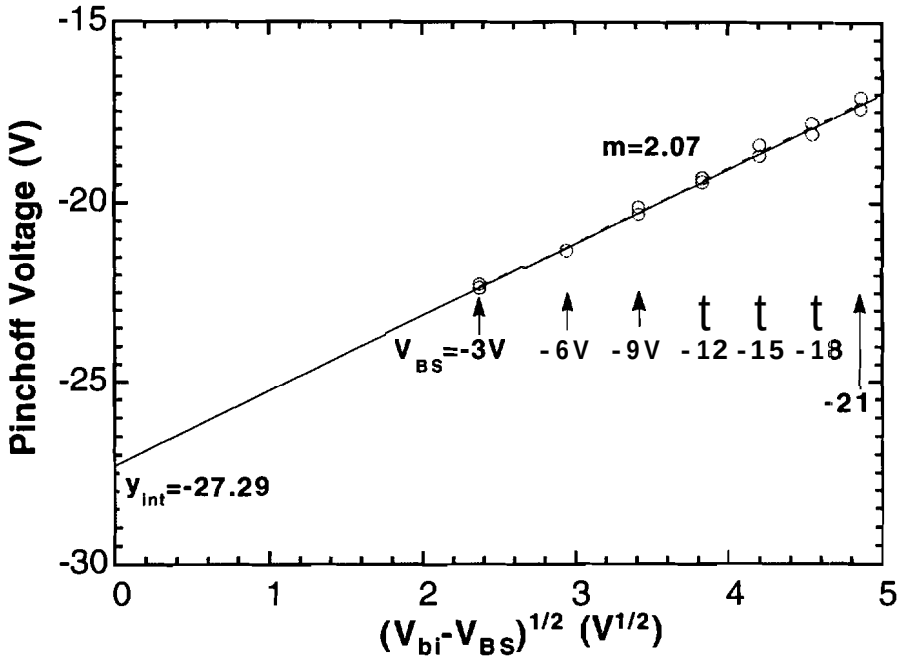


Figure 2.13

Pinch-off voltage versus $\sqrt{(V_{bi}-V_{BS})}$ from the data of Fig. 2.12. Junction depth x_j=0.16 μm is extracted from the slope, while channel doping N_D=4.7x10^{17} cm^{-3} is found from the y-intercept, confirming a built-in voltage of about 2.65 V.

as well as threshold voltage, transconductance, pinchoff voltage, and flatband voltage.

The 6H-SiC MOS capacitor at room temperature operates; much like a silicon device at 77K. Surface centers that reside deep in the 3.0 eV bandgap of this material cannot respond to sweeping gate bias because of the slow emission rates. When the n+p junction of a gate-controlled diode is used as a source of inversion charge, the surface state density of this device is found to be about 4x10^{12} cm^{-2}. The low-drain-bias current response of an inversion-channel MOSFET offers additional information about the SiC-SiO_2 interface. Typical electron surface mobilities of 20 cm^2/Vs are obtained from the linear portion of this measurement, and the transconductance for a circular device of 5 μm length is 10 μS/mm.

The buried-channel MOS devices presented here are the first to be reported for the 6H polytype of SiC. The C-V characteristics clearly show four regions of operation: accumulation, depletion, punch-through, and inversion.

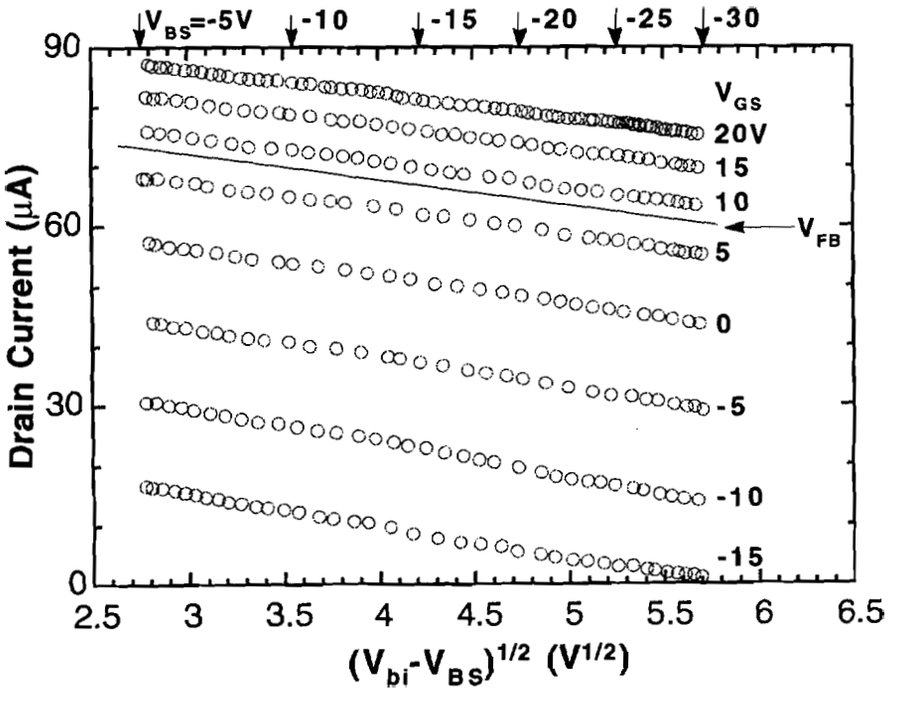


Figure 2.14

Drain current versus $\sqrt{(V_{bi}-V_{BS})}$ for several gate voltages and V_{bi} =2.65V. Specific values of V_{BS} are shown at the top of the diagram. Flatband is represented by the solid line. In depletion, the channel mobility increases with decreasing V_G from 140 to 180 cm^2/Vs.

The electrostatic potential minimum ϕ_{min} and its depth from the surface W_{min} are calculated from the punch-through conditions at each diode voltage. These values correspond well to those calculated with a one-dimensional depletion model.

The 6H-SiC BC MOSFET is characterized with a simplified drain current expression to extract information on the implanted channel. The variation of pinchoff voltage with respect to substrate voltage allows us to calculate a channel doping of $4.7\text{-}4.9\times10^{17}$ cm^{-3} and a metallurgical junction depth of 0.16 μm. The mobility of electrons decreases from 180 cm^2/Vs far into the depletion mode to 140 cm^2/Vs near flat band. The electron mobility in these implanted channel MOSFETs is comparable to those in epitaxial channel JFETs for the same doping.

CHAPTER 3 - PRINCIPLES OF CCD OPERATION AND DESIGN

Demonstration of the various SiC field effect devices in Chapter 2 establishes a baseline fabrication process and characterization procedure for more complicated MOS devices such as the CCD. It would seem that a mere extension of these techniques could be applied to design, fabricate, and operate a textbook example linear shift array. The classic charge-coupled device, first fabricated in silicon at Bell Labs over twenty years ago [27], [53], has been meticulously investigated and improved upon. Also, the operation of the CCD is well understood, and it now serves as an excellent example of advanced MOS semiconductor devices in silicon [52]. Therefore, duplicating the CCD in SiC presents a well-known example of a charge transfer device and gives a sound basis for further development of an imager. Unfortunately, the physics of such a device, whether a surface channel or buried channel, cannot be oversimplified when investigating this technology in a different material system. In addition, because of the relatively young state of silicon carbide fabrication technology, many special considerations must be taken in order to make the device.

In the following chapter, an overview of charge-coupled device fundamentals is given. In many texts and review papers describing CCD technology [31], [66], discussions focus on the physics of the surface channel device (SCCD) with only brief coverage or short, analogous references made to the buried channel device (BCCD). This is mainly due to the simpler nature of the SCCD and the fact that basic operation techniques can apply to both devices. Some scientific papers have examined specific problerns to consider when designing the BCCD [33], [39], [67], [78]. The purpose of Chapter 3 is to address these problems and present special information pertaining to the SiC BCCD. The bulk of Section 3.1 contains the more general aspects of the CCD, including a standard device description and a detailed discussion of the typical one dimensional model used for analysis. In Section 3.2, this model is used to

consider design concepts such as operating voltages, dynamic range of charge capacity, breakdown 'field limitations, and preventing weak inversion at the n-type surface.

3.1 Buried-Channel CCD Fundamentals

The following introduction to the buried-channel CCD includes many aspects of the fundamental operation of the CCD, including charge confinement, signal charge injection and readout, and charge transfer. Many of the main concepts are drawn from authoritative references in the field, Schroder [52], Kim [66], and Hobson [67].

3.1.1 Device Description

The construction of a BCCD can be likened to that of a long buried-channel MOSFET with a series of separate gates, as shown in Fig. 3.1 (a) (cf. Fig. 2.10). Instead of a continuous flow of carriers from source to drain, a packet of charge is shifted from input to output by switching the most positive voltage to each successive gate. The gates along the device are interconnected in a periodic manner to form the phases of the CCD. As will be explained later in this section, the chosen interconnect scheme designates the number of clocking voltages required to sustain a unidirectional transfer. The device in Fig. 3.1 (a) is, of course, a four phase structure. This idea of having a switched analog shift register served as the original concept for which CCDs were developed [73].

3.1.1.1 Charge Confinement

Recall from Section 2.3 that an n-channel between oxide and p-type substrate serves to form a potential well for electrons away from the surface. A positive voltage V_{ch} applied to the n-layer reverse biases the PN junction and the surface under the gate, causing the two opposing depletion widths to spread into the n-layer. For V_{ch} sufficiently high, the channel becomes

completely depleted as shown in the band diagram in Fig. 3.1 (b) and under phases Φ_1 and Φ_3 in Fig 3.1 (a). A signal charge packet introduced into the device alters the band diagram as shown in Fig. 3.1 (c). The charge under Φ_2 or Φ_4 in Fig 3.1 (a) is simply an undepleted portion of the well that is vertically confined from the surface. The charge per unit area (C/cm^2) is defined as the undepleted thickness multiplied by the carrier density in the channel times the unit of electronic charge,

$$Q_n = -qN_D\left(x_j - x_n - W\right). \tag{3.1}$$

The channel regions towards the center of the CCD are electrically decoupled from the external terminal voltages at input and output:. Therefore, the vertical potential distribution under a given phase is a function only of the phase voltage and the amount of charge contained in the well. This is the basic operating principle of the CCD and will be investigated later to aid in explaining the physics of the device. Fig. 3.2 (a) shows several possible vertical potential distributions under the phases in Fig. 3.1 (a). The curves are shown with electrostatic potential as positive downwards in order to facilitate the common analogy of potential wells; electrons in a potential well are likened to water in a bucket. The dashed line exhibits the empty potential well under Φ_1 and Φ_3 when at zero gate voltage, and the two solid curves represent the profiles under Φ_2 at a positive voltage with (upper) and without (lower) signal charge.

Fig. 3.2 (b) introduces the potential minimum diagram, also called the channel potential diagram, which is instrumental in visualizing the influence of phase voltages on the lateral potential minimum in the channel. Corresponding to the vertical potential wells plotted in the adjacent figure, the potential minimum under Φ_2 is "lower" than the surrounding phases, forming a well also in the lateral direction (y-direction). In this way, a charge packet is confined in the potential well that is formed by the three phases. The solid lines in the potential minimum diagram represent zero charge under the phase. The addition of charge (denoted by the shaded region) fills the well and reduces the potential. Note that the potential distribution under Φ_2 is changed significantly when charge is present in the channel.

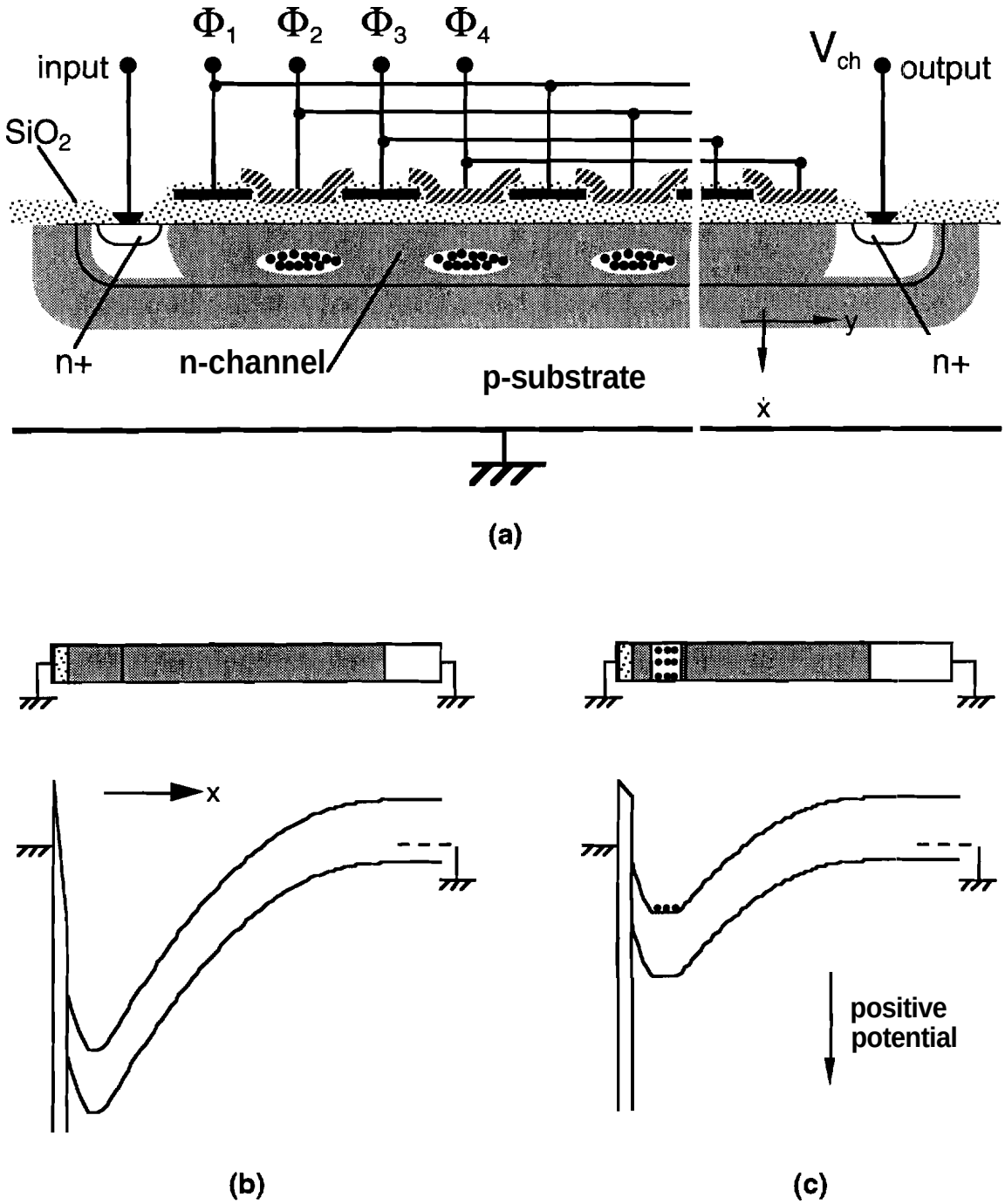


Figure 3.1

Schematic cross section of a four phase buried-channel CCD. The n-layer between oxide and p-layer in (a) forms a potential well for electrons, shown in (b) and (c). A fully depleted layer (b) has zero signal charge. A charge packet raises the potential well minimum in (c).

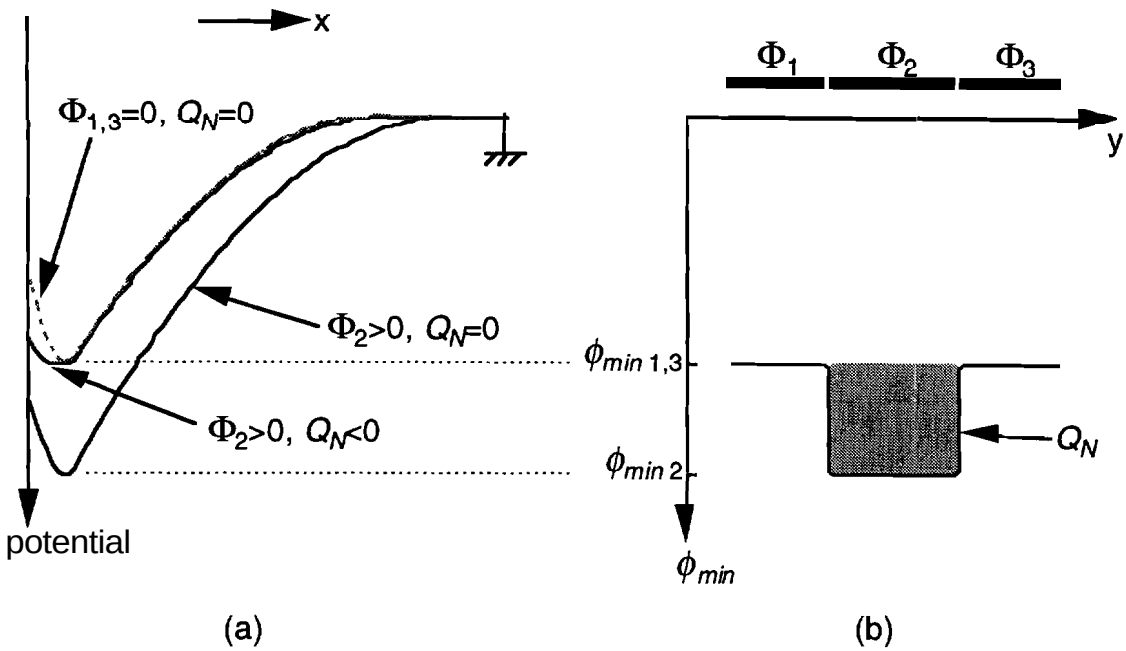


Figure 3.2

Charge confinement by three phases in a BCCD. Phase voltage and stored charge modify the vertical potential distributions in (a). The potential minimum diagram in (b) shows the lateral confinement of the charge packet.

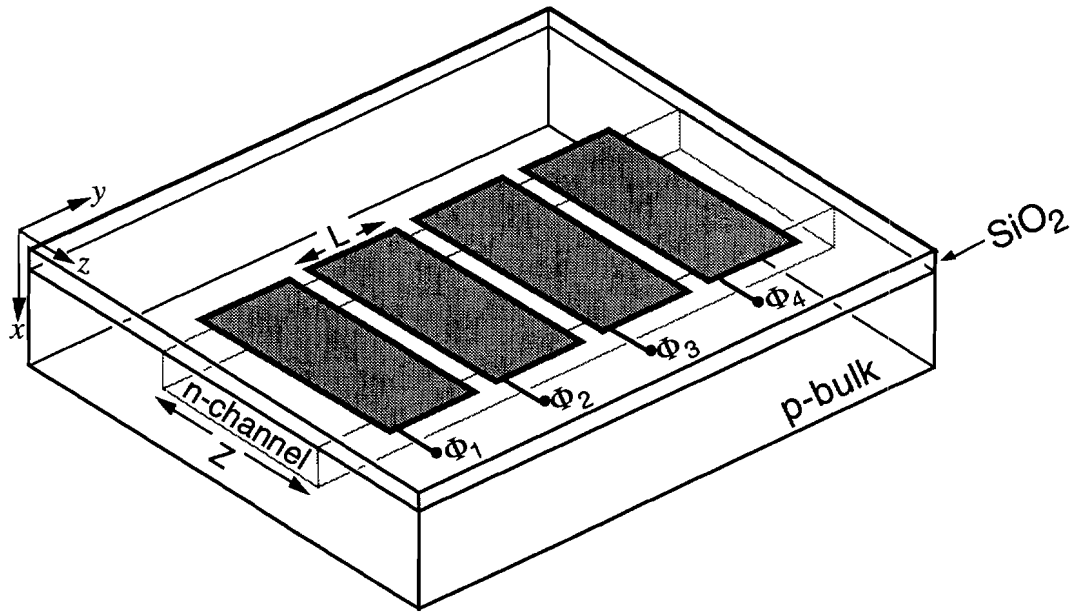


Figure 3.3

A crude three-dimensional (3D) view of the general CCD structure. Charge is confined in the lateral z-direction by the reverse biased PN junction. The total amount of charge in a packet is $Q_N = ZLQ_n$ (C).

A rudimentary 3-dimensional picture of the basic CCD structure is shown in Fig. 3.3. It shows that lateral confinement in the z-direction is maintained by the reverse biased PN junction. The gates of the CCD must extend past the n-channel in order to ensure pinchoff of the entire width. The total amount of charge under a given phase is approximated as the product of charge density and electrode area over the channel, $Q_N = ZLQ_n$. The existence of a parasitic surface channel CCD at the edges of the n-channel can be prevented with a p^+ channel stop implant (not shown), which are generally used to make the p-surface insensitive to the fixed oxide charge and any mobile surface contamination. Using the "chan-stop" alone causes an unacceptable increase in stray wiring capacitance, so a thick field oxide can also be used outside the channel area. In Si, local oxidation or LOCOS [68] is commonly used to selectively grow thick oxides, but initial attempts with the LOCOS technique in SiC have seen marginal success [69], [70].

3.1.1.2 Charge Transfer

Given that the charge packet is confined properly under a single CCD phase, charge transfer along the device is accomplished by proper sequencing of the phase voltages such that the potential well in Fig. 3.2 (b) moves from input to output. In certain implementations of the BCCD, charge transfer is likened to the wavelike action of peristalsis in organs of the body [71], [67]. Generally, overlapping clock waveforms are needed with a three phase CCD in order to guarantee unidirectional charge transfer. This action is demonstrated in the potential minimum diagrams in Fig. 3.4. Given a charge packet under Φ_2, a barrier against backwards flow is maintained by a low potential under Φ_1. The charge moves forward after an abrupt reduction in the barrier under Φ_3 (i.e., the voltage on Φ_3 is clocked more positive). In a scheme called *push clocking* [72], a slow fall time on the clock of Φ_2 pushes the entire amount of charge into a potential under Φ_3. In general, the clock transition on the receiving well can be abrupt, but the sending well must by raised slowly to prevent any charge from spilling backwards over the barrier [67].

The number of phases required to confine a charge packet (without backwards transfer) defines a stage of the CCD. The clocks are synchronized

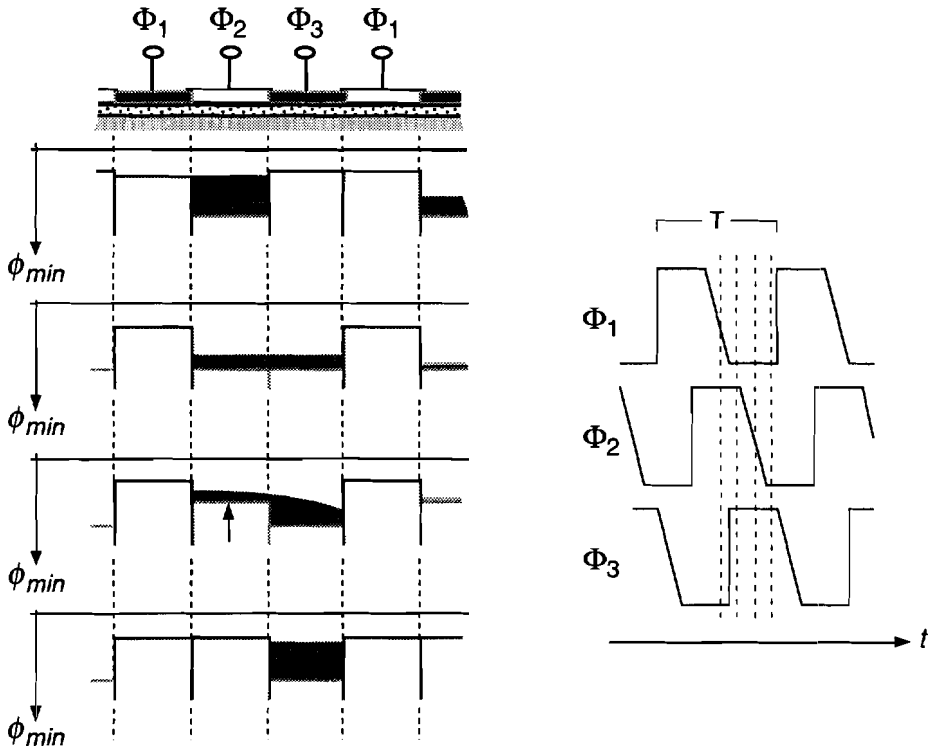


Figure 3.4
Pictorial of charge transfer in the 3 phase CCD with the overlapping waveforms that demonstrate push clocking.

to transfer the charge through the entire stage in one clock period. So, in the three phase device, the charge packet is moved three times before the next period begins.

The drawbacks of the three phase structure are, of course, the number of clock signals required and the relative complexity of waveforms needed for push clocking. Unidirectional transfer of charge can be cleverly achieved with a two phase structure if a potential well asymmetry is incorporated under each phase such that a well is formed in the direction of charge transfer. The V_G vs. ϕ_{min} relationship is altered under one half of each phase by using a different oxide thickness [73] or implanting impurities [74] so as to form a barrier on the input side. In the case of a BCCD, a thinner oxide or implanted donors are used to create a barrier under part of each gate. Although these methods add complexity to the fabrication process, other steps that are needed to complete a three phase device can be eliminated. Additionally, the two phase device is simpler to operate because only two clock waveforms are required, and they

need not overlap or have specially designed fall times (drop clocks [75]). These simplifications also make the two phase device more amicable from a systems standpoint.

3.1.1.3 Signal Charge Input

The charge input to a CCD that is used in an optical imager is generally due to optically generated carriers collected at the most positive potential of each stage. For purposes of electrical characterization and other early applications of CCD circuits (delay lines, signal processing, memories, etc.), controlled electrical injection of charge is necessary. Modern imagers can actually utilize electrical injection of background charge (called the fat zero) to reduce effects of trapping and increase transfer efficiencies [73]. Charge injection is realized quite easily in the buried channel device with an ohmic contact to the channel. Two input gates, whose voltages are controlled separately from the phase clocks, are used to control the size of the charge packet.

Consider the input configuration shown in Fig. 3.5. The connection to the channel at V_S is usually facilitated by a shallow n^+ region under the contact. An input voltage V_{in} is connected between the two input gates such that V_{G2} is always more positive than V_{G1} (here V_{in} is assumed positive). Then V_{G1} can be dc-biased to obtain a desired constant value of channel potential, ϕ_{minG1}. Before any charge is input to the well under V_{G2}, the source is biased to a potential higher than ϕ_{minG1}. During the half clock period that Φ_1 rests at its lower value, the source voltage is pulsed to a value lower than ϕ_{minG1}. At this point, the source voltage effectively sets the channel potential under both input gates by filling the whole region with electrons. Care must be taken to avoid reducing V_S below the channel potential set by Φ_1, so as to not inject charge directly into the CCD proper. When the source bias returns back to its original value, the excess charge residing under the input gates spills back into the contact. A certain amount of charge will remain under V_{G2} due to the barrier caused by a less positive V_{G1}, and the channel potential under both input gates will be identical. Hence, this method is known as the potential equilibration

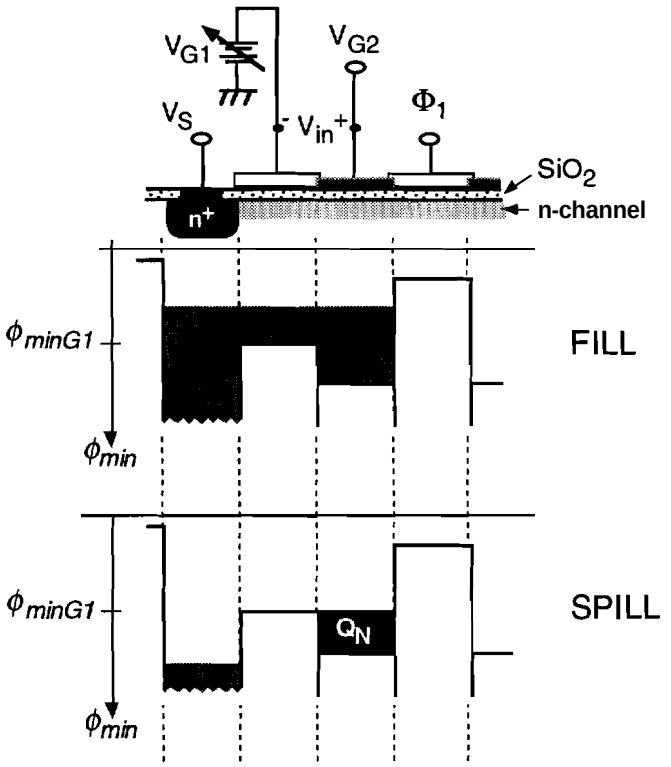


Figure 3.5
Electrical injection of charge by the potential equilibration or "fill and spill" method.

method, and the magnitude of the charge input is directly metered by the input voltage.

In a surface channel CCD, the metered charge is directly proportional to V_{in} [52]. Unfortunately, the charge to gate voltage relationship for the BCCD is non-linear because (a) the charge packet is spread over an undepleted portion of the channel and (b) the effective distance between the charge and the manipulating gate voltage is not a constant [67]. The issue of charge capacity of the BCCD is discussed in a later section of this thesis after the development of a few important equations.

3.1.1.4 Charge Readout

The output configuration of a CCD plays an important role in interpreting the size of a charge packet that has been transferred along the device. One of the easiest readout schemes to implement is shown in Fig. 3.6. It involves an output reset transistor coupled to the last stage of the CCD via a transfer gate, V_{OG}. The floating n^+ source basically acts as a capacitor that can be reset to a positive potential prior to receiving the signal charge Q_N (C). After potential equilibration to the adjacent channel under the reset gate V_{RG}, the floating region is decoupled from the reset drain by turning off the reset transistor. Next, the electrons are released into the floating node by the output gate, which reduces the preset potential by a voltage that is proportional to the charge magnitude and the total capacitance of the output node,

$$\Delta V_{n^+} \cong \frac{Q_N}{C_{out}}. \tag{3.2}$$

Typically, the total output capacitance is comprised of the overlapping capacitances of the output and reset gates, the n+p junction depletion capacitance, and the input capacitance of the amplifier used to detect ΔV. For a modest value of signal charge 9 (1×10^{11}) C/cm^2, a conservative CCD gate area of 20x100 μm, and an achievable value of 0.6 pF for C_{out}, the voltage swing is about 0.53 V. Strictly, the relationship between charge and voltage swing is not linear due to the voltage dependence of junction capacitance in C_{out}, but Eq. (3.2) is still useful as a rough guideline when designing the output circuit. A more exact relationship is used in Chapter 4 for interpretation of CCD output signals.

Two stringent requirements are placed on the method of measuring the voltage swing of the floating node. First, the input impedance of the circuit must be high enough so that the preset potential does not decay to ground. Also, the input capacitance of the amplifier must not add significantly to the value of C_{out}. In an experimental arrangement, measuring AV by directly probing to the n^+ output node can add a significant shunt capacitance to C_{out} due to cabling and the instrument.

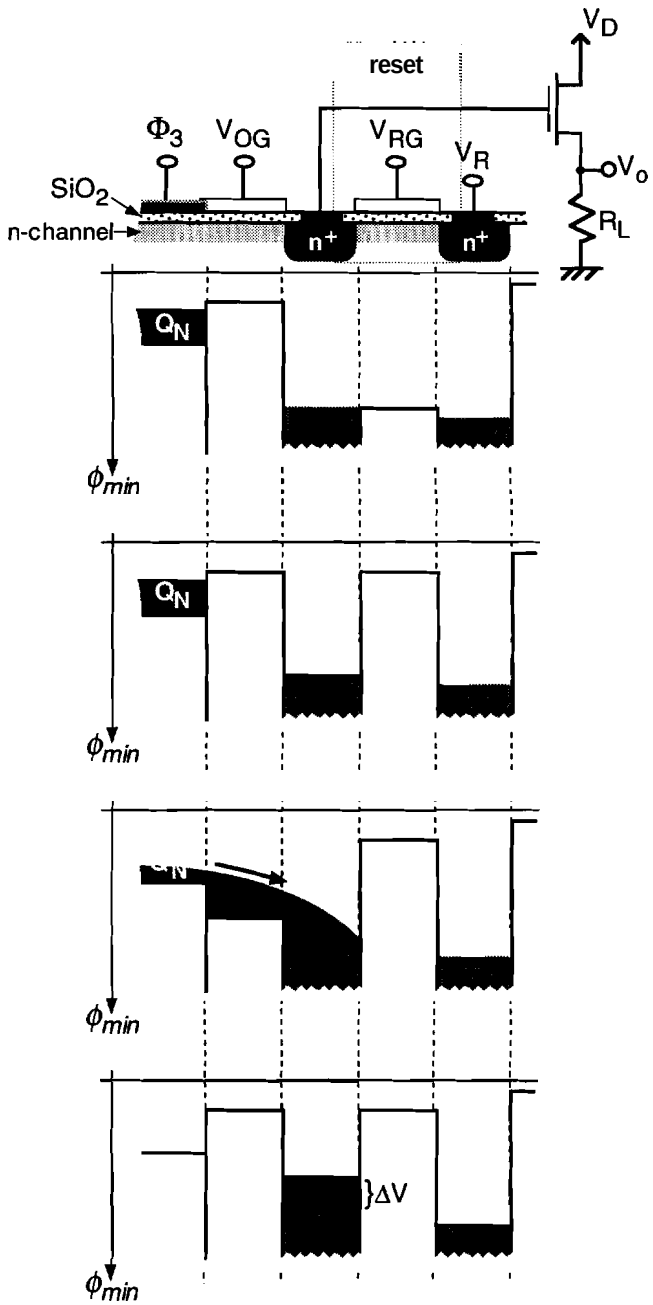


Figure 3.6

Charge readout scheme at the end of a CCD transfer. The voltage swing AV is proportional to the size of the charge packet. The gate of a MOSFET serves as a high impedance, low capacitance connection to the output node.

A sensible arrangement to monitor the floating node is a connection to the gate of a MOSFET that is monolithically integrated with the CCD. The gate capacitance (plus any interconnect capacitance) can be limited to about 0.1 pF, and the input impedance of an ideal MOSFET is infinite. The voltage swing of the output node is transferred directly to the gate of the MOSFET, modulating the drain current according to the transconductance, g_m. Addition of a load resistor (which can be off-chip) in series with the integrated MOSFET completes a simple source-follower buffer amplifier [76], which has a gain equal to $g_m R_L/(1+g_m R_L)$. The measured voltage swing at V_o is related directly to the magnitude of the signal charge by

$$\Delta V_o = \left(\frac{g_m R_L}{1 + g_m R_L} \right) \Delta V_{n^+} . \tag{3.3}$$

3.1.2 Standard Models, 1-D Depletion Approximation

Analytical relationships, including oxide thickness (t_{ox}), n-channel thickness (x_j), n-channel doping (N_D), and background p-layer doping (N_A), provide a useful way to generate design curves for the buried-channel structure and predict operating voltages and charge capacity with good accuracy. Also, when interpreting measurements of a device, the experimental dependence of pinchoff voltage with respect to substrate bias is an excellent source of information on the device structure, if used with an appropriate mathematical model. In setting a basis for comparison to other models discussed later, the depletion approximation is used below to derive a simple one dimensional (1-D) model of the charge, electric field, and potential profiles for a BC structure.

Historically, the operational characteristics of the BCMOSFET have been studied intensely since its introduction as a depletion load in NMOS logic circuits [77]. Although complimentary MOS (CMOS) has largely replaced depletion load NMOS technology in modern silicon VLSI circuits, the early literature concerning the buried n-channel is still of importance to the buried channel charge coupled device (BCCD), MESFETs and Schottky barrier CCDs [78] (in the case of zero oxide thickness), and NMOS logic circuits in SiC [24], where complimentary circuits are not presently realizable. Since the buried n-

channel devices were originally formed by ion implantation of donor atoms into p-type material, exact expressions for the terminal characteristics of a device with a Gaussian implanted profile were obtained [79]. Unfortunately, the cumbersome results hindered physical interpretation of the model. A more amenable formulation for the pinchoff voltage of an ion implanted channel was derived by using a linearly graded distribution [80], but the analysis was limited to the situation of a totally depleted channel and lacked information on the spatial potential distribution in the presence of an arbitrary charge density in the channel.

A more universal model resulted from a transformation of the Gaussian shape to an equivalent box representation [81], [82], allowing the device to be viewed as a uniformly doped n-type MOS capacitor in series with an abrupt NP junction. The advantage of this model, when coupled with the depletion approximation, is its relative simplicity. In order to better utilize the simpler model, device researchers have even tailored multiple implants to make the resulting profile as rectangular as possible [83], [84]. This gives a great deal of leverage to modeling the uniform implant profiles also used for the SiC CCDs.

Consider the vertical slice of the buried-channel MOS device in Figure 3.7 (a), which simply consists of an n-type region inserted between a thin insulating layer of SiO_2 and p-type bulk with a junction at a distance x_j from the surface. The oxide thickness is t_{ox}. Congruent with the operation of a CCD, the substrate p-region is grounded, and no direct terminal connection to the channel region is assumed. A top metal or polysilicon electrode controls the gate voltage, V_G. The analysis of this device is greatly simplified by making use of the depletion approximation [85] and determining electrostatic fields and potentials with the Poisson equation in 1-D. The salient features of the depletion approximation are included here for reference in a discussion of the exact solution in a later section. The 1-D picture is valid because the lateral device dimensions are assumed much larger than the channel thickness, reducing the contribution of any edge effects.

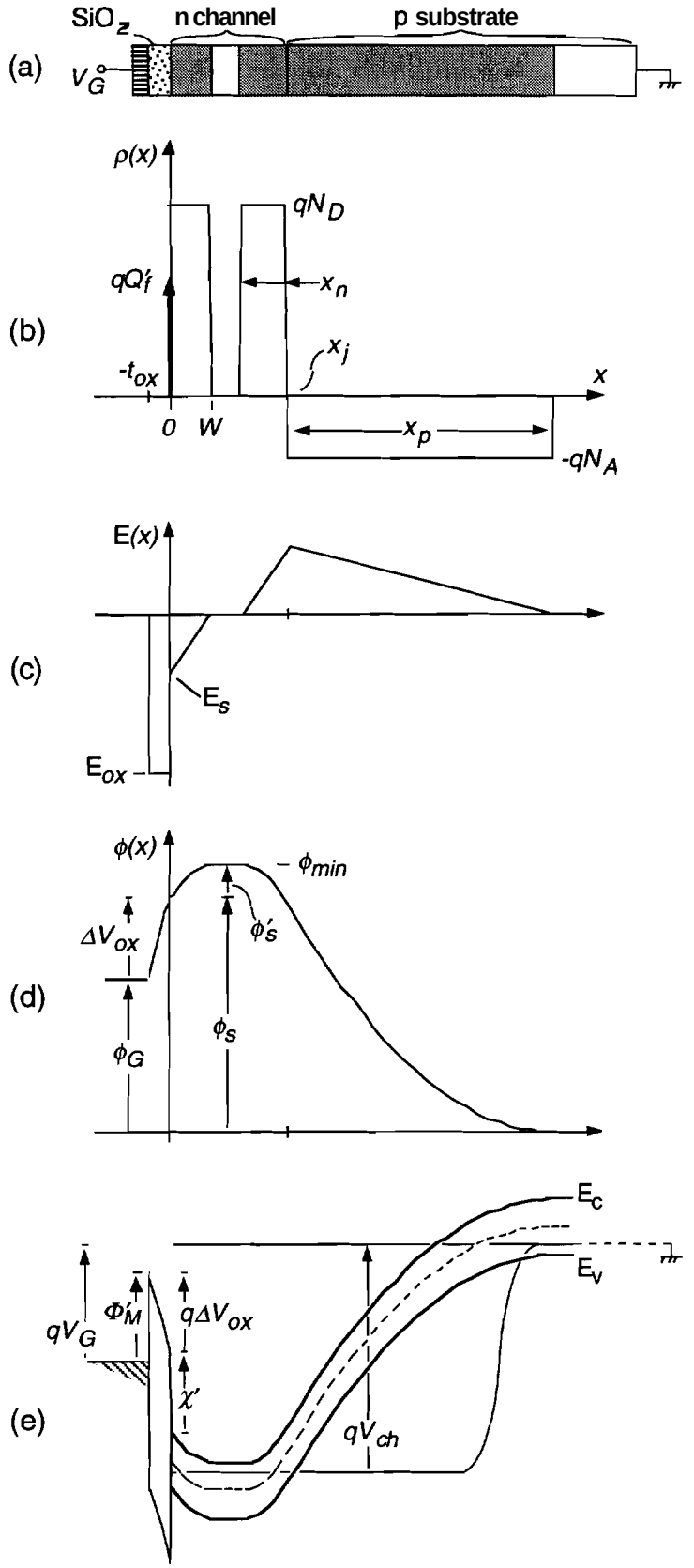


Figure 3.7
Representations of the 1-D space charge, electric field, potential, and energy band profiles in a uniformly doped n-chiannel with abrupt junction.

The net space charge density ρ (coulombs/cm^3) at every point in the semiconductor is equal to the imbalance between the free carriers and active dopant atoms

$$\rho(x) = q(p - n + N_B) \tag{3.2}$$

where N_B is the net active doping concentration at the point x. From electrostatics, the Poisson equation gives that the Laplacian of potential is proportional to space charge density. In one dimension,

$$\frac{d^2\phi}{dx^2} = -\frac{\rho(x)}{\varepsilon_r \varepsilon_o} \tag{3.3}$$

where ε_o is the permittivity of free space and ε_r is the relative permittivity of the medium in which (3.3) is being solved. An exact solution of (3.3) inside a semiconductor is quite involved (even for uniform dopings) since p and n in (3.2) are exponential functions of potential, the unknown. The depletion approximation is a set of assumptions applied to (3.2) to make the closed form solution more tractable.

In the depletion approximation, carrier densities n and p are set equal to zero wherever energy bands are bent away from the majority carrier band. This leaves behind space charge equal to the net doping concentration, N_B. At the depletion edge, an abrupt transition to the neutral bulk defines a point at which the electric field must go to zero (a useful boundary condition). Space charge neutrality prevails in the bulk region because of a surplus of majority carriers, and the energy bands are flat.

The key features of the depletion approximation are applied to the uniform channel device and shown in Fig. 3.7 (b). The surface depletion region extends to a distance W under the oxide-semiconductor interface. Also, the natural depletion widths on either side of the junction are x_n and x_p, setting the depletion edges at x_j-x_n and x_j+x_p, respectively. The neutral part of the channel, which contains the mobile electrons, is confined between two opposing depletion region edges. In this way, the structure is partitioned into regions with different values for $\rho(x)$ given in Table 3.1. Note from Fig. 3.7, terms N_D and N_A now represent the net doping concentrations in the n-channel and p-bulk,

Table 3.1

Space charge regions of the buried channel MOS structure in the depletion approximation. N_D is the net donor concentration in the n-layer, and N_A is the net acceptor concentration in the p-bulk. An effective fixed oxide charge is included.

1	$\rho = 0$	$-t_{ox} \le x < 0$	oxide
2	$\rho = qN_D$	$0 < x \le W$	surface depletion
3	$\rho = 0$	$W \le x \le (x_j - x_n)$	neutral channel
4	$\rho = qN_D$	$(x_j - x_n) \le x \le x_j$	n-side depletion
5	$\rho = -qN_A$	$x_j \le x \le (x_j - x_p)$	p-side depletion
6	$\rho = 0$	$(x_j + x_p) \le x \le \infty$	neutral p-bulk
$\otimes$	$\rho = Q_f' \delta(x)$	$x = 0$	interfacial charge

respectively. This is a useful distinction because doping values extracted by the differential C-V method always represent net concentrations.

In order to make the ensuing derivation more general, an effective interfacial fixed oxide charge Q_f' (C/cm^2) is included as a sheet charge at the semiconductor-oxide interface. This charge will of course contribute to a net flatband voltage shift, commonly defined in discussions of MOS physics [86]. The effective charge density is comprised of positive fixed charge Q_f and net surface state charge at the flatband condition Q_{IT}^{flatband}, giving

$$Q_f' = Q_f + Q_{IT}^{flatband} \tag{3.4}$$

Now, the 1-D Poisson equation in Eq. (3.3) can be solved within each of the six regions to give an equation (or equations) for $\phi(x)$. This is achieved more easily by intermediately solving for electric field through Gauss' Law

$$\frac{d\mathcal{E}}{dx} = \frac{\rho(x)}{\varepsilon_r \varepsilon_o} \tag{3.5}$$

and applying the appropriate boundary conditions

$$K_{OX}\mathcal{E}(0^-) = K_S\mathcal{E}(0^+) - Q_f' \tag{3.6a}$$

$$K_S\mathcal{E}(x_j^-) = K_S\mathcal{E}(x_j^+) \tag{3.6b}$$

$$\mathcal{E}(W) = \mathcal{E}(x_j - x_n) = \mathcal{E}(x_j + x_p) = 0 \tag{3.6c}$$

K_{OX} and K_S are the relative permittivitties for oxide and semiconductor, respectively, and electric field has units of V/cm. Also, $\mathcal{E}(0^-)$ is referred to as $\mathcal{E}_{OX}$ and $\mathcal{E}(0^+)$ is the surface electric field inside the semiconductor $\mathcal{E}_S$. Equation (3.6a) is important when calculating the proper magnitude of electric field in the oxide for a given gate bias. Condition (3.6b) is valid, assuming 'that no significant amount of defect charge is present at 'the metallurgical junction. Equation (3.6c) comes directly from the depletion approximation. A qualitative graphical integration of the charge distribution in Fig. 3.7 (b) yields the electric field profile shown in Fig 3.7 (c).

Next, the negative gradient of the potential is proportional to the electric field. Written in 1-O, that is

$$-\frac{d\phi}{dx} = \mathcal{E}(x). \tag{3.7}$$

Again using a rough graphical interpretation, Eq. (3.7) yields the profile in Fig. 3.7 (d). Several key potential values are defined in this figure: ϕ_s is the surface potential at $x=0^+$, ϕ_s' is the total band bending within the surface depletion region, and ϕ_{min} is the most positive potential in the n-channel. It may seem counter-intuitive to name the maximum potential in such a way, but this nomenclature facilitates the discussions of CCD operation in later sections because of the potential well analogy. The electrostatic potential must be continuous, giving the following boundary conditions for application to (3.7):

$$\phi(-t_{ox}) = \phi_G \tag{3.8a}$$

$$\phi(0^-) = \phi(0^+) = \phi_s \tag{3.8b}$$

$$\phi(W^-) = \phi(W^+) = \phi_{min} \tag{3.8c}$$

$$\phi\left(\left(x_j - x_n\right)^-\right) = \phi\left(\left(x_j - x_n\right)^+\right) = \phi_{min} \tag{3.8d}$$

$$\phi(x_j^-) = \phi(x_j^+) \tag{3.8e}$$

$$\phi(x_j + x_p) = 0 \tag{3.8f}$$

Assuming there are no distributed charges within the oxide, the electric field is a constant $\mathcal{E}_{OX}$. By integrating ***(3.7)*** from the gate ($x=-t_{ox}$) to an arbitrary point x within the oxide, we have

$$\int_{\phi_G}^{\phi(x)} d\phi' = \int_{-t_{ox}}^{x} [-\mathcal{E}_{OX}]\, d\xi . \tag{3.9}$$

The result is a linearly varying potential within the oxide

$$\phi(-t_{ox} \le x \le 0) = \phi_G - \mathcal{E}_{OX}(x + t_{ox}), \tag{3.10}$$

where ϕ_G is the electrostatic potential in the gate.

The uniform doping assumption gives that the space charge in a depletion region is a constant. Applying this to Gauss' Law in the surface depletion region

$$\int_{0}^{\mathcal{E}(x)} d\mathcal{E}' = \int_{W}^{x} \left(\frac{qN_D}{K_S \varepsilon_o} \right) d\xi \tag{3.11}$$

produces a linearly varying electric field described by

$$\mathcal{E}(0 < x \le W) = \frac{-qN_D}{K_S \varepsilon_o}(W - x). \tag{3.12}$$

Again, the potential variation is found as in ***(3.9)***

$$\int_{\phi_{min}}^{\phi(x)} d\phi' = \int_{W}^{x} \left[\frac{qN_D}{K_S \varepsilon_o}(\xi - W) \right] d\xi , \tag{3.13}$$

giving a quadratic expression in x as

$$\phi(0 < x \le W) = \phi_{min} - \frac{qN_D}{2K_S \varepsilon_o}(W - x)^2 , \tag{3.14}$$

which is a well known result of the depletion approximation and uniform doping. Similarly, $\mathcal{E}(x)$ and $\phi(x)$ are found throughout the remainder of the structure, and the results are summarized:

$$\mathcal{E}(x_j - x_n < x \le x_j) = \frac{qN_D}{K_S\varepsilon_o}\left[x - \left(x_j - x_n\right)\right] \tag{3.15a}$$

$$\phi(x_j - x_n < x \le x_j) = \phi_{min} - \frac{qN_D}{2K_S\varepsilon_o}\left[x - \left(x_j - x_n\right)\right]^2 \tag{3.15b}$$

$$\mathcal{E}(x_j < x \le x_j + x_p) = \frac{qN_A}{K_S\varepsilon_o}\left[\left(x_j + x_p\right) - x\right] \tag{3.16a}$$

$$\phi(x_j < x \le x_j + x_p) = \frac{qN_A}{2K_S\varepsilon_o}\left[\left(x_j + x_p\right) - x\right]^2 \tag{3.16b}$$

From the boundary conditions at x_j, the junction depletion widths are found as

$$x_p = \sqrt{\frac{2K_S\varepsilon_o}{qN_A}\left(\frac{N_D}{N_A + N_D}\right)\phi_{min}} \tag{3.16a}$$

$$x_n = \frac{N_A}{N_D}x_p \tag{3.16b}$$

Finding an expression for W involves the physics of an MOS structure [87], including interfacial charge and metal-semiconductor workfunction differences. Consider the energy band diagram shown in Fig 3.7 (e), which can be inferred from the shape of the potential distribution. The workfunction differences are grossly represented by step offsets in allowable energy levels. Here, χ' (eV) is the conduction band offset between oxide and semiconductor, and Φ'_M (eV) is the offset between metal and oxide. Summing the energies through the whole structure gives a consistent picture of how these surface features are incorporated into the model,

$$-qV_G + \Phi'_M - q\Delta V_{OX} - \chi' - q\phi'_s - \left(E_C - E_F\right) + q\phi_{min} - qV_{bi} = 0 \tag{3.17}$$

where V_{bi} is the built-in potential and ΔV_{OX} is the potential drop across the insulator, and $\left(E_C - E_F\right)$ is taken in the neutral channel. By making use of Eqs. (3.6a), (3.10), (3.12) and (3.14) and defining the metal-semiconductor workfunction difference as

$$\phi_{MS} = \frac{1}{q}\left\{\Phi'_M - \left[\chi' + \left(E_c - E_F\right)\right]\right\}, \tag{3.18}$$

Eq. (3.17) is rewritten to include all factors of W,

$$V_G - \left\{ \phi_{MS} - \frac{qQ_f'}{C_{ox}} \right\} + t_{ox}' \frac{qN_D}{K_S \varepsilon_o} W + \frac{qN_D}{2K_S \varepsilon_o} W^2 - \phi_{min} + V_{bi} = 0 \qquad (3.19)$$

where $t_{ox}' = (K_S / K_{OX}) t_{ox}$, and ϕ_{MS} is specified in volts. Finally, the sought expression for surface depletion width is extracted from (3.19) as

$$W = \sqrt{(t_{ox}')^2 + \frac{2K_S \varepsilon_o}{qN_D} \left[\phi_{min} - V_{bi} - (V_G - V_{FB}) \right]} - t_{ox}'. \qquad (3.20)$$

The two MOS non-idealities in the braces in (3.19) are written into a single term V_{FB}, which is the flatband voltage of the n-type MOS structure with respect to the electron quasi-Fermi level in the channel F_N. However, V_{FB} is not the flatband voltage for the entire buried-channel structure in Fig. 3.7. To achieve flatbands at the n-type surface (i.e., W=0) when the p-type substrate is the reference, the applied gate voltage must be equal to $V_{FB}+(\phi_{min}-V_{bi})$, which can be written as an equivalent flatband voltage for the buried-channel structure,

$$V_{FB}^{bc} = V_{FB} + V_{ch}. \qquad (3.21)$$

Referring to the band diagram in Fig. 3.7 (e), the channel voltage V_{ch} is defined as the reverse bias on the PN junction corresponding to a ϕ_{min} greater than V_{bi}. The relationship in (3.21) is experimentally observed with the C-V measurement of the BGCD [54], [84] because the channel voltage can be arbitrarily set via the ohmic contact at the drain.

At this point, it is easy to find an expression for the resultant electrostatic potential at the gate, ϕ_G. Summing potentials in Fig. 3.7 (d) gives the relation,

$$\phi_G + \Delta V_{OX} + \phi_s' - \phi_{min} = 0 \qquad (3.22)$$

which is similar in form to Eq. (3.17). By substituting (3.20) into the expressions for ΔV_{OX} and ϕ_s' and simplifying, ϕ_G can be shown to be

$$\phi_G = V_G - \phi_{MS} + V_{bi}. \qquad (3.23)$$

This result can be justified by realizing a simple fact from solid-state theory [2]: the total change in electrostatic potential across the device is equivalent to the

electrochemical potential difference (V_G) minus the net change in chemical potential. Contact potentials (ϕ_{MS} and V_{bi}) are due to differing chemical potentials between materials. The term ϕ_G has been widely misinterpreted as $V_G - V_{FB}$ [55], [88].

The previous exercise of deriving Eqs. (3.10), (3.12), (3.14)-(3.16), and (3.20) is instrumental in visualizing how the field and potential profiles in Fig. 3.7 arise, but an example profile from a real device cannot be calculated unless both a gate voltage and channel potential are known. This is practical when modeling the buried channel MOSFET, as stated before, because the channel potential is fixed. On the other hand, the channel under any given phase along the CCD (except possibly near the input or output) is truly floating, and ϕ_{min} cannot be directly controlled. However, it can be manipulated by the gate voltage through the field effect. So, a relationship between ϕ_{min} and V_G is required to complete the above set of equations.

A typical approach is to assume the channel to be fully depleted [66], [89] by writing $W + x_n = x_j$ and algebraically solving for ϕ_{min} as a function of V_G. Given that, one can calculate an expected V_G vs. ϕ_{min} curve for a channel without any charge, as was done for the SiC BGCD in Section 2.2.2.1.

Unfortunately, this method lacks generality [78] because of the fully depleted channel assumption. It will be shown in a later section that channel potential is also a strong function of the charge, so a relationship amongst the triplet $\{Q_n, \phi_{min}, V_G\}$ is more useful for determining clocking voltages and modeling charge transfer. Although the nature of charge storage is different for the surface channel device, a similar three-way relationship is used for describing the SCCD [52]: given two of the three variables in the set, it is always possible to determine a value for the third.

Fortunately, only a slight modification is needed to find the expanded relationship. When a portion of the channel is undepleted (i.e., charge is present), the arbitrary charge is included by writing

$$x_j' = x_j + \frac{Q_n}{qN_D} = W + x_n. \tag{3.24}$$

where Q_n (C/cm^2) is defined as negative. By substituting the newfound expressions for W and x_n from Eqs. (3.16) and (3.20), one can find the expression for channel potential that depends on V_G and Q_n

$$\phi_{min} = \left(1 + \frac{N_A}{N_D}\right)\left[\begin{array}{l}(V_G - V_{FB}) + V_{bi} + V_1 + V_2 \\ -\sqrt{(V_2)^2 + 2V_2\left[(V_G - V_{FB}) + V_{bi} + V_1\right]}\end{array}\right] \tag{3.25}$$

where the terms V_1 and V_2 are defined as

$$V_1 = \frac{qN_D}{2K_s\varepsilon_o}\left(1 + 2\frac{t'_{ox}}{x'_j}\right)\left(x'_j\right)^2 \tag{3.26a}$$

$$V_2 = \frac{qN_A}{K_s\varepsilon_o}\left(1 + \frac{t'_{ox}}{x'_j}\right)^2\left(x'_j\right)^2 \tag{3.26a}$$

to make the notation more concise. The influence of the charge comes through the x'_j terms in Eqs, (3.26). In the analysis of a particular device, it is also useful to have the "reciprocal" versions of (3.25), which are repeated here for convenience. For instance, the gate voltage needed to hold a particular charge packet size at a given channel potential is calculated via

$$V_G = V_{FB} - V_{bi} - V_1 + \left(\frac{N_D}{N_A + N_D}\right)\phi_{min} + \sqrt{2V_2\left(\frac{N_D}{N_A + N_D}\right)\phi_{min}}\,. \tag{3.27}$$

Alternately, the amount of the charge at a certain gate bias and a known channel potential can be found with the relation

$$Q_n = -qN_D\left(\begin{array}{l}x_j - \sqrt{\frac{2K_S\varepsilon_o}{qN_D}\left(\frac{N_A}{N_A + N_D}\right)\phi_{\min}} + t'_{ox} \\ -\sqrt{(t'_{ox})^2 + \frac{2K_S\varepsilon_o}{qN_D}\left[\phi_{\min} - V_{bi} - (V_G - V_{FB})\right]}\end{array}\right). \tag{3.28}$$

Finally, a complete set of equations is available to find the 1-D field and potential profiles quantitatively for the uniformly doped device as in Fig. 3.7. Figure 3.8 shows a sample calculation of the potential profiles of a silicon carbide buried n-channel device with physical parameters: N_D=6x10^{16} cm^{-3}, N_A=1x10^{16} cm^{-3}, t_{ox}=1000 Å, x_j=5000 Å, V_{FB}=0 V. In this example, the gate voltage is held at a constant 5 V, while different values of charge are present in the channel. Many features of device operation can be obtained from this

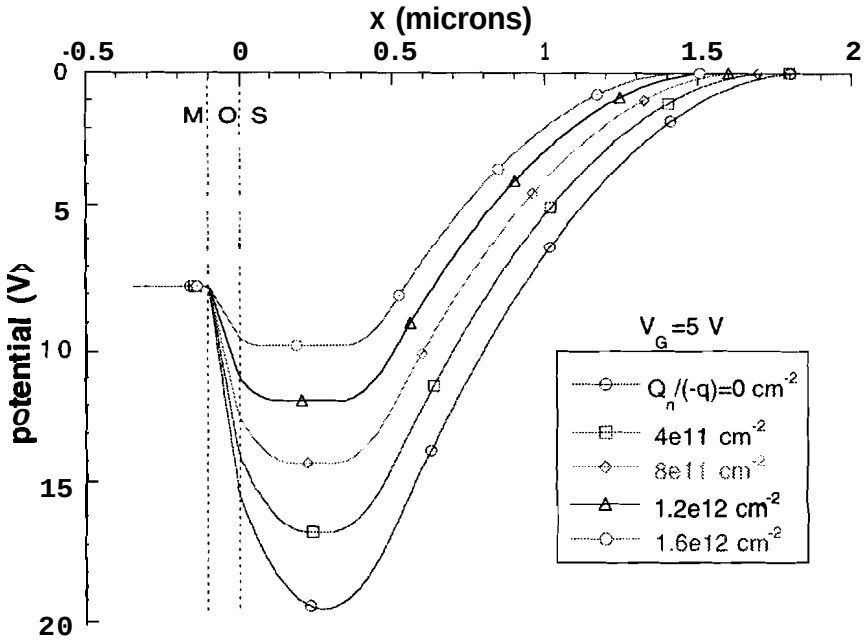


Figure 3.8

Sample calculation of the potential variation under the gate of a buried channel structure with a constant gate voltage V_G =5 V and varying well charge. Device parameters are: N_D=1.6x10^{16} cm^{-3}, N_A=1x10^{16} cm^{-3}, t_{ox} =1000 Å, and x_j =5000 Å. Other parameters assumed are: T=296 K, n_i =1.66x10^{-6} cm^{-3}, V_{FB} =0 V. The varying amount of charge demonstrates how strongly ϕ_{min} can change.

simple curve family. One can see that addition of negative electronic charge uncler a CCD phase reduces the positive potential in the channel. Plotting the profiles with positive potential downwards lends to the analogy of a well being "filled" with electrons.

Also, the charge packet tends to spread towards the interface as the number of electrons increases. This is in contrast to the SCCD, where the charge resides in a thin layer at the interface. If charge continue!; to dump into the well (from an adjacent well or via electron-hole pair generation), then the surface depletion region goes to zero and charges are no longer confined from the surface. This "saturation of charge" is undesirable, of course, because of the potentially destructive interaction with surface states and reduced mobility of carriers near the interface [53]. Hence, the concept of a maximum charge packet size $Q_{n,max}$ (C/cm^2) must be included when designing device

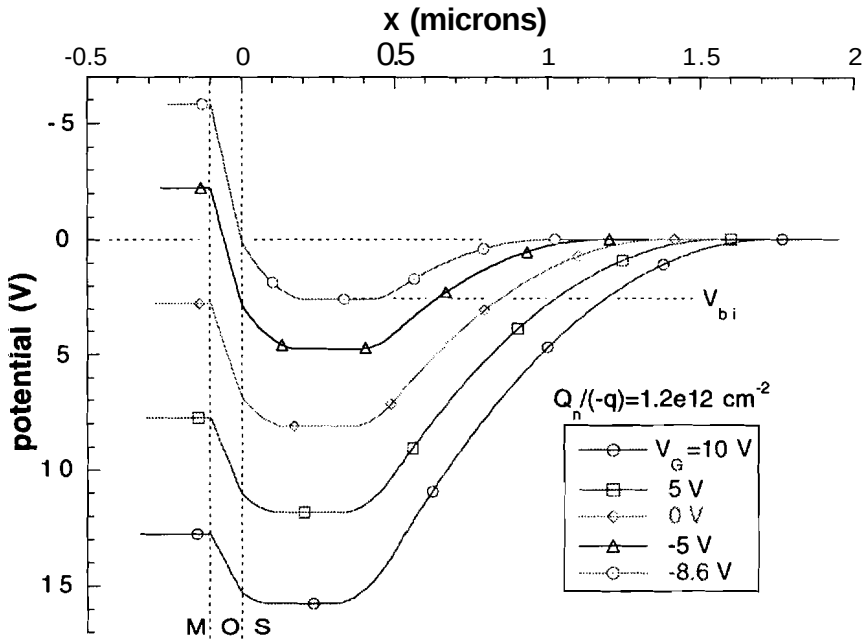


Figure 3.9

Sample calculation of the potential variation under the gate of a buried channel structure with a constant charge $Q_n/(-q)=1.2\text{x}10^{12}$ cm^{-2} and varying gate voltage. Device parameters are: $N_D=1.6\text{x}10^{16}$ cm^{-3}, $N_A=1\text{x}10^{16}$ cm^{-3}, $t_{ox}=1000$ Å, and $x_j=5000$ Å. Other parameters assumed are: T=296 K, $n_i=1.66\text{x}10^{-6}$ cm^{-3}, $V_{FB}=0$ V. The different gate biases change the channel potential accordingly, but also change the position of the charge packet in the well.

parameters. In addition, the maximum allowable charge is gate voltage dependent. This fact is not evident from the curves in Fig. 3.8, but will be discussed in more detail in Section 3.2 during a discussion of other design constraints.

Additional insight on device behavior can be derived from the plots of Fig. 3.9. For the same device as in Fig. 3.8, curves are shown for a constant charge of $Q_n/(-q)=1.2\text{x}10^{12}$ cm^{-2} and five different values of gate bias: -8.6, -5, 0, 5, and 10 V. The channel potential minimum is manipulated by the gate bias according to Eq. (3.25), and the constant charge density (Q_n) is reflected by the constant width of the neutral, "flat" region on each curve. Note also, that a change in gate voltage alters the position of the charge packet in the channel, such that the surface depletion width is reduced for higher gate bias. For this

reason a maximum gate voltage $V_{G,max}$ must also be adopted to avoid operating a particular device in a surface channel mode. An exact definition of the maximum gate voltage will be defined in a later section, but a crude expression can be taken directly from Eq. (3.20). For a particular channel potential, the gate bias must not reach the equivalent flatband voltage V_{FB}^{bc} defined in (3.21).

At the other extreme of V_G, applying a more negative gate bias will eventually reduce V_{ch} to zero. This point constitutes another bias limit on the device because any further negative gate voltage will tend to "forward bias" the junction, resulting in loss of charge to the substrate. In this example, the gate voltage -8.6 V was calculated by using $Q_n/(-q)=1.2\text{x}10^{12}$ cm^{-2} and $\phi_{min}=V_{bi}$ in Eq. (3.27).

3.2 Desian Considerations

The basic description of CCDs and detailed derivations of buried channel MOS equations in the previous section yield a starting point for designing a real device. In this section, specific limitations on device operation are presented, including maximum charge capacity, maximum gate voltage, oxide breakdown strength, and surface inversion. All of these must be considered to fully understand the operation of a CCD and to choose the physical parameters, layout scheme, and operating voltages.

3.2.1 Charge Capacity

The charge capacity of an n-channel BCCD is basically lirnited by the maximum achievable width of the neutral bulk. Using this broad definition, the maximum charge $Q_{n,MAX}$ is proportional to the junction depth minus an equilibrium (zero bias) depletion width, x_{no}. This is obviously not a useful definition for the CCD application because of the interaction of the charge packet with the surface. In order to take full advantage of bulk mobility and minimize the surface state interaction, the charge packet must be confined from the surface.

For this purpose, the surface band bending ϕ'_s can be visualized as a barrier that prevents signal charge from reaching the surface, which should always be larger than a certain critical value, $\phi'_{s,min}$. In the literature, an arbitrary value of $10kT/q$ has been widely used for design purposes [66], [90]. This constraint alters the above definition of $Q_{n,max}$ to be

$$Q_{n,max} = -qN_D\left(x_j - x_n - W_{min}\right), \tag{3.29}$$

where W_{min} is the surface depletion width corresponding to the minimum allowed surface barrier. We differentiate between $Q_{n,MAX}$ and $Q_{n,max}$ because the former is the peak value of the latter. Notice that the equilibrium n-side depletion is not stipulated in Eq. (3.29), meaning that $Q_{n,max}$ is gate voltage dependent. For a given gate voltage, the channel potential under the maximum charge condition is most easily calculated with a rearrangement of Eq. (3.19)

$$\phi_{min} = V_G - V_{FB} + V_{bi} + t'_{ox}\frac{qN_D}{K_S\varepsilon_o}W_{min} + \phi'_{s,min}. \tag{3.30}$$

Again, the vertical potential profile is used in visualizing the three way relationship, $\{Q_n, \phi_{min}, V_G\}$. For the example device of the previous section, six profiles are plotted in Fig. 3.10, using gate voltages -10, -5, 0, 5, 10 and 15 V. For each of the four lower curves, the channel potential is calculated by (3.30). Subsequently, the maximum charge (allowed by the $\phi'_{s,min}$ constraint) is found via Eqs. (3.16) and (3.29). Qualitatively, we can see that the n-side depletion region increases with V_G, and the surface depletion is constant, so that $Q_{n,max}$ must decrease.

The two uppermost curves in Fig. 3.10 (-5 and -10 V) correspond to the negative bias range where charge capacity is limited by injection to the substrate. Here, we make the assumption that the NP junction cannot be forward biased too strongly, so that ϕ_{min} remains in line with the built-in potential for decreasing gate biases. The n-side depletion is constant at the equilibrium value, while W must increase to compensate for the gate charge, resulting in a narrower neutral channel.

Taking into account, then, the rules of charge confinement and charge loss to the substrate, the locus of the charge capacity is calculated and depicted in Fig. 3.11 for three different values of the surface barrier. The two regimes are

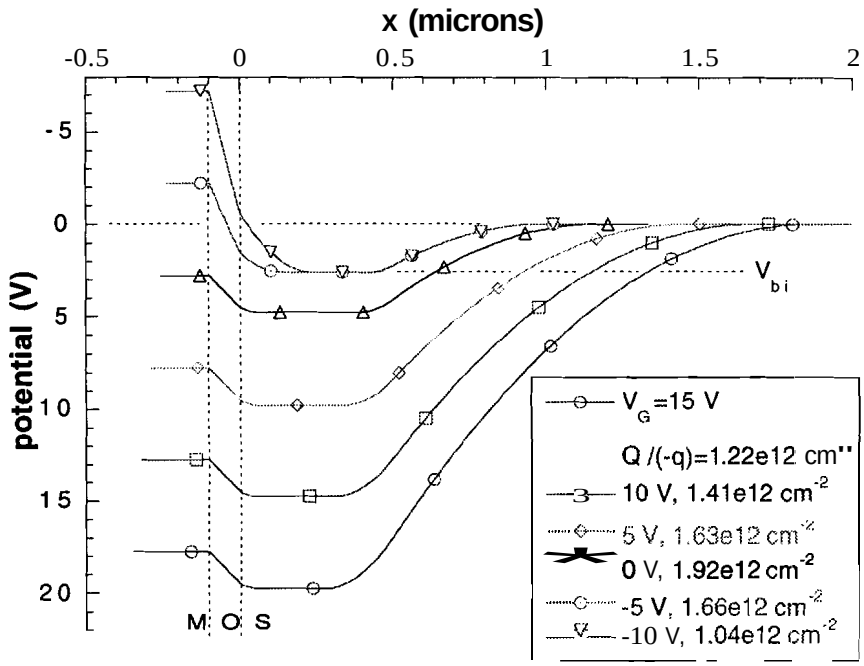


Figure 3.10

Sample calculation of the potential variation under the gate of a buried channel structure at the saturation charge. Device parameters are: N_D =1.6x10^{16} cm^{-3}, N_A =1x10^{16} cm^{-3}, t_{ox} =1000 Å, and x_j =5000 Å. Other parameters assumed are: T=296 K, n_i =1.66x10^{-6} cm^{-3}, V_{FB} =0 V. The channel is in communication with the substrate for the two upper curves. For the four lower curves, the charge is confined from the interface by the minimum allowed surface barrier, $\phi'_{s,min}$=10kT/q.

clearly evident on either side of the peak value $Q_{n,MAX}$, which is at the bias point with the minimum allowed values of the opposing depletion regions, W_{min} and x_{no}. Each curve is unique for a particular set of parameters (N_A, N_D, t_{ox}, x_j, etc.) and height of $\phi'_{s,min}$.

$Q_{n,MAX}$ represents the maximum charge capacity of the buried channel, when special attention is paid to confine charge from the surface. During CCD operation, however, the size of the charge packet is actually determined by the lateral confinement of the adjacent phases as shown in Fig. 3.2 (b).

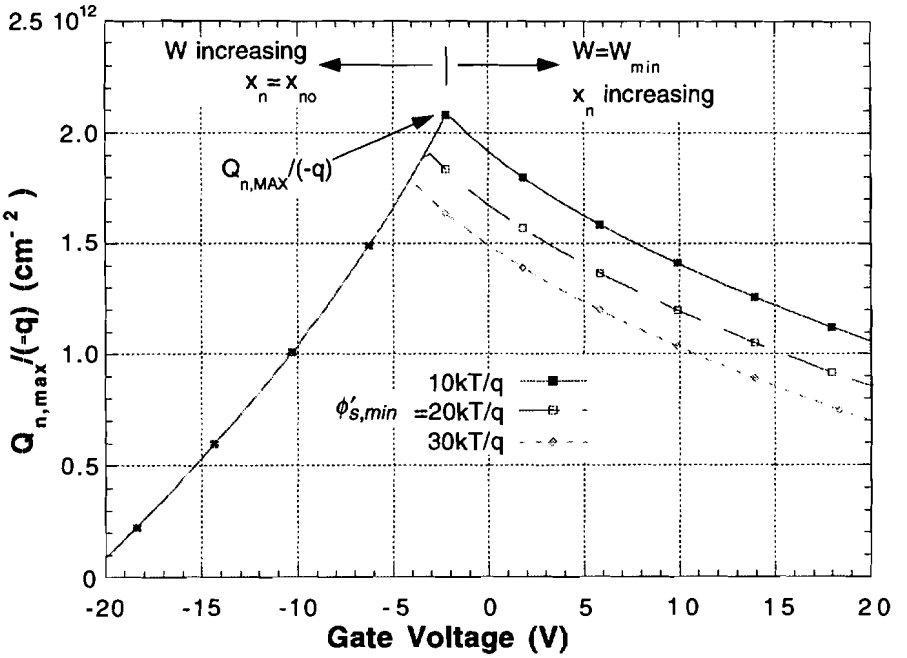


Figure 3.11

Variation of the saturation charge with respect to gate voltage for three values of the surface barrier. The peak of each curve designates the charge capacity of the well $Q_{n,MAX}$.

3.2.2 Maximum Gate Voltage

Just as the surface barrier requirement limits the charge (i.e., width of the neutral region) at a specific gate bias, it is useful to realize the inverse relationship when choosing clocking potentials. If a certain amount of charge is to be contained in the channel without saturation, the maximum gate voltage can be inferred from a plot similar to Fig. 3.11. Choosing an example of for $\phi'_{s,min}$=10kT/q and $Q_n/(-q)$=1.5x10^{12} cm^{-2}, the gate voltage should not exceed $V_{G,MAX}$=8 V.

3.2.3 Avoiding Weak Surface Inversion

In general, a lower limit on gate bias should be set in order to prevent surface inversion. From the analysis of a simple p-channel MOS capacitor, *strong inversion* is prevented at the surface as long as the intrinsic energy level remains below the hole quasi-Fermi energy plus the background doping parameter ϕ_{fn}, or $E_{i,s} < F_{P,s} + \phi_{fn}$. This criterion is used when designing BCMOSFETs to ensure that the device can be turned off before inverting the surface [55]. A more stringent rule of preventing weak *inversion* rnust be applied to the SiC device because of the influence of surface states on stable operation.

In a generic MOS device at any temperature, surface states above the Fermi energy can be filled with electrons for a limited time period if (a) their energy separation from the conduction band precludes thermal emission during the time period, or (b) no holes are present at the surface with which the electrons can recombine. This fact is commonly overlooked in the literature when analyzing room-temperature CV curves on SiC MOS devices, due to the wide bandgap and long emission times [49], [91]. Deep level trapping was demonstrated with the operation of the buried-channel gated diode that was presented in Chapter 2 (see Fig. 2.8). While sweeping the gate lbias negatively frorn accumulation, deep level surface states pushed above the Fermi level did not change charge state until the arrival of holes at the surface at a very strong negative bias. The large flatband shift due to the charge in the surface states prevents a precise control of the channel potential, which is absolutely necessary for CCD operation.

The strategy, then, is to prevent a significant number of holes from reaching the surface at all. Referring to the band diagram in Fig. 3.7 (e), the new condition requires that $E_{i,s}$ must remain below the hole quasi-Fermi energy. Assuming that the surface hole concentration is in equilibrium with the p-bulk due to the lateral connection, we can write that $F_{P,s} = E_{F,bulk}$. Consequently, the weak inversion constraint becomes $E_{i,s} < E_{F,bulk}$. Relating this rule to the familiar definitions of the previous section, we fincl

$$\phi_s > \phi_{fp} \; ; \; \phi_{fp} = kT/q \, ln(N_A / n_i), \tag{3.31}$$

where ϕ_{fp} is the bulk doping parameter. By algebraic manipulation of Eqs. (3.19) and (3.20), the general expression for the surface potential (as defined in Fig. 3.8 (d)) is

$$\phi_s = V_{bi} - (V_G - V_{FB}) - V_o + \sqrt{V_o^2 + 2V_o\left[\phi_{min} - V_{bi} - (V_G - V_{FB})\right]} \qquad (3.32)$$

with the conventional abbreviation, $V_o = K_S \varepsilon_o q N_D / C_{ox}^2$. Utilizing the criterion in Eq. (3.31) with (3.32), one finds that the "threshold voltage" for weak inversion depends on ϕ_{min} as

$$V_{Ti} = V_{FB} + \phi_{fp} - V_{bi} - \sqrt{2V_o\left(\phi_{min} - \phi_{fp}\right)}. \qquad (3.33)$$

The next section describes how to utilize Eq. (3.33) when choosing the operating points of the CCD.

3.2.4 CCD Operating Domain

It is very difficult to assess the proper operation of a BCCD without constructing a family of curves that incorporates the constraints in Sections 3.2.1-3.2.3 into the general models of Section 3.1. These factors and other subtle points are culminated in the operating domain plot in Fig. 3.12 for the sample device of previous sections (T=296 K, N_D =6x10^{16} cm^{-3}, N_A=1x10^{16} cm^{-3}, t_{ox} =1000 Å, x_j =5000 Å, V_{FB}=0 V). The thin solid lines represent loci of constant charge for the $\{Q_n, \phi_{min}, V_G\}$ relationships in Eqs. (3.24)-(3.28). The gray shaded areas of the plot represent regions in which the device will either (a) dump signal charge to the substrate, (b) violate the condition of weak inversion in Eq. (3.31), or (c) operate near the surface channel mode by reducing the surface barrier below the specified $\phi'_{s,min}$. For the given set of parameters, the entire region above the $Q_n/(-q)$=0 locus is not physically attainable', so it is also shaded as a forbidden zone. The remaining clear region defines the safe operation domain for the device.

The thick solid black line is defined by the special relationship in Eq. (3.30), where the surface band bending is at its minimum allowed value. The boundary specifies both $Q_{n,max}$ and $V_{G,max}$. Each locus of constant charge

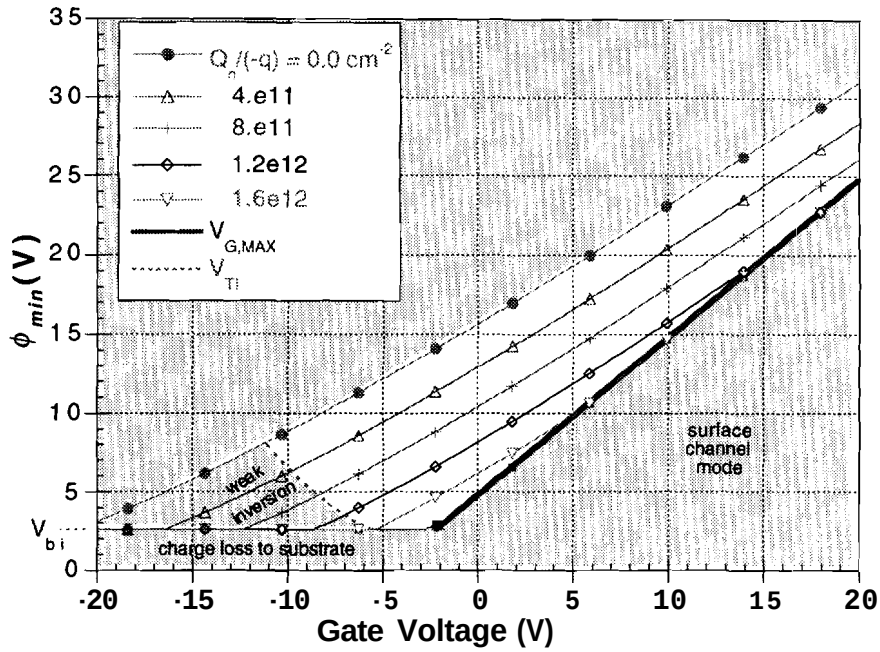


Figure 3.12

Operating domain plot for the sample device: N_D=1.6x10^{16} cm^{-3}, N_A =1x10^{16} cm^{-3}, t_{ox} =1000 Å, x_j=5000 Å, T=296 K, n_i=1.66x10^{-6} cm^{-3}, V_{FB}=0 V. Clocking voltages and charge input should be controlled to limit the device to the clear zone of the plot. Otherwise, there is a possibility of weak inversion at the surface, charge injection to the substrate, or interaction with the surface.

terminates at a point on this line, which designates $V_{G,max}$. Conversely, when the gate is held at a certain bias, the addition of charge should be limited so as to keep ϕ_{min} more positive than the same line. At the gate voltage where this $V_{G,max}$ line meets the constant V_{bi} line, both the surface depletion width and the n-side depletion width are at their minimum values, meaning; this point is coincident with the maximum charge capacity, $Q_{n,MAX}$ (cf. Fig. 3.11).

In order to prevent the possibility of holes at the n-type surface, the CCD must be kept out of the region labeled as weak inversion. The dashed line that demarcates the boundary to this region is the threshold voltage V_{Ti} defined in Eq. (3.33). The value of V_{Ti} calculated for $\phi_{min}=V_{bi}$, specifying the term V_{TI}, is the most negative clock voltage that should be used, unless a lower charge capacity is acceptable.

Fortunately, it is possible to design the BC device so that the operating domain intersects little or none of the weak inversion regime. In most cases, this can be achieved by a reduction in the junction depth, but not without sacrificing some of the charge capacity. Design curves presented in the next section aid in device design by showing how V_P, V_{TI}, and $Q_{n,MAX}$ vary with physical attributes such as t_{ox}, x_j, N_D, and N_A.

3.2.5 Design Curves for the Practical SiC BCCD

Design of a buried channel device can be expedited for typical background dopings by examining design curves given in this section. Recall that all of the equations in this chapter have been derived assuming a CCD configuration, meaning the substrate is the reference terminal. The following discussion may not apply to design of the BCMOSFET, where the source is typically the reference.

3.2.5.1 Electric field limitations

The maximum electric field of the buried-channel MOS structure is present at the semiconductor-oxide surface when a large negative gate bias is used to completely deplete the channel. Considering the relationship between $\mathcal{E}_{OX}$ and $\mathcal{E}_S$ in Eq. (3.6), the field in the oxide will always have a larger magnitude because of the ratio K_S/K_{OX}. The presence of interface fixed charge just serves to make $\mathcal{E}_{OX}$ more negative. Therefore, the concern arises whether a certain buried-channel design will have electric fields in the oxide that are larger than the critical breakdown field of SiO_2. In order to demonstrate that the oxide field is not an important design issue, oxide electric field at pinchoff is plotted in Fig. 3.13 for practical values of junction depth and channel doping in the SiC BCCD process. A typical oxide thickness of 700 Å, p-layer doping of 1×10^{16} cm^{-3}, T=296 K, and V_{FB}=0 V are assumed. The result shows that electric field is well below the breakdown field of oxide (5-10 MV/cm) and is not a limitation for device design.

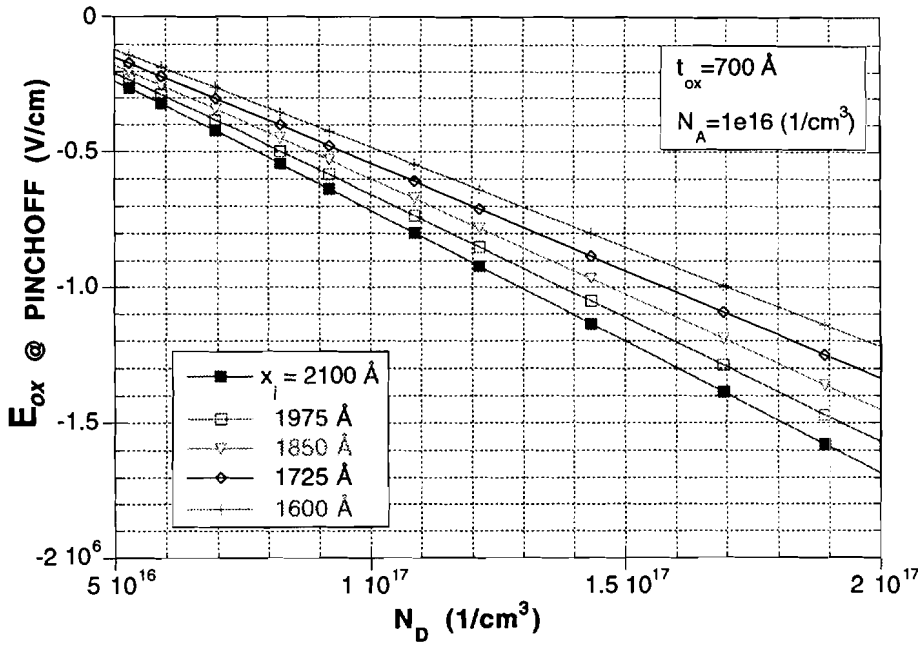


Figure 3.13

Variation of the maximum electric field in the oxide for practical values of junction depth and channel doping in the SiC BCCD process. A typical oxide thickness, p-layer doping, T=296 K, and V_{FB}=0 V are assumed. The result shows that electric field is well below the breakdown field of oxide and is not a limitation for device design.

3.2.5.2 Maximum charge capacity

It is important to make sure that a certain design has the dlesired charge capacity, in order to be able to detect charge packets. Maximum charge capacity as defined in Section 3.2.1 is plotted in Fig. 3.14 over the same "parameter space" as Fig. 3.13. There is, of course, a trade-off between designing a less negative pinchoff and having sufficient Q_n. Fig. 3.14 can be used in conjunction with Fig. 3.15 (next section) to keep everything under consideration when setting-up the device.

3.2.5.3 Pinchoff-voltage

A device designer may want to choose the parameters of his BCCD according to an operating voltage constraint imposed by the system design. In this case, the two plots in Fig. 3.15 are useful. Values of pinchoff voltage are calculated from Eq. (3.27), using $Q_n=0$ and $\phi_{min}=V_{bi}$, and plotted for practical values of junction depth and channel doping in the implanted channel process. For reference, the threshold voltage for weak inversion V_{TI} is plotted as a dashed line, showing that thinner or lower-doped n-channels have better chance to pinchoff before inversion.

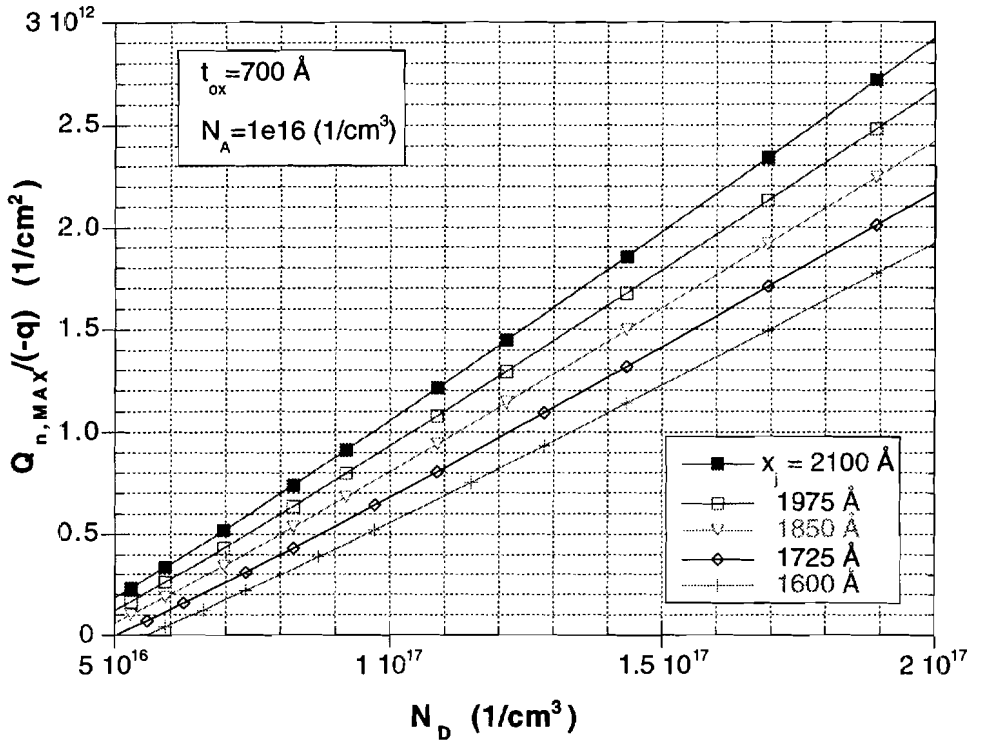


Figure 3.14

Variation of the charge capacity for practical values of junction depth and channel doping in the SiC BCCD process. A typical oxide thickness, p-layer doping, T=296 K, and $V_{FB}=0$ V are assumed. This plot must be used in conjunction with Fig. 3.15 to analyze the tradeoff between a less negative V_{PO} and sufficient Q_n.

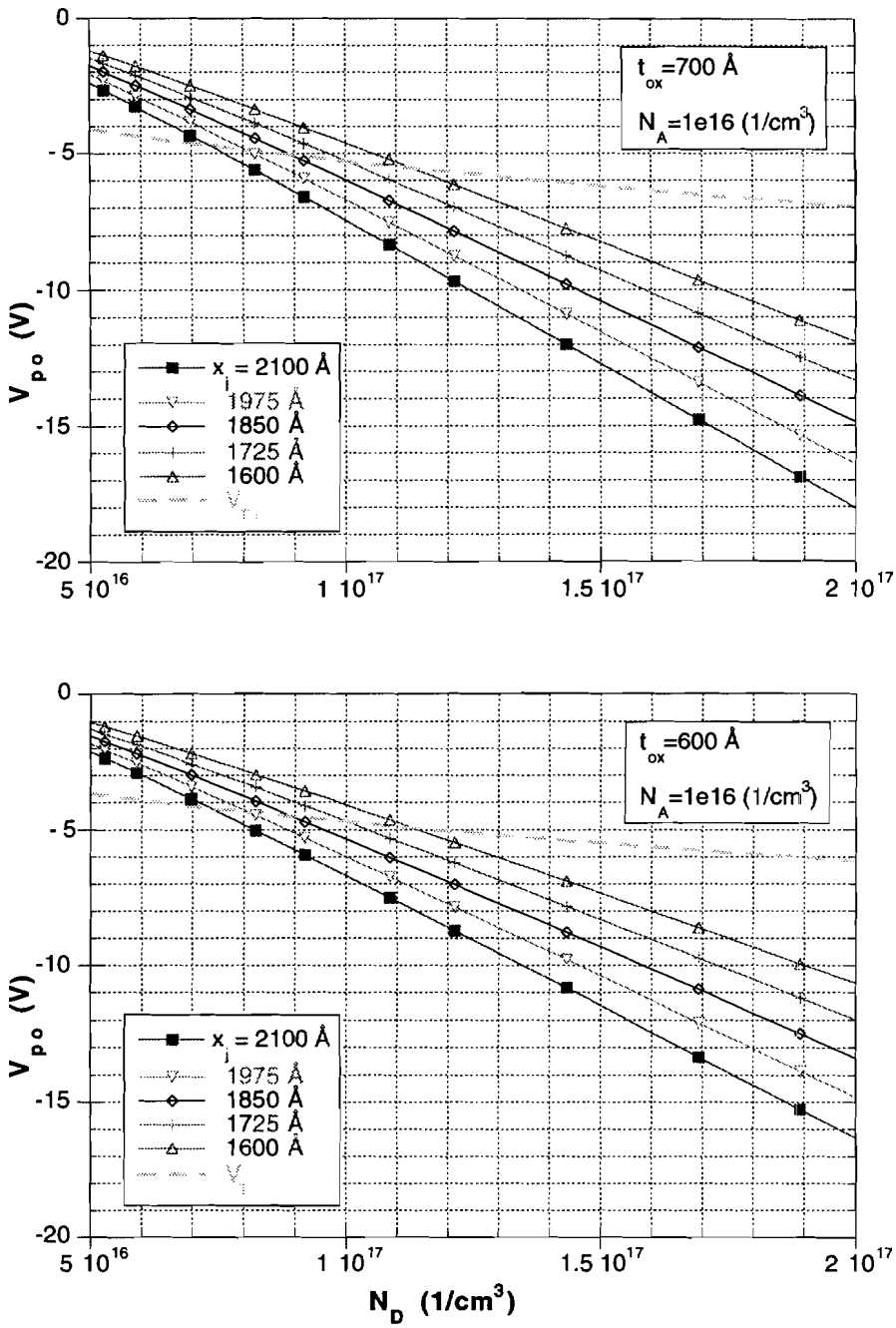


Figure 3.15

Variation of the channel pinchoff voltage for practical values of junction depth and channel doping in the SiC BCCD process. Typical oxide thicknesses, p-layer doping, T=296 K, and V_{FB}=0 V are assumed.

CHAPTER 4 - CCD FABRICATION AND CHARACTERIZATION

Considering the preliminary results of the implanted channel MOS devices presented in Chapter 2, the fabrication and characterization of a linear CCD was pursued. The device was based on a general textbook: example of a four phase overlapping-gate CCD with electrical input and outpul:. Simpler, more fundamental charge transfer devices were also investigated to demonstrate the behavior of stored charge in a buried channel. Section 4.1 discusses the general fabrication process for the two CCD test chips that were fabricated. The test device structures and their operation are outlined in Section 4.2. Electrical measurements for non- charge transfer devices are reported in Section 4.3, and the results are used to calculate the operating domains for the CTDs. Next, Section 4.4 explains the electrical rneasurement of the CTD and the verification of charge transfer in the buried channel. Section 4.5 describes the demonstration of the first SiC CCD shift register.

4.1 SiC CCD Fabrication

The many similarities that can be drawn between the SiC-MOS system and the early developments in the Si-MOS system have given impetus for the recent device research effort to duplicate MOS devices in SiC. Fortunately, the experience of more than twenty years of CCD development can be exploited to demonstrate the charge-coupled concept in SiC. In comparison,,however, the MOS technology in Si was already quite mature during the first years of CCD development [92], whereas many fabrication problems in SiC are still being solved. The SiC CCD fabrication process reported below represents the culmination of several iterations that aspired towards the best features of the silicon process. An excellent summary of the various CCD technologies from a historical basis has been given in Ref. [92] and will not be repeated here.

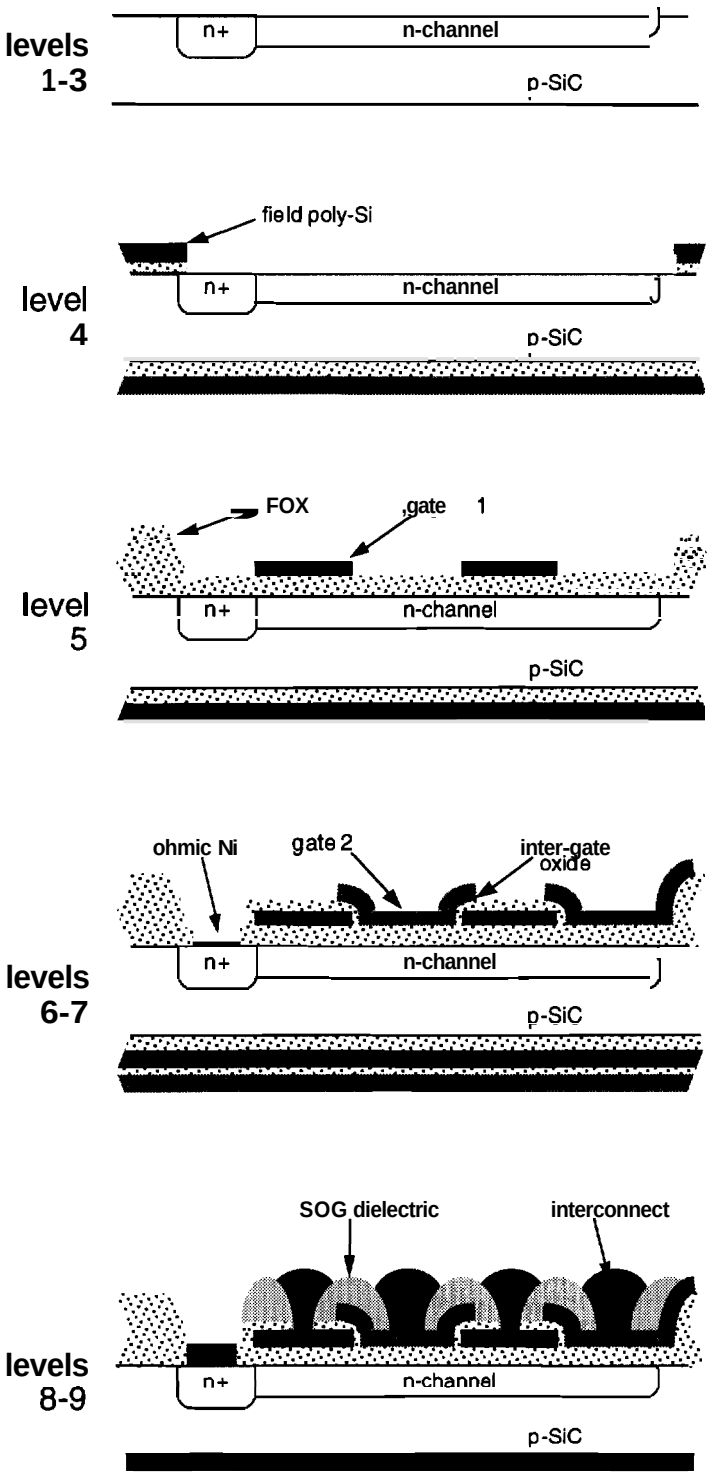


Figure 4.1

Schematic outline of the BCCD process flow, including the conversion of poly-Si to FOX and the overlapping-gate, dual level poly-Si steps. Note that the gate oxides exposed during the patterning of gate 1 are not thinned appreciably.

4.1.1 Process Flow

The general process sequence for the SiC CCD is outlined at the mask level in Table 4.1. The first three steps were taken from the first BCMOSFET run reported in Chapter 2. Additional steps were added for the two level overlapping gate process [93], and an interconnect level was facilitated with a spin on dielectric layer. A thick field oxide was achieved by depositing polysilicon and patterning active area regions with dry etching. Subsequent gate oxidation was sufficiently long to convert the entire thickness of polysilicon to SiO_2. A similar method has been reported previously as Local Oxidation of Polysilicon on Silicon (LOPOS) for device isolation [108].

Like any MOS process in Si, special care was taken at every step to avoid contamination of samples or equipment; especially prior to high temperature processing. Processing tweezers and sample containers were cleaned frequently between steps. Equipment, glassware, and tweezers were only handled while wearing latex gloves.

The nine mask process is described pictorially in Fig. 4.1 with the cross section of a fictitious overlapping-gate device. A run-sheet in Appendix I of this thesis gives meticulous details of the CCD fabrication. The process started with an appropriately doped p-epilayer of 6H-SiC grown 3-5 microns thick onto a highly doped p-substrate. Registration alignment marks (not shown) were etched into the surface with reactive ion etching in SF_6 at 100 mtorr and 100 W. Selective implantations of nitrogen through thick metal masks were performed

Table 4.1

Outline of the BCCD fabrication process at the mask level. All mask polarities are listed for use of positive photoresist.

	Fabrication Step	Mask Polarity	Process
1	Registration Etch	darkfield	Al Wet Etch and SiC RIE
2	S/D Implant Mask	lightfield	Ti/Au Liftoff
3	Channel Implant Mask	lightfield	Ti/Au Liftoff
4	GOX Area definition	darkfield	Poly-silicon Dry Etch
5	Gate Level 1 definition	lightfield	Poly-silicon Wet or Dry Etch
6	Gate Level 2 definition	lightfield	Poly-silicon Wet or Dry Etch
7	S/D Contact Window	darkfield	SiO_2 Wet Etch and Ni Liftoff
8	Dielectric, Via	darkfield	SiO_2 Wet Etch and Al Liftoff
9	Top Level Interconnect	lightfield	Al Etch

in two successive lithography steps to form n^+ and n-channel regions [84]. Desired implant profiles were calculated using empirical data reported by Ahmed et al. [94]. The nitrogen atoms were activated in argon at 1500 °C for 12 minutes.

Next, a thin oxide was grown as a base layer for 2000 Å of undoped polysilicon. The polysilicon was patterned with dry etching, and the underlying base oxide was etched away. A gate oxide of optimum quality was grown using careful cleaning procedures and special loading techniques [13]. Then, samples were loaded immediately into an LPCVD furnace to avoid atmospheric contamination, and 4000-5000 Å of polysilicon gate material was deposited at 620 °C and 150 mtorr. Doping of polysilicon was achieved with an arsenic doped spin-on insulator and a subsequent high temperature drive-in. To complete level 5, gate 1 was patterned with either wet chemical (etchant given in App. I) or dry reactive ion etching in SF_6. The etches were carefully calibrated to remove very little of the underlying gate oxide.

Narrow inter-electrode gaps are required for efficient charge transfer between CCD phases because inter-electrode channel potentials cannot be controlled for spacings greater than about 3 microns [66], especially if large amounts of spurious charge exist in the oxide. For this reason, the overlapping gate process was adapted. Polysilicon gate 1 was encapsulated by 0.1-0.2 microns of thermally grown oxide. Subsequently, metal or a 2nd polysilicon layer was deposited and etched (mask 6) to overlap the 1st gate level, thus forming the 2nd level gate. In this manner, the inter-electrode spacing is fixed by the thickness of the inter-gate oxide.

In a single mask step at level 7, windows were etched into the oxide, and nickel ohmic contacts were defined by liftoff. The Ni was deposited to 500 Å by e-beam evaporation. All of the critical gate regions were covered by a thick layer of photoresist during evaporation.

At this point, the multiple layers of oxide and polysilicon on the wafer backside were stripped by first protecting the frontside with photoresist and wet etching. Then, 1000 Å of platinum was sputter deposited for a backside contact. Pt was chosen due to its high workfunction. The samples were then electrically characterized to determine if the contacts were satisfactorily ohmic. Typically, the Ni contacts to implanted n^+ have been ohmic as deposited. However, even large area backside contacts have shown Schottky-like behavior, which can

impede proper interpretation of high frequency CV characteristics'. If this was the case, then the contacts were annealed at 900 °C for 2 minutes in N_2.

The final two photolithography steps were used for the interconnect of alternating phases of the CCD. An undoped silicate glass was applied with a spin-on technique and densified in N_2 at 450 °C for 60 minutes. Vias were patterned with mask level 8 by etching in buffered hydroflouric acid (BHF). Lastly, 5000 Å of Al is blanket evaporated and etched to define the top pad and interconnect metal.

4.1.2 Ion Implantation Profiles

Ion implantation has been designated as the method for selective junction formation for planar circuits in SiC due to the high temperatures required for impurity diffusion [8]. As a result, a variety of atoms have been implanted into 3C- and 6H-SiC to investigate the basic technology. Results showed that p-type material implanted with nitrogen was converted to n-type for activation temperatures as low as 750 °C, and most of the activation occurs within the first 2 minutes above 1000 °C [95]. Systematic studies of annealing behavior showed full recrystallization of implanted areas above 1000 °C [96], and n^+ sheet resistances in 3C-SiC decreased monotonically for temperatures up to 1600 °C [97], [98]. Implantation at elevated temperatures provided *in situ* annealing and allowed lower activation temperatures, leading to the first depletion and enhancement mode self-aligned MOSFETs in 3C-SiC [99]. Elevated temperature implantation was later validated in 6H-SiC with n+p diodes [100] and inversion channel MOSFETs [19].

Ion implantation was chosen over epitaxial growth [101] as the method for channel formation in this work in order to investigate a variety of doping profiles. Therefore, an analysis of methods to predict irnplanted depth profiles was necessary. Unfortunately, single energy implant profiles of atoms are shallower and narrower in SiC as compared to Si [102]. Also, redistribution of implanted atoms in SiC is assumed negligible during implant activation. Therefore, multiple energy/dose implants are required to achieve rectangular channel profiles and junction depths that are practical for BCCD applications. The device parameters in Section 3.2 are strongly related to channel doping

and depth, so a precise knowledge of the depth profile of implanted nitrogen is crucial to the electrical performance of the device.

The multiple implant profile of the SiC BCMOSFET in Chapter 2 was calculated using fitted parameters from the widely used simulation program TRIM [103]. The actual profile was never verified by physical characterization, but the extracted channel doping and depth were 60% higher and 30% shallower than predicted. This indicated perhaps that TRIM calculation:; were not accurate.

4.1.2.1 Empirical depth-profile data

Recent results reported by Ahmed et al. [94] on ion implantation of N, Al, B, and As into 6H-SiC allow for atomic profile calculations that are faster and more accurate than typical Monte-Carlo calculations as in TRIM. In their experiment, each atomic specie was implanted into samples of 6H-SiC for several energies up to 300 keV, and the resultant profiles were measured with secondary ion mass spectroscopy (SIMS). Then, each profile was fit to a Pearson-IV frequency distribution by extracting the first four statistical moments of the spatial profile: projected range (R_p), straggle (ΔR_p or σ_p), skewness (y), and kurtosis (β). Using simple Gaussian distributions cannot be accurate due to ubiquitous channeling effects [104]. The reader is referred to Refs. [105], [106] for the detailed equations required to reproduce a Pearson-IV distribution from the flour moments. Each statistical moment was represented as an empirical function of energy, so that implantation depth profiles could be quickly simulated. For reference, the equations are repeated in Table 4.2.

4.1.2.2 CCD n-channel calculations

Two CCD chips were fabricated (subsequently referred to as CCD_1 and CCD_2) in order to explore different channel profiles and further validate the use of implantation in this process. The two channel profiles were formulated to achieve approximate charge capacities of $1x10^{12}$ cm^{-2} and $3\text{-}5x10^{11}$ cm^{-2}. After determining the doping values of starting p-epilayers by differential-CV on

Table 4.2

Empirical equations describing ion implantation profiles for atoms implanted into 6H-SiC, where E is energy in keV. The four statistical moments can be used to predict an implant depth profile for the given atom specie at energies up to 300 keV. After [94].

	N	Al	B	As
R_p	$2.39E^{0.885}$	$1.58E^{0.945}$	$4.9E^{0.824}$	$1.35E^{0.811}$
ΔR_p	$2.91E^{0.552}$	$1.98E^{0.699}$	$5.44E^{0.511}$	$1.35E^{0.649}$
γ	$2.05 - 0.533 \ln E$	$4.24 - 0.682 \ln E$	$2.47 - 0.551 \ln E$	$6.33 - 0.923 \ln E$
β	$1.03\beta_o$	$1.24\beta_o$	$1.35\beta_o$	$1.04\beta_o$

$$\beta_o = \left[39\gamma^2 + 48 + 6\left(\gamma^2 + 4\right)^{\frac{3}{2}} \right] \Big/ \left(32 - \gamma^2\right)$$

Schottky contacts, the channel dopings and thicknesses were chosen using the design criteria defined in Chapter 3. The target channel parameters were chosen as (a) N_{D1}=1x10^{17} cm^{-3} and x_{j1}=2000 Å and (b) N_{D2}=6x10^{16} cm^{-3} and x_{j2}=2200 Å for CCD_1 and CCD_2, respectively. The corresponding peak atomic concentrations were chosen as N_{o1}=1.2x10^{17} cm^{-3} and N_{o2}=8x10^{16} cm^{-3} because of background acceptor concentrations in the range 1.7-2.1x10^{16} cm^{-3}. We have assumed that 100% of implanted nitrogen can be electrically activated at these low concentrations.

The empirical equations from Table 4.2 and the analytical Pearson-IV distribution equations were used to realize the desired rectangular profiles as closely as possible. With the aid of the computer program listed in Appendix II, an iterative method was used to calculate the profiles shown in Fig. 4.2. The atomic profiles are shifted negatively by 700 Å to account for about 200 Å of oxide screen layer and approximately 500 Å of SiC consumed during subsequent oxidations.

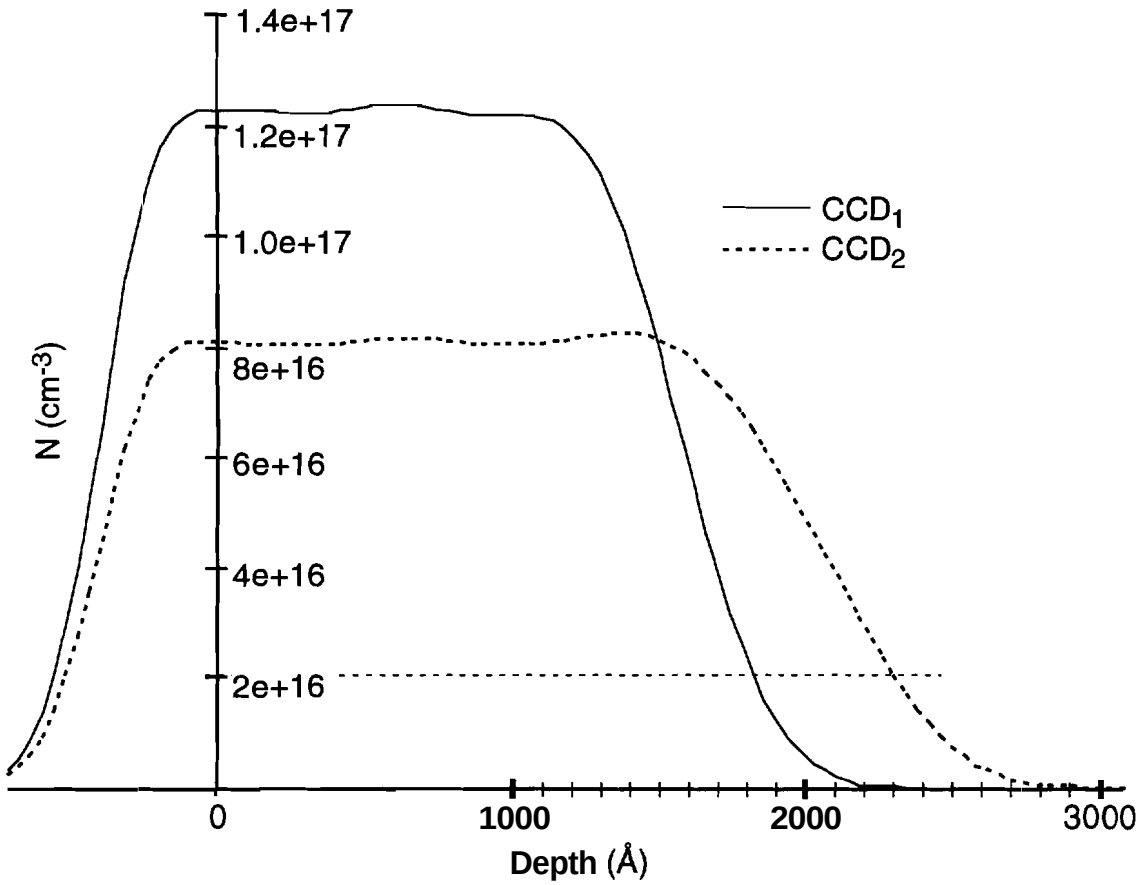


Figure 4.2

Buried channel profiles calculated for the two CCD samples in this work. The profiles are estimated from a set of empirical implant equations reported in Ref. [94]. The background acceptor doping concentration is demarcated by the horizontal dashed line at $2x10^{16}$ cm^{-3}.

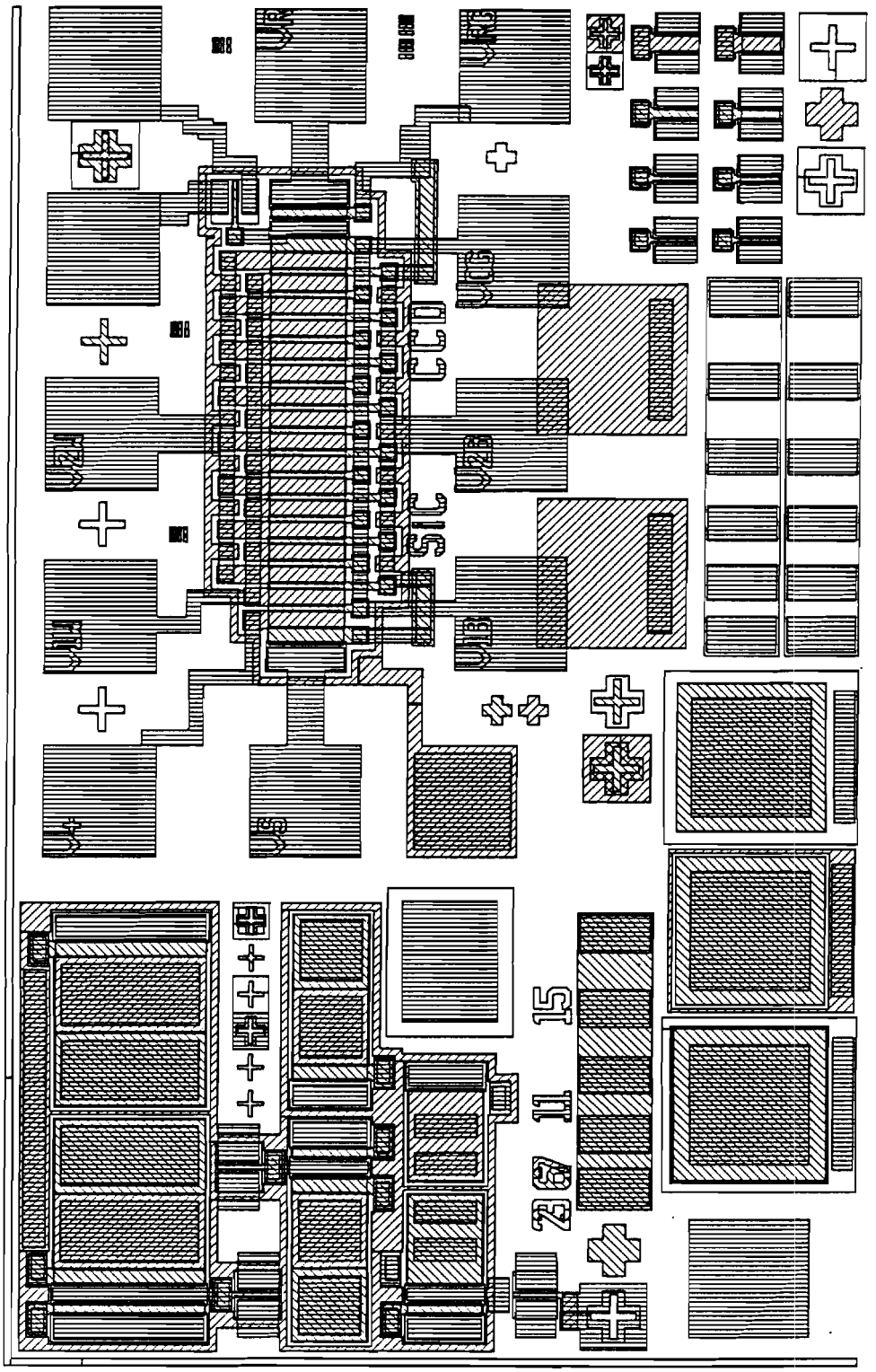


Figure 4.3
Plan view of the CCD test chip.

4.2 Test Devices

In this section, the physical layout of an implanted channel four phase CCD is described. This arrangement is chosen because of its simple fabrication procedure, requiring only two gate levels and one interconnect metallization. Additionally, it has the flexibility to be operated in the pseudo two-phase configuration, which reduces the number and complexity of clock waveforms without the additional fabrication steps normally required for two-phase operation.

A plan view of the test chip designed for these experiments is shown in Fig. 4.3. The CCD structure occupies most of the area because of the large bonding pads required for testing the device. A variety of test structures were included on the die to facilitate the types of measurements used in Chapter 2. These diagnostic structures included MOSFETs and MOS-Cs for both gate levels, transmission line resistors of Ni contacts to n+, Al and Ni Schottky contacts to the p-epilayer, and various process testers. Additionally, a powerful set of basic charge transfer devices (CTDs) were incorporated for characterizing the charge transfer concept in the buried channel.

4.2.1 Charge Transfer Test Devices

The basic charge transfer device used in this experiment resembles the output portion of a CCD as described in Section 3.1 - Figure 4.4 depicts the layout of the largest CTD and labels all of the relevant design rules. The two large area capacitor plates serve as electrodes that can store charge similar to an oversized end stage of a linear shift register. The n-channel implanl: region is 200 microns wide, and the length of each storage node (V_1 and V_2) is 100 microns. The output transfer gate is 20 microns long over the n-channel. The gates adjacent to source/drain regions overlap the n^+ implant and the 2nd level polysilicon overlaps the 1st level gate. In both cases, a maximum overlap of 2 microns (corresponding to 2X the single level misalignment tolerance) is used to minimize capacitance between electrodes and decrease the chance of current leakage through the inter-electrode dielectric. The gates also extend past the edge of the n-channel by 2 microns.

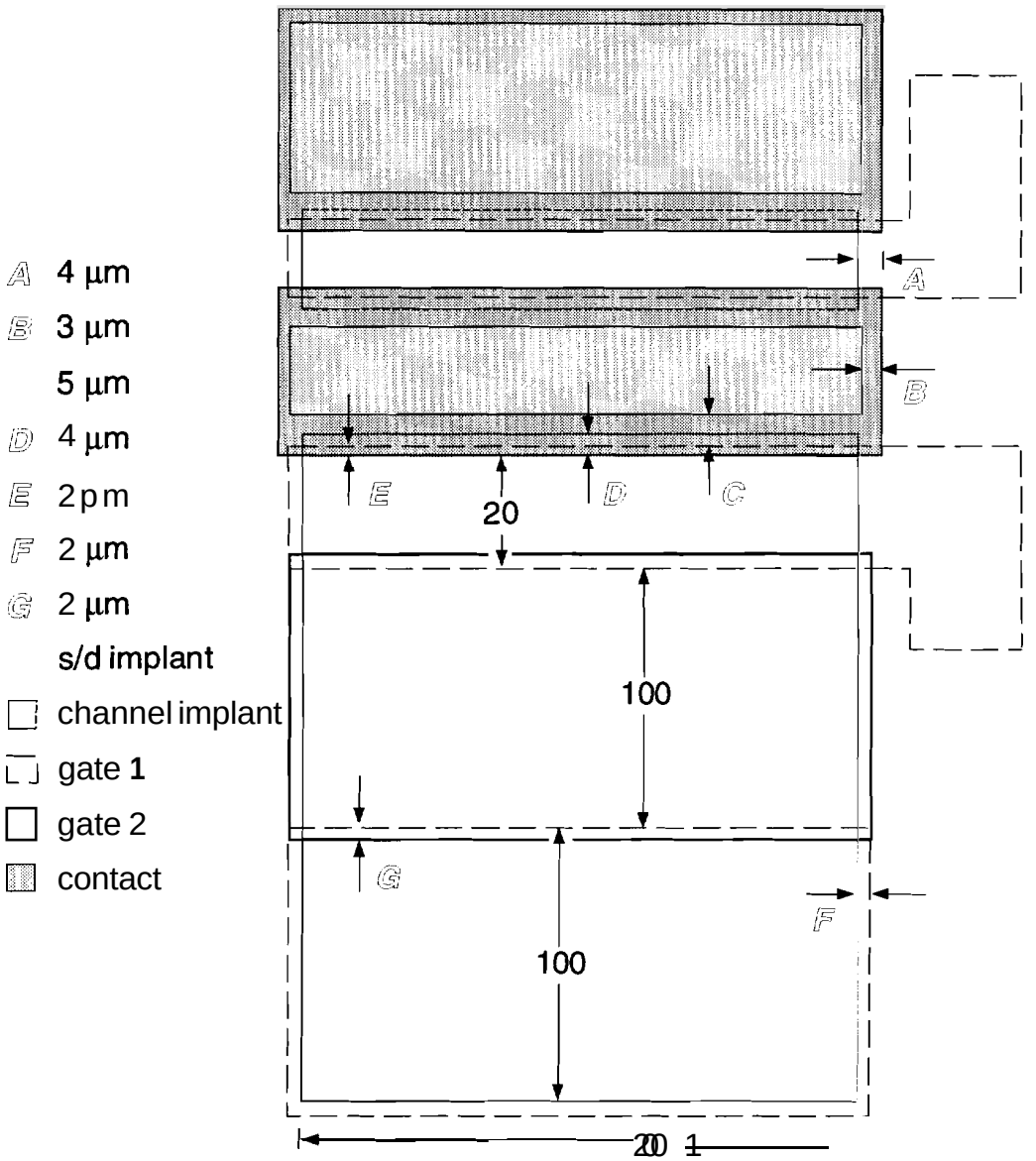


Figure 4.4

Detail of the largest floating node CTD on the CCD test chip (not to scale). Relevant design spacings are shown.

The n^+ source and drain islands on this chip extend past the n-channel by **4** microns on each side. Also, a minimum contact dimension of **16** x **16** µm and a contact-to-gate spacing of 5 microns determined the minirnum allowable length for the n^+ regions between two gates. Since the capacitance should be minimized due to charge sharing considerations, the area of the output diode was chosen as 30 x 208 µm. The adjacent amplifier MOSFET (shown in Fig. 4.3) has a gate area of **4** x 54 µm.

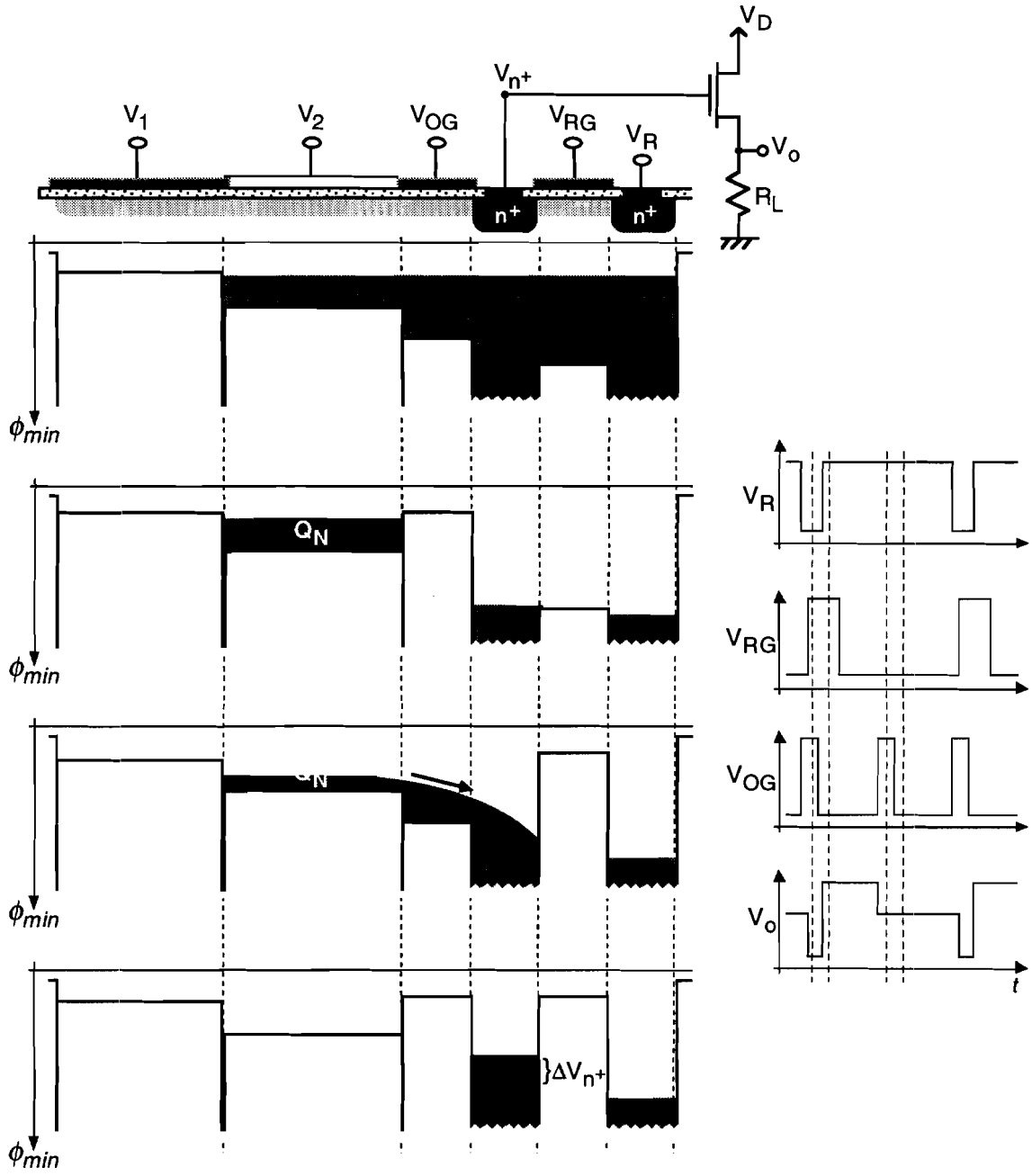


Figure 4.5

Operation of a charge transfer test device. A well under V_2 is purposely filled with electrons and then isolated from the output by the transfer gate, V_{OG}. At this point, the device resembles an output stage of a linear CCD with charge in the last stage. The floating node is reset and left floating before the charge Q_N is coupled into it. V_1, V_{OG}, and V_{RG} are polysilicon level 1. V_2 is polysilicon level 2. An example set of clock waveforms for this device is shown.

The operation principle of the test CTD shown in Fig. 4.5 is just a variation of the charge readout procedure discussed in Section 3.1.1.A well under V_1 is purposely filled with electrons and then isolated from the output by transfer gate, V_{OG}. At this point, the floating node is reset by potential equilibration and left floating before the charge Q_N is coupled into it. The charge magnitude can be measured by a change in output of the MOSFET amplifier, V_o. This measurement is important in establishing that charge can be injected (or not injected) into a potential well, stored, and subsequently read out and detected with the source follower amplifier circuit.

4.2.2 Linear CCD Test Structure

A photomicrograph of a completed four phase SiC CCD is shown in Fig. 4.6. The device connections are labeled for pseudo-two phase operation. This CCD is from one of the first processing iterations with aluminum 2nd level gates,

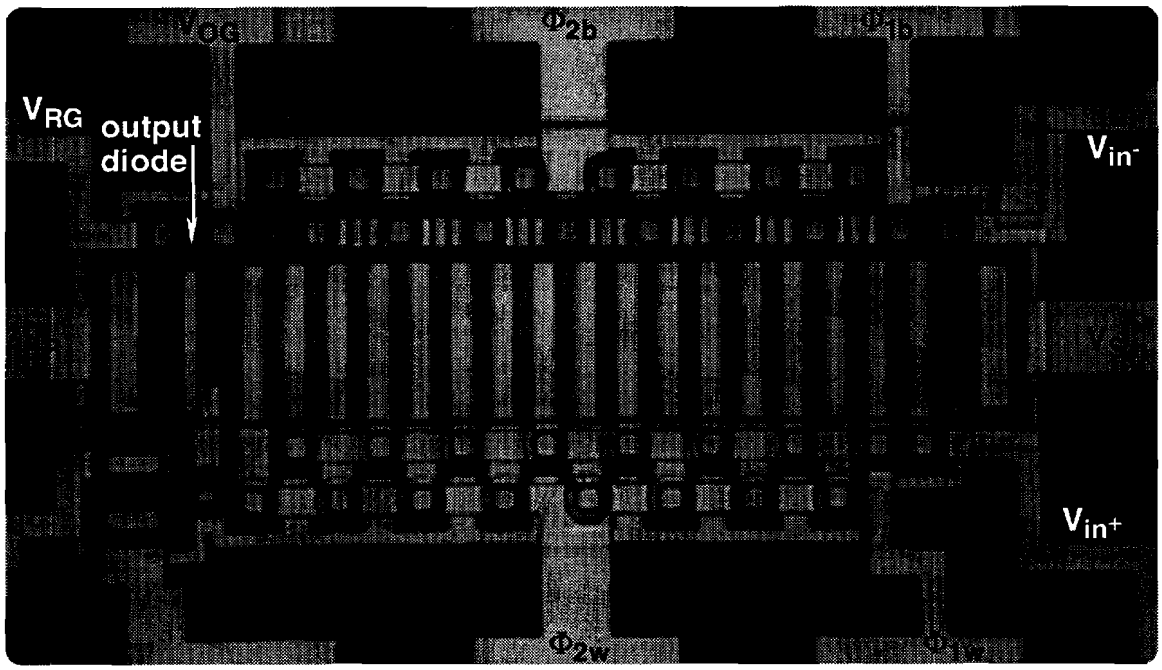


Figure 4.6

Photomicrograph (X200) of a completed SiC BCCD including top metallization. The device connections are labeled for pseudo-two phase operation. This CCD is from one of the first processing iterations with Al 2nd level gates, giving a good visual contrast between barrier and well portions of each phase.

giving a high visual contrast between alternating electrodes. The n-channel is 100 microns wide and 540 microns long. Two 20 micron input gates are positioned before 32 gates of the CCD proper. Half of the gates are 20 microns long, while the rest are only 10 microns. This facilitates the pseudo-two phase configuration by reducing the transfer length of each phase. A 20 micron long output gate lies between the end stage and a 30 x 108 μm output diode, which is connected directly to the gate of an enhancement type MOSFET with dimensions Z =56 μm and L =4 pm. The active area of the device ends 2 microns outside the n-channel, where the field oxide (FOX) region begins. A 10 micron wide guard ring fashioned from gate level 2 surrounds the entire device.

In the pseudo-two phase mode of operation, the adjacent gates of the four phase CCD are paired as two half electrodes of a single phase. In this configuration, the 32 gates become 8 stages (see Section 3.1.1.2). Potential well asymmetry (PWA) is formed by applying a constant offset voltage V_{dc} between the two half electrodes as shown in Fig. 4.7. The more positive side of the phase! forms a well in the direction of charge transfer. In the design used

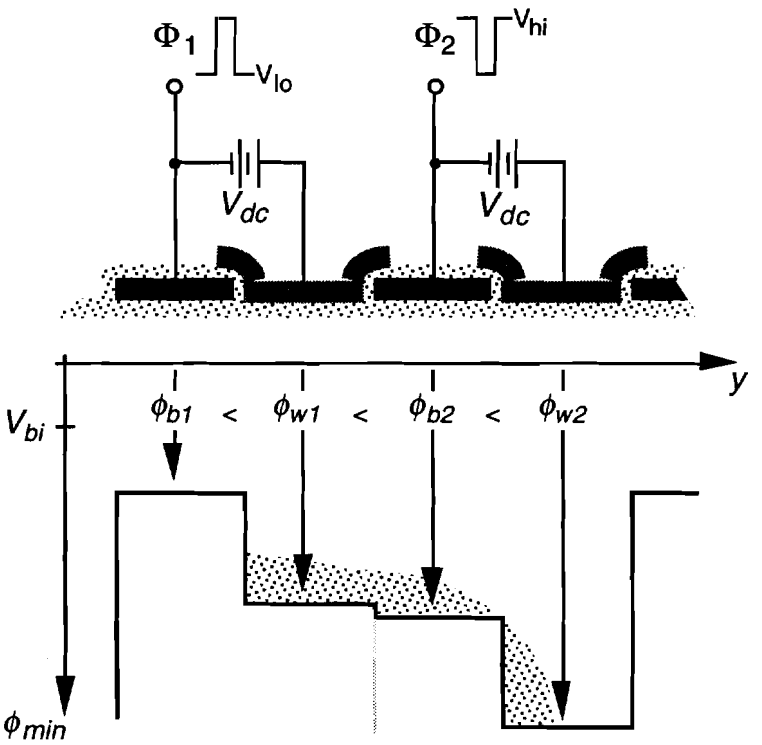


Figure 4.7
Configuration of a four phase CCD operated in the pseudo-two phase mode.

here, the well side of each phase is synonymous with polysilicon layer 2, and the barrier is always under polysilicon layer 1. The pulse trains applied to the two phases (Φ_1 and Φ_2) have maximum and minimum values V_{hi} and V_{lo}, but are 180° out of phase. Charge is moved along the device as shown in the potential minimum diagram in Fig. 4.7. For complete transfer, the barrier of the receiving phase must be pushed below the well of the sending phase; in this example, $\phi_{b2} > \phi_{w1}$.

The three characteristic clocking voltages can be chosen from the operating domain plot of a given device (Sect. 3.2.4). Fig. 3.12 is repeated in Fig. 4.8, showing the method of determining V_{lo}, V_{hi}, and V_{dc}. For a charge packet size of $Q_n/(-q)$ equal to 8×10^{11} cm^{-2}, the pseudo-two phase device can be operated with V_{lo}=-5 V, V_{hi}=3 V, V_{dc}=7 V. A difference in flatband voltages under the two gate levels can be compensated with a different offset voltage by:

$$V'_{dc} = V_{dc} + \left(V_{FB}^{well} - V_{FB}^{barrier}\right). \tag{4.1}$$

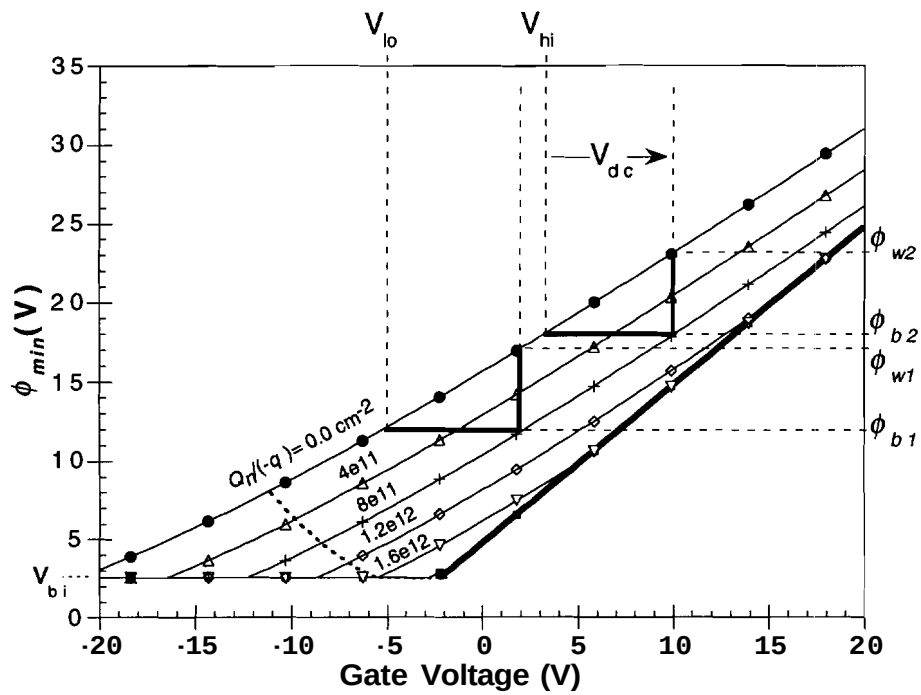


Figure 4.8

An illustration of how to choose clocking voltages of a CCD for the pseudo-two phase mode of operation. The operating domain plot of Fig. **3.12** is used as an example.

4.3 MOS Test Structures

The electrical characterization of the CCD wafers was divided into three major parts, starting with measurements of the diagnostic MOS devices described in this section. Then, the vital information was used to test the charge transfer device (CTD) and demonstrate the CCD as described in Sections 4.4 and 4.5, respectively. All measurements were performed under probe test at room temperature (296 K) in the dark. Although charge-transfer measurements are only given for CCD_1 in later sections, CV and IV measurements are reported for both CCD_1 and CCD_2.

4.3.1 MOS Capacitor Results

A comparison of the oxide quality under both gate levels for CCD_1 and CCD_2 began with simple high-frequency CV measurements of MOS-Cs over the p-epilayer material. Initial results were discouraging because of the large negative flatband voltage observed for polysilicon level 1 of both samples. Typical values of V_{FB} were -15.5 V and -14.5 V for CCD_1 and CCD_2, respectively. Using a metal-semiconductor workfunction difference of -2.1 V for n^+ polysilicon on p-SiC, the effective fixed charge lies in the range 3.8 - 4.1 $\times 10^{12}$ cm^{-2}.

The results were poor despite the very careful procedures followed for the gate oxidation of these samples. Further experiments to be discussed in Chapter 5 have shown that the large fixed charge is attributed to any high temperature processing step performed when the polysilicon gate is present. This fact was not known during the doping process of polysilicon layer 1, and a high drive-in temperature of 1050 °C was based on the product specifications of the arsenic spin-on glass.

Fortunately, these undesirable effects were detected prior to deposition and doping of polysilicon level 2 because of a process monitor sample. The arsenic drive-in conditions were changed to 950 °C for 20 minutes to ameliorate the oxides. Flatband voltages improved to -7 V for CCD_1 and -6.5 V for CCD_2, yielding effective fixed charge values of 1.6×10^{12} cm^{-2} and 1.5×10^{12} cm^{-2}, respectively. The results for both gate levels are summarized in Table 4.3.

Table 4.3
Summarized results of MOS capacitors over the p-epilayers of CCD_1 and CCD_2. A ϕ_{ms} of -2.1 V is used to calculate effective fixed charge.

	poly-Si	t_{ox} (Å)	V_{FB_p} (V)	Q'_{f_p}/q (cm^{-2})
CCD_1	level 1	708	-15.5	$4.1x10^{12}$
	level 2	645	-7.0	$1.6x10^{12}$
CCD_2	level 1	708	-14.5	$3.8x10^{12}$
	level 2	650	-6.5	$1.5x10^{12}$

It is worthwhile to mention another processing difference between the two samples (in addition to the differing channel profiles). The 1st level polysilicon layer of CCD_1 was wet-etched, while CCD_2 was etched by RIE in SF_6. Both the etches were calibrated for high selectivity between polysilicon and the underlying SiO_2, and only 50 - 60 Å of SiO_2 was removed. Despite the likelihood of plasma induced radiation damage in the exposed oxide [107] during the RIE of sample 2, the fixed charge for both samples are similar. Any plasma damage that may have been incurred was either (a) "cured" or removed during the subsequent thermal oxidation of the inter-gate dielectric, or (b) insubstantial compared to other effects that determine SiC-MOS characteristics.

4.3.2 Buried-channel Gated Diodes

Following the CV measurement technique outlined in Section 2.2.2.1, the MOS characteristics of the BCGDs were analyzed for the four gates (two gate levels per CCD sample). The measurements were performed at 10 kHz due to the large device areas and high series resistances at pinchoff.

Characteristic capacitance curves for the two gate levels on both chips are shown in Fig. 4.9. The average channel doping concentrations for each sample were extracted by differential CV methods. Representative values from several devices were N_{D1} =1.6x10^{17} cm^{-3} and N_{D2} =8.5x10^{16} cm^{-3}. These values are not influenced by interface states because they are extracted from the depletion portion of the CV characteristic. The "n-type" flatband voltages (for zero diode bias) were found from the calculated flatband capacitance of each

curve. The results are summarized in Table 4.4, including effective fixed charge numbers.

A crude observation for the number of surface states under each gate can be made by relating the "p-type" effective fixed charge (Table 4.3) to the "n-type" fixed charge with

$$N_{IT} = \frac{1}{q}\left(Q'_{f_p} - Q'_{f_n}\right). \tag{4.2}$$

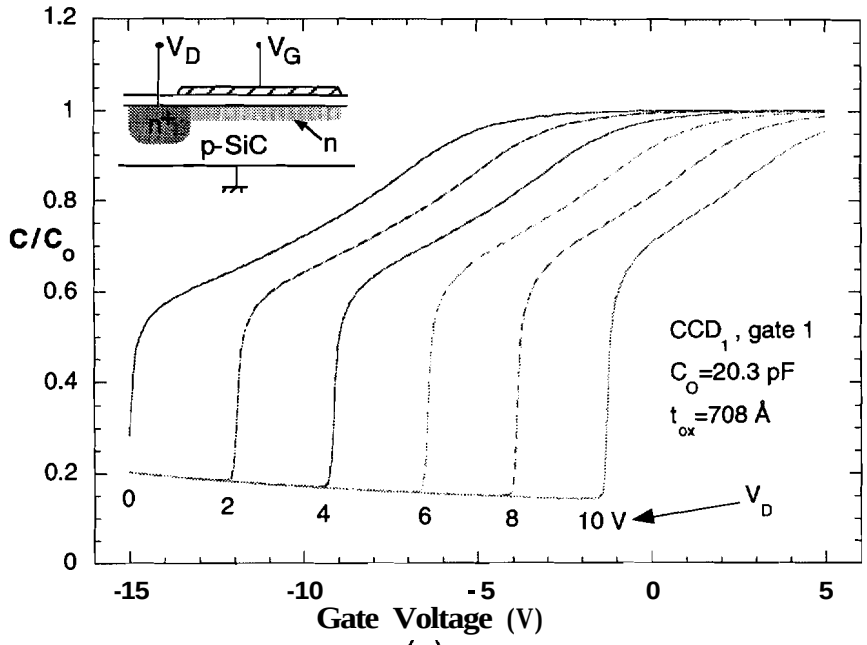
These are also listed in Table 4.4, showing that the higher surface state density correlates with the higher 1050 °C drive-in temperature used for doping polysilicon level 1. In silicon, such a large value of interface states would preclude any reasonable attempt to operate a CCD. The silicon carbide buried channel device can be operated with such a large value of N_{IT} because the deep level interface states will not change charge at room temperature. Both directional sweeps are shown in the CV curves of Fig. 4.9, but no surface state hysteresis is observed.

Various values of pinchoff voltage were extracted from many devices, including the ones of Fig. 4.9, and were plotted in the two graphs in Fig. 4.10 (a) and (b). The slight scatter in values is due to the variation over devices and to the arbitrary graphical method of choosing Vp. A best fit value for junction depth was found using Eq. (3.25) (recall $\phi_{min} = V_{ch} + V_{bi}$) and the previously extracted values of t_{ox}, N_A, V_{FB_n}, and N_D. The solid lines show the relationship for junction depths x_{j1} =1830 Å and x_{j2} =2250 Å, validating the use of the 1-D channel model derived in Chapter 3.

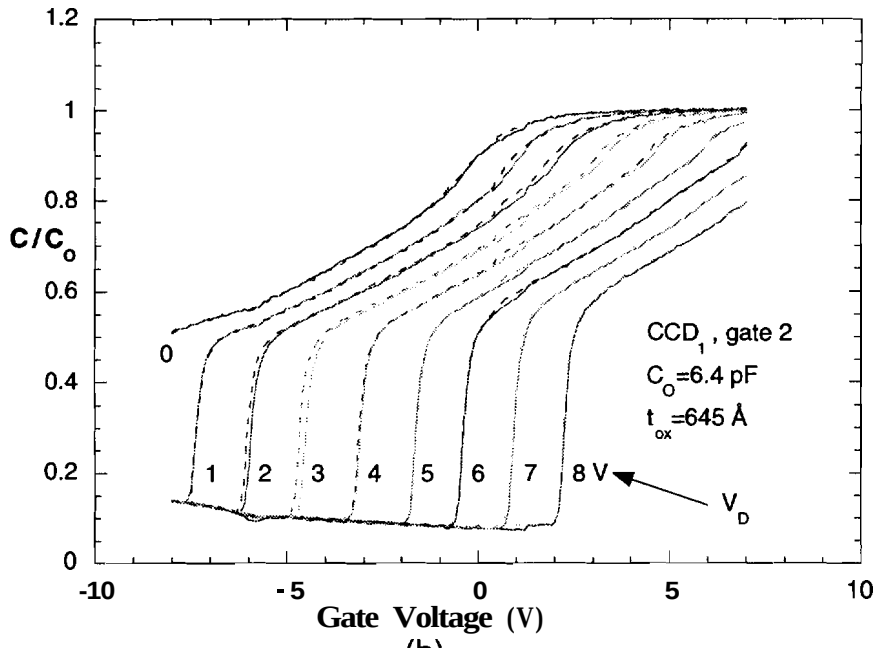
Table 4.4

Summarized results of MOS capacitors over the n-channel regions of CCD_1 and CCD_2. A ϕ_{ms} of 0.0 V is used to estimate effective fixed charge. The total nunnber of interface traps N_{IT} under each gate accounts for the difference between effective fixed charge over n- and p-type material.

	poly-Si	t_{ox} (Å)	V_{FB_n} (V)	Q'_{fn}/q (cm-2)	N_{IT} (cm^{-2})
D	level 1	708	-5.0	1.5×10^{12}	2.6×10^{12}
	level 2	645	0.5	-1.7×10^{11}	1.8×10^{12}
D	level 1	708	-5.3	1.6×10^{12}	2.2×10^{12}
	level 2	650	0.6	-2.0×10^{11}	1.7×10^{12}



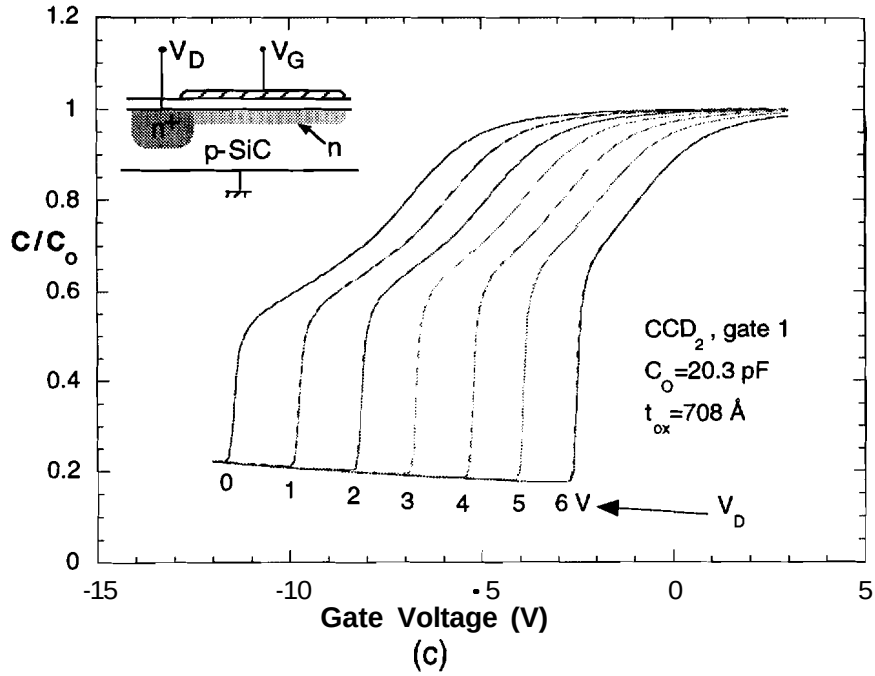
(a)



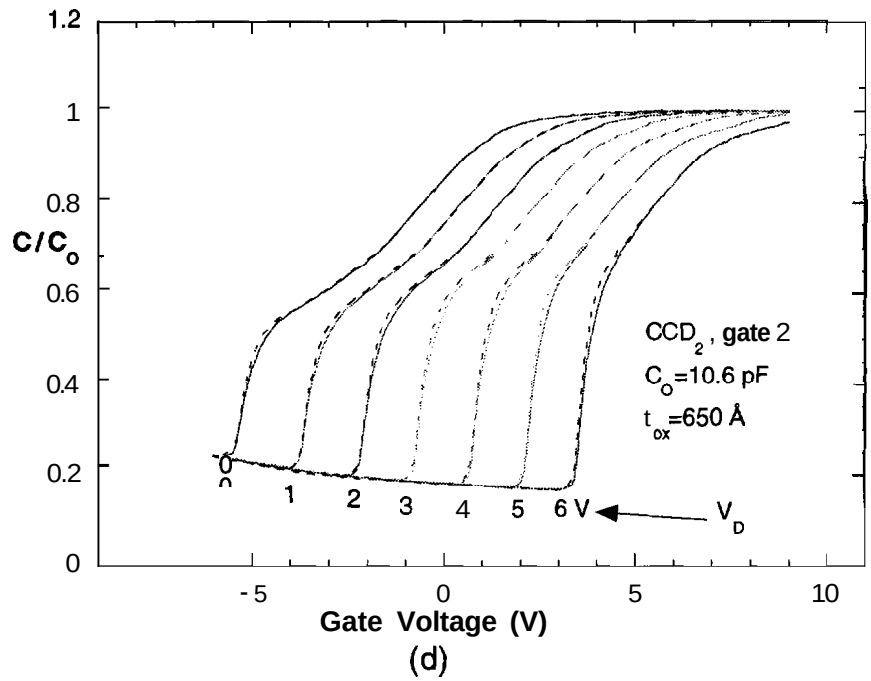
(b)

Figure 4.9

(a) and (b) BCGD capacitance measurements on both gates of CCD_1.



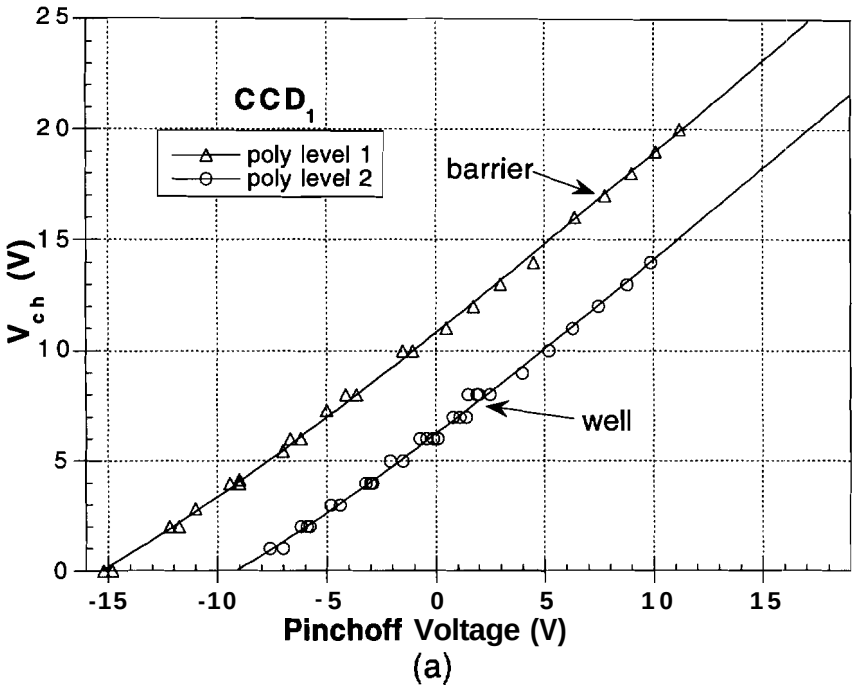
(c)



(d)

Figure 4.9

(c) and (d) BCGD capacitance measurements on both gates of CCD_2.



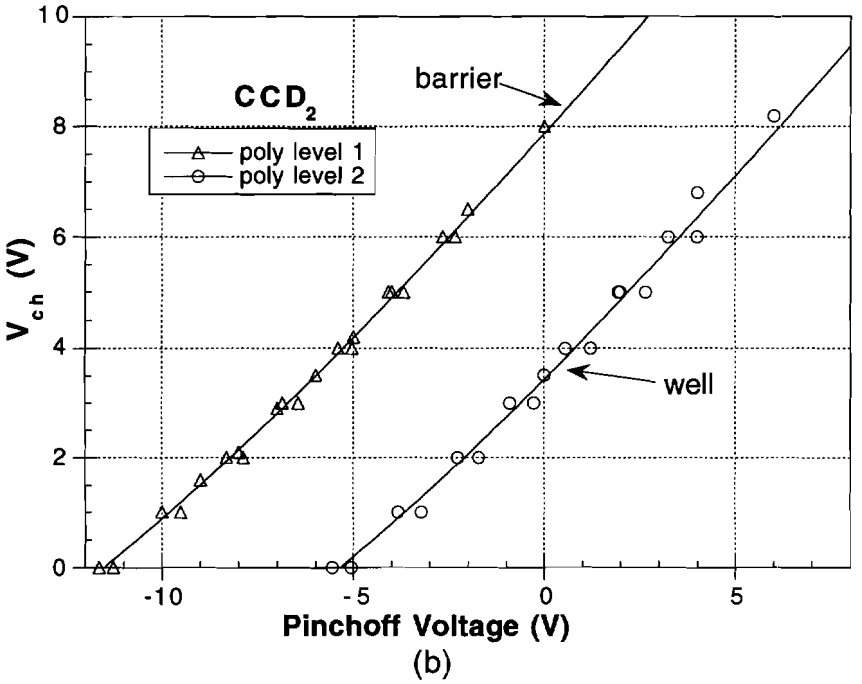


Figure 4.10

Values of pinchoff voltage extracted from BGCD measurements of (a) CCD_1 and (b) CCD_2. The solid lines represent fits to the data according to Eq. (3.25).

4.3.3 Buried-channel MOSFETs

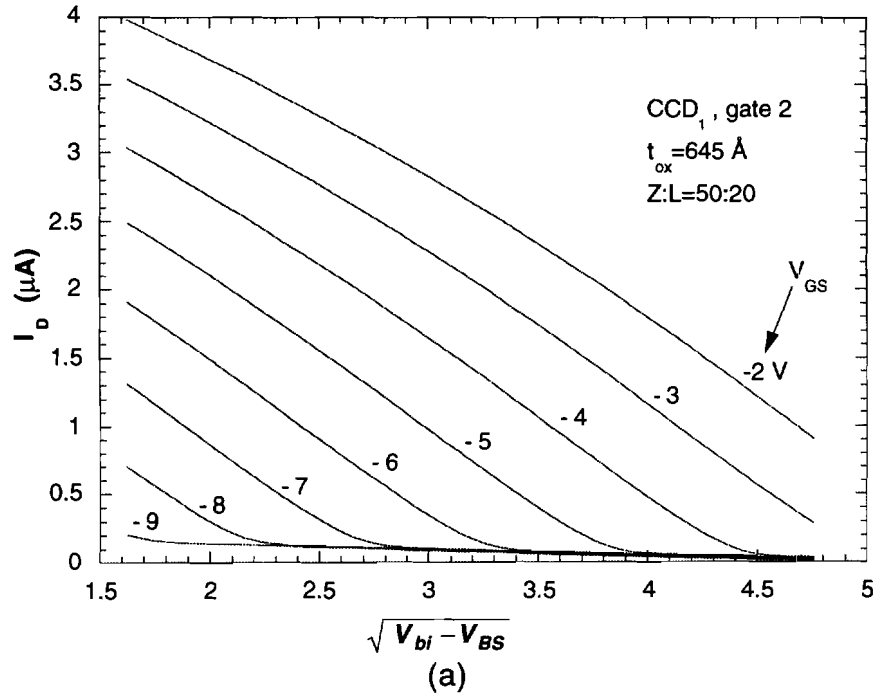
Linear transistors were analyzed to find electron mobility values in each of the implanted channels, which is important for estimating the speed performance of the CCD shift register. Recall from Chapter 2 that the mobility measurement is based on the influence of substrate bias on drain current in the linear region, when $V_{DS} \approx 0$. Due to high series resistances in these CCD samples, the equation for calculating channel mobility must be modified as

$$\frac{1}{\mu_n} = \frac{(V_{DS} - R_S I_D)^2}{\frac{d}{d\Theta} I_D} \frac{n_{ch}}{N_D} \frac{Z}{L} \sqrt{2 K_S \varepsilon_o q \left(\frac{N_D N_A}{N_D + N_A} \right)} \quad \text{(cf. Eq. 2.12),} \tag{4.3}$$

where $\Theta = \sqrt{V_{bi} - V_{BS}}$, and mobility is assumed constant over the gate voltage range of interest. In (4.3), R_S is the total drain to source series resistance. Plots of I_D vs. Θ for CCD_1 and CCD_2 are shown in Fig. 4.11 (a) and (c). Series resistance values for these MOSFETs were estimated at 3.9 kΩ with the transmission line method. Corresponding mobility figures are calculated and also plotted in Fig. 4.11, giving conservative estimates for channel electron mobility for CCD_1 and CCD_2 as 200 cm^2/Vs and 240 cm^2/Vs, respectively.

4.4 Charge Transfer Device Operation

An experiment was conducted to demonstrate basic charge transfer in the implanted channel of CCD_1. Speed of the output circuit was estimated by observing the potential equilibration process in the reset transistor and by measuring the rise time at the output of the source-follower amplifier. Also in this section, influence of gate leakage and parasitic shunt leakage of the BC transistors are explained.



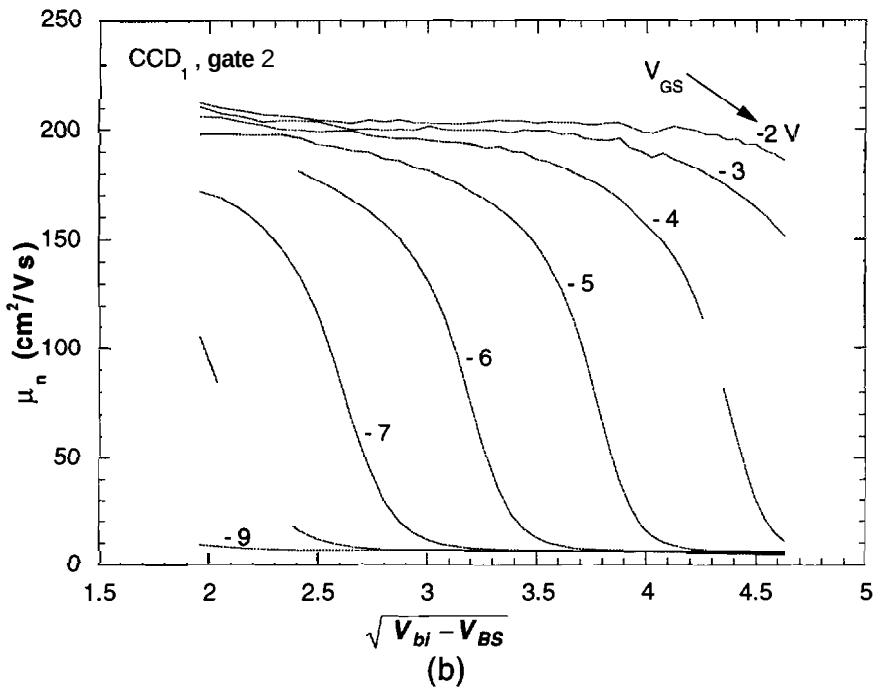
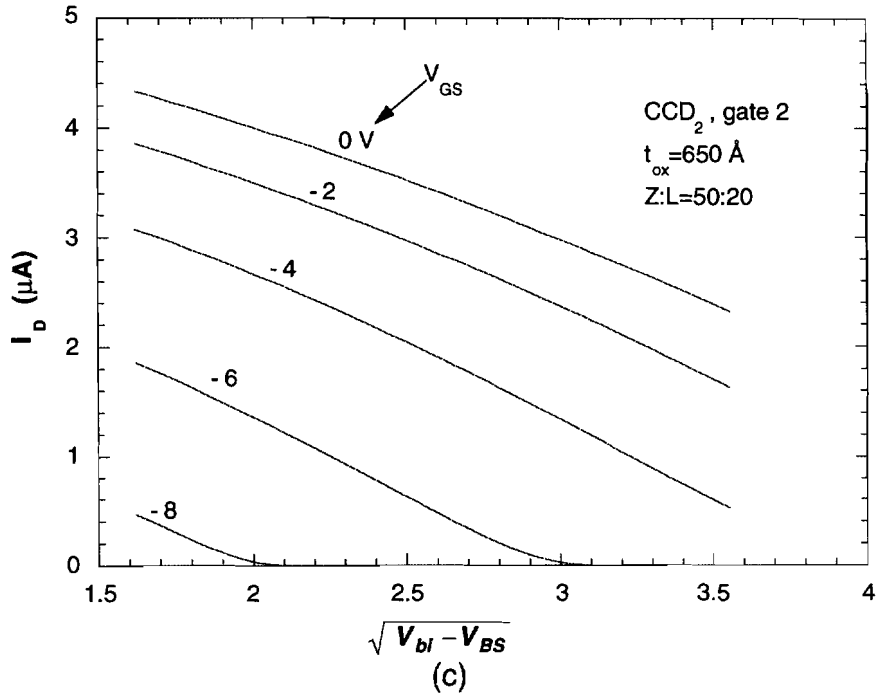


Figure 4.11

(a) Drain current vs. $\sqrt{V_{bi}-V_{BS}}$ for a BCMOSFET on CCD_1, gate 2. (b) Mobility extracted using R_S =3.9 kΩ and Eq. (4.3).



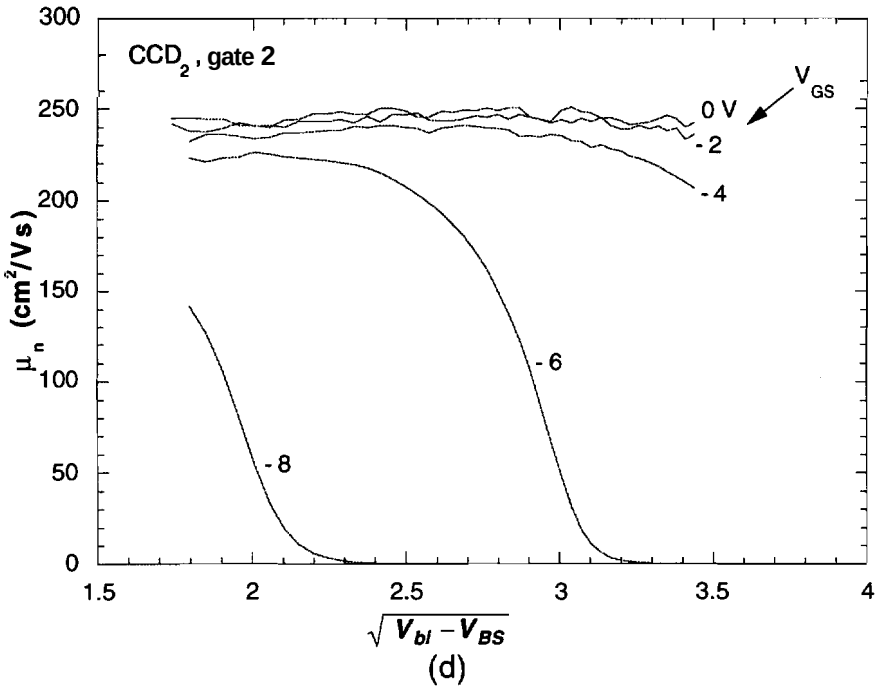


Figure 4.11

(c) Drain current vs. $\sqrt{V_{bi}-V_{BS}}$ for a BCMOSFET on CCD_2, gate 2. (d) Mobility extracted using R_S=3.9 kΩ and Eq. (4.3).

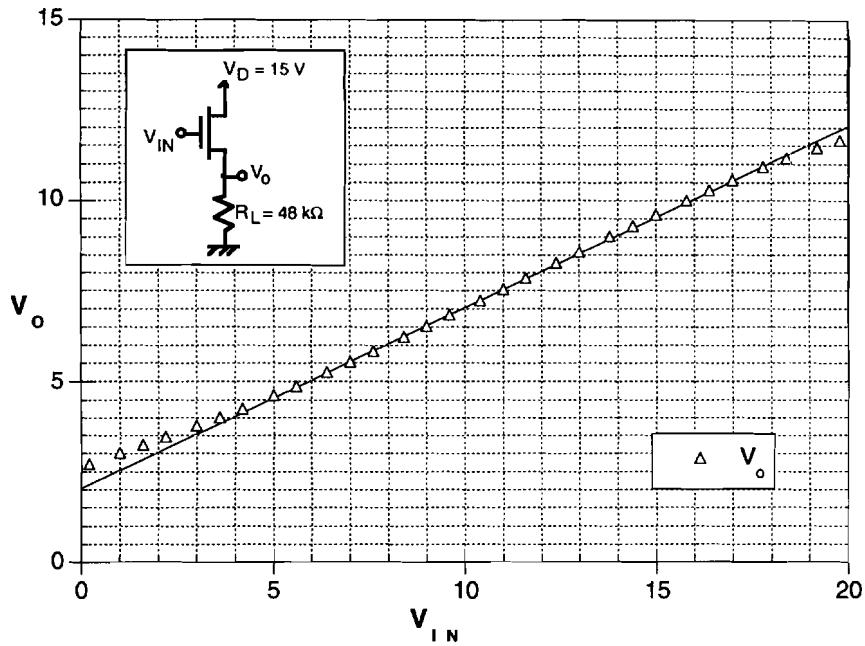


Figure 4.12

Transfer characteristic of the source follower amplifier attached at the output node of the CTD. The MOSFET is integrated on-chip and the load resistor is external. The gain is 0.5 over the input voltage range of interest.

4.4.1 Source Follower Buffer Amplifier

All of the amplifier MOSFETs on the chip were configured as surface channel devices with a 4 micron gate length. Due to high series resistance and poor surface conditions, the transconductances were quite low (g_m ~ 0.4 mS/mm). According to Eq. (3.3), the load resistance can be arbitrarily chosen to increase the source follower gain towards unity. However, this also arbitrarily reduces the bandwidth of the simple amplifier and increases the signal rise time for a step input, so a tradeoff arises in this method of determining packet size.

The output transfer characteristic of the source follower circuit on the CTD is shown in Fig. 4.12, using V_D=15 V and R_L=48 kΩ. The linear fit to the measured points (open triangles) shows a linear response with a 0.5 gain over the input voltage range of interest. The output voltage is non-zero at zero V_{IN} due to a negative threshold voltage on these transistors. A simple speed measurement was conducted by applying a square wave directly to the

amplifier input. Corresponding rise and fall times are on the order of 5 μs, limiting the frequency of operation to below 100 kHz.

4.4.2 Characteristic Leakage Currents

In the operation of the CCD output circuit, the reset voltage of the floating node is ideally determined by potential equilibration with the bottom of 'the well under the reset gate V_{RG} (see Figs. 3.6 and 4.5). In reality, the potential on the floating node can be very hard to control if parasitic leakage currents are present. Generation currents that typically plague silicon CCD circuits are not considered here because of the wide bandgap of SiC. Unfortunately, other important leakage mechanisms were found on the CCD_1 chip, including parasitic surface channel conduction at n-channel edges and gate leakage. An understanding of these undesirable effects is necessary to interpret CTD and CCD results.

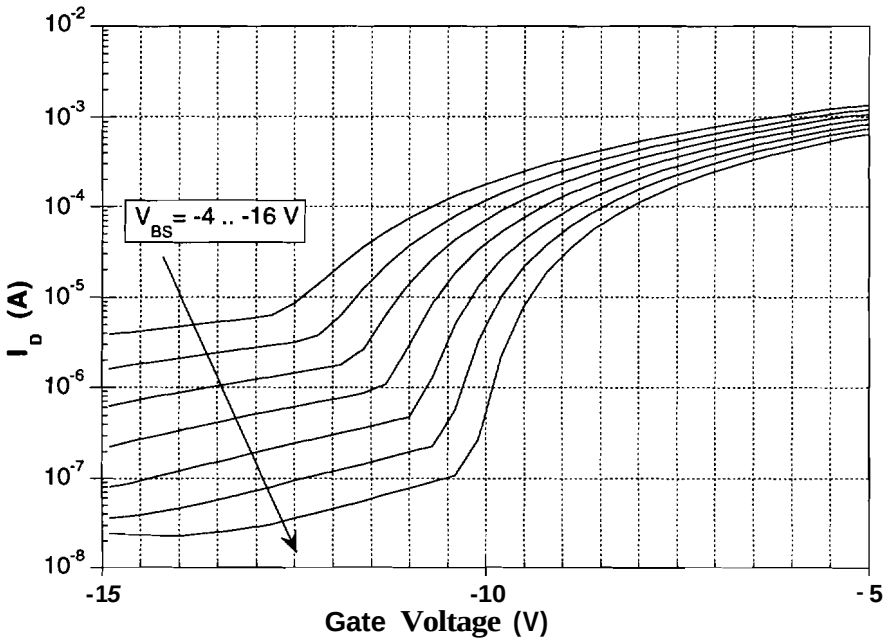


Figure 4.13

Drain current versus gate voltage on the reset transistor of CCD_1, showing parasitic leakage current for several values of V_{BS}. Here, V_{DS}=15 V and the source is grounded.

The initial characterization of the CCD_1 devices showed that the potential of a floating output node could not be controlled by the reset gate, but tended to drift towards the reset potential, V_R. This indicated the existence of a leakage path around the edges of the channel. A typical drain current measurement on a reset transistor is displayed in Fig. 4.13, where the source is grounded, V_{DS}=15 V, and the substrate bias is varied from -4 to -16 V. At the gate voltages that the n-channel should be pinched-off, a residual current on the order of micro-amps flows. This is exaggerated by the large V_{DS}, but alternate measurements with the drain bias at 50 mV showed leakages above 10 nA. Plotting the current on a logarithmic scale shows how strongly the leakage current depends on substrate bias and gate voltage.

A good understanding of how this leakage current affects the charge readout can be found by actually measuring potential equilibration on a reset transistor as shown in Fig. 4.14. A Keithley Model 610C electrometer was used in the high impedance mode to monitor voltage swings on the source while various waveforms were applied to V_{RG} and V_R. According to the data given in Fig. 4.10 for CCD_1 polysilicon level 1, an electrode voltage of zero volts sets the channel potential to approximately 10.5 V. This is demonstrated in Fig. 4.15 (a), when the drain bias is pulsed above (more positive) than the reset channel potential. The source equilibrates to the channel potential in about 40 μs. This slow response is attributed to the electrometer, since a step waveform applied directly at the instrument produces nearly the same rise time (0-'100%). The source voltage should remain pre-charged at this value until the drain is pulsed back to the "fill" part of the cycle.

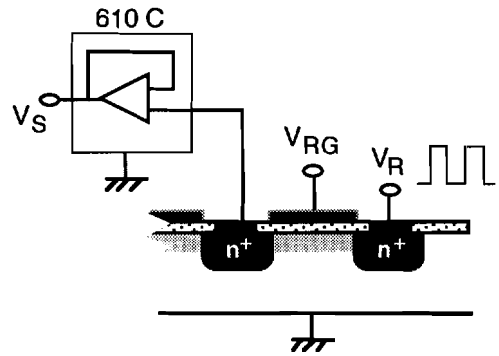
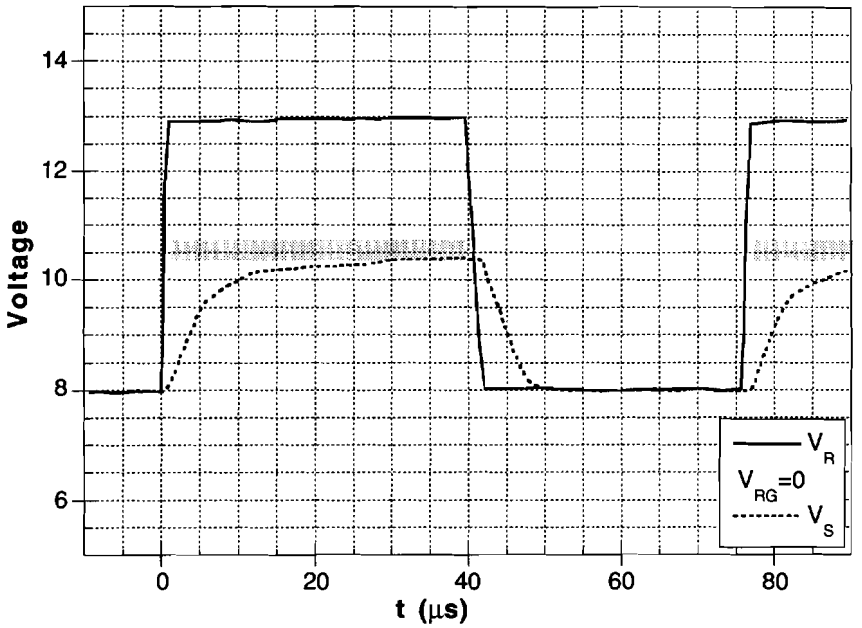
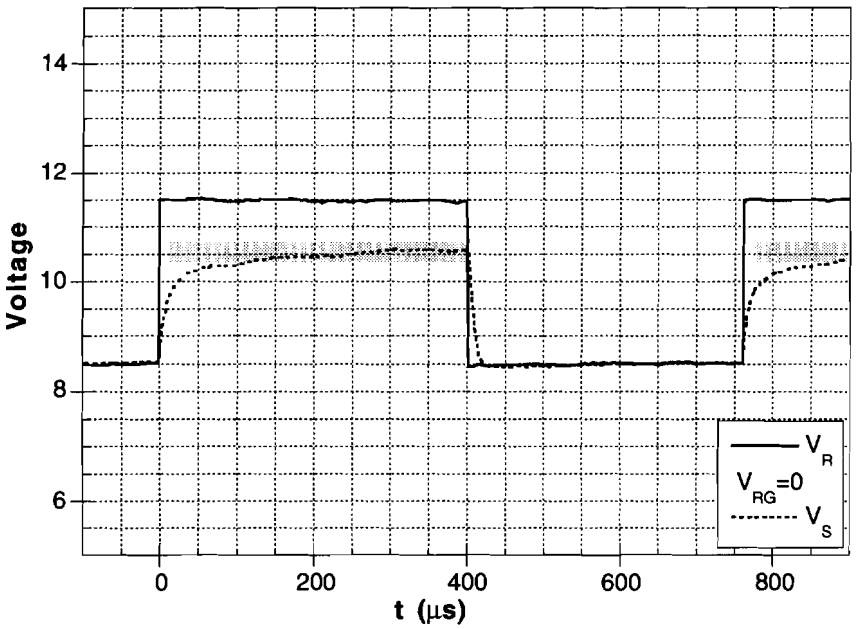


Figure 4.14

Simple measurement configuration for observing potential equilibration on the reset transistor. The source voltage is measured through a Keithley 610C electrometer, which has a high input impedance.



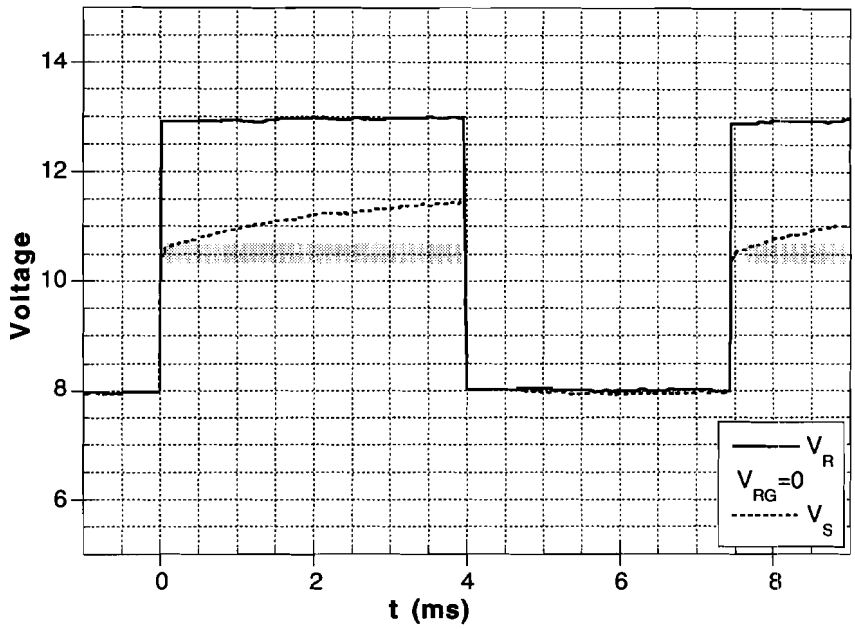
(a)



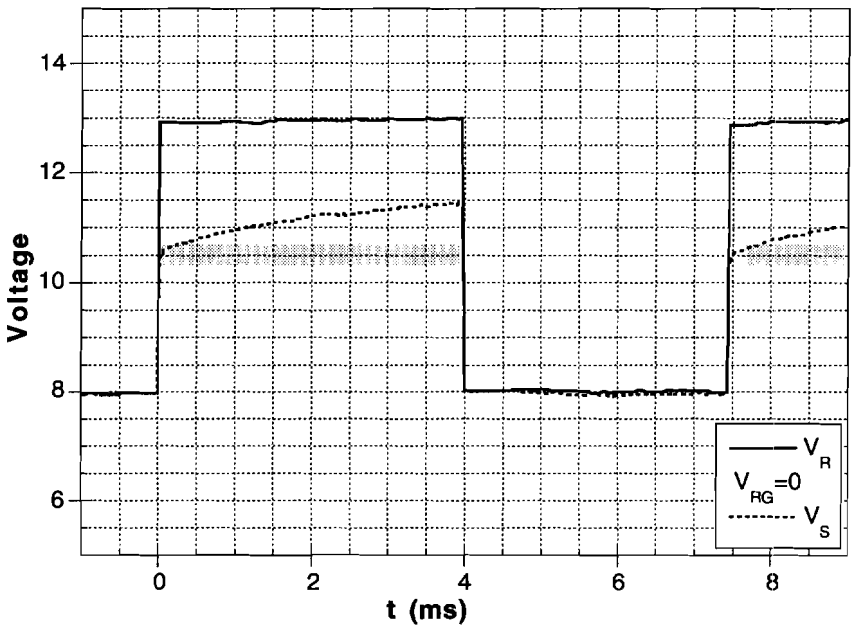
(b)

Figure 4.15

Potential equilibration of the floating output node as measured with a high-impedance voltage monitor. The shaded area is the point that Vs should settle, which is the approximate channel potential under the reset gate for V_{RG}=0.



(c)



(d)

Figure 4.15

Potential equilibration of the floating output node as measured with a high-impedance voltage monitor. The shaded area is the point that Vs should settle, which is the approximate channel potential under the reset gate for V_{RG}=0.

The influence of the source-to-drain leakage becomes evident by reducing the pulse frequency and examining the response over a larger time scale. After equilibration in Fig. 4.15 (b), the source only increases slightly during 400 µs. When the frequency is reduced again in Fig. 4.15 (c), it becomes clearly evident that the source leaks towards the more positive drain bias. The 2 pF floating node changes roughly 1 V in 4 ms, showing that the leakage current is on the order of 50 nA. The effect is further exaggerated in Fig. 4.15 (d), where the source finally reaches the drain bias in about 40 ms.

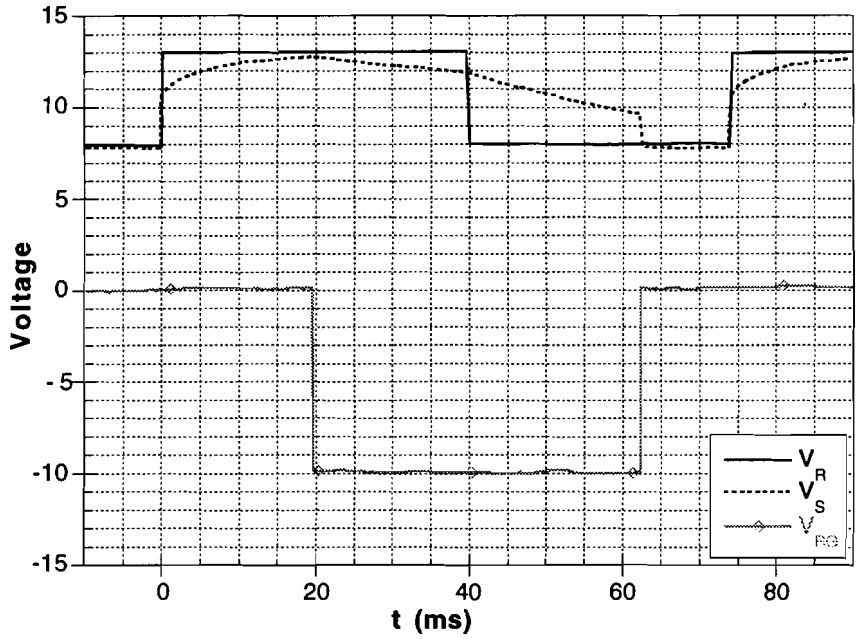


Figure 4.16

Potential equilibration of the floating output node as measured with a high-impedance voltage monitor, characterizing both types of leakage currents. The signal is drawn towards ground when the gate voltage is switched to a large negative value, corresponding to a gate leakage component.

Many of the devices on this chip exhibited nano-amperes of gate leakage when the gate bias was large and negative compared to the n+ islands. This had an effect on the floating source that is opposite the source-to-drain leakage as demonstrated in Fig. 4.16. During the first 20 ms, the source nearly reached V_R as shown previously, but the trend actually reversed when the reset gate voltage was stepped negative, indicating that electronic charge was leaking into the floating node faster than parasitic drain current could remove it. The effect was not as dramatic if the gate was switched to -5 V instead of -10 V.

4.4.3 Calculation of Charge on the Output Diode

The total output capacitance C_{out} is comprised of the variable diode depletion capacitance and other stray capacitances that are constant, including gate capacitance of the amplifier MOSFET and gate overlap capacitance to V_{RG} antl V_{OG}. Considering the dimensions of the CTD in Fig. 4.4 and an epilayer doping concentration $N_A = 1.7 \times 10^{16}$ cm^{-3}, C_{out} is calculated with respect to V_{n+} antl plotted in Fig. 4.17 over the voltage range of interest. The stray capacitance component of C_{out} totaled 0.21 pF.

The charge stored on a variable capacitance such as C_{out} must be calculated by integrating the differential charge $dQ = CdV$. Using the depletion approximation for a one sided abrupt n+p junction, the expression for the total charge on the output node is written as

$$Q_{OUT} = \sqrt{2K_S\varepsilon_o qN_A}\left(\sqrt{V_{bi}+V_{n^+}} - \sqrt{V_{bi}}\right)A_{n^+} + C_W V_{n^+}, \tag{4.4}$$

where A_{n+} is the area of the n+ diode, V_{bi} is the built-in potential, and C_W is the stray capacitance. The total charge is also plotted in Fig. 4.17. When a step change in diode potential is observed due to a charge leaving or entering the node, we have

$$Q_N = \sqrt{2K_S\varepsilon_o qN_A}\left\{\sqrt{V_{bi}+V_a} - \sqrt{V_{bi}+V_b}\right\}A_{n^+} + C_W\left(V_a - V_b\right), \tag{4.5}$$

where $\Delta V_{n+} \equiv V_a - V_b$. Given the voltage swing ΔV_{n+}, the corresponding signal charge can be graphically calculated from Fig. 4.17 as

$$Q_N = Q_{OUT}(V_a) - Q_{OUT}(V_b). \tag{4.6}$$

Note V_a and V_b represent the voltage swing at the output node, not the output of the buffer amplifier. For convenience in determining the charge directly from output waveforms, the output voltage is labeled at the top of Fig. 4.17 according to the transfer function of the source follower amplifier as measured in Fig. 4.12.

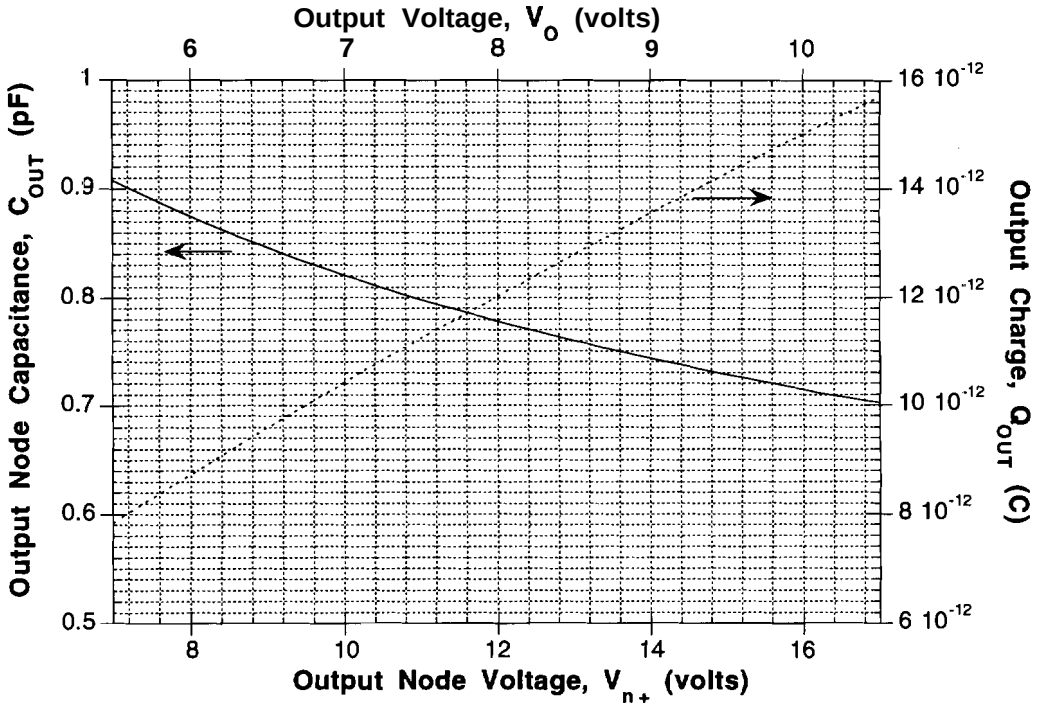


Figure 4.17

Variable capacitance and output charge of the floating n+ island at the CTD output. The stray capacitance C_W is about 0.21 pF, the diode area is 30 x 208 µm, and the p-side doping is 1.7×10^{16} cm^{-3}.

4.4.4 Charge Transfer

The charge transfer concept was demonstrated in these devices (CCD_1) according to the experiment outlined in Section 4.2.1. The eight terminal "circuit", including the backplane and amplifier MOSFET, was measured under probe test. Drive waveforms and output were monitored and stored with a Tektronix 11401 digitizing oscilloscope.

The rectangular waveforms V_R, V_{RG}, and V_{OG} were realized with three triggerable function generators on which the duty cycle, pulse magnitude, dc offset voltage, and trigger delay were adjustable. A simple frequency divider circuit was used to synchronize the waveforms. It was realized with an SN5473 four-bit binary counter configured to count continuously. The input master clock at frequency f was supplied by a fourth function generator. The output gate

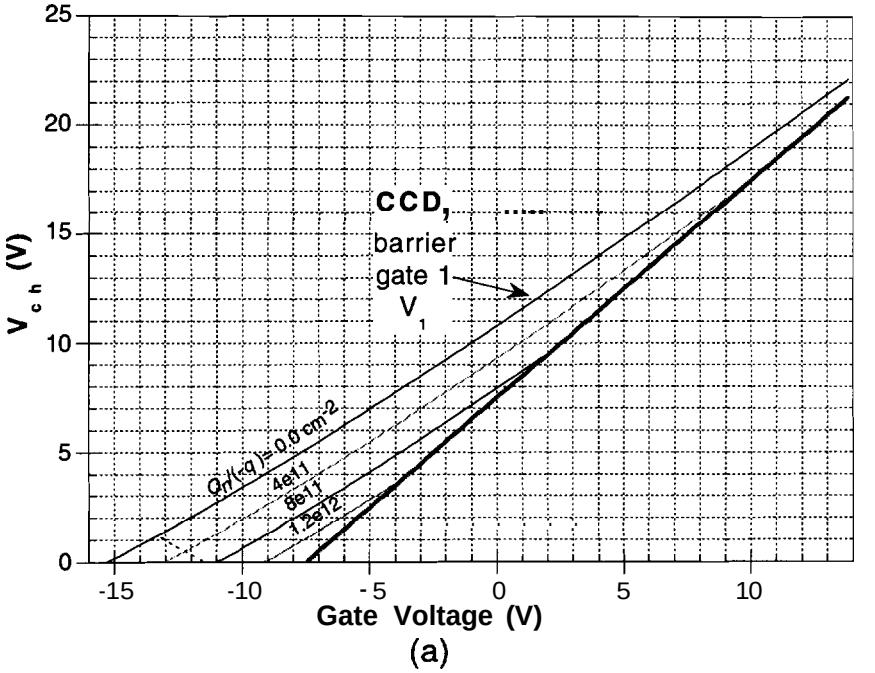
V_{OG} signal was triggered at f /4 and both the reset gate V_{RG} and reset voltage V_R were triggered at f 18. The high and low values for these waveforms were chosen with careful consideration of the operating domains of Fig. 4.18 (a) and (b), which were calculated using the parameters extracted in Section 4.3. For CCD_1 we have found: N_A =1.7x10^{16} cm^{-3}, N_D=1.6x10^{17} cm^{-3}, x_j=1830 Å, t_{ox1} =708 Å, V_{FB1} =-5 V, t_{ox2}=645 Å, and V_{FB2_n}=0.5 V.

The operation of the CTD is shown with the waveforms in Fig. 4.19. Electrode voltages V_1 and V_2 were held constant at -1 V and 8.5 V, respectively, such that the channel under V_1 did not receive charge and the storage region under V_2 was filled to its maximum capacity of 7.5x10^{11} cm^{-2} at a channel voltage of 10 V (see Fig. 4.18). At the point where V_{RG} is clocked back to -1V, the output voltage drops about 0.5 V due to capacitive coupling through the overlapping gate.

The output voltage drops from 9.6 V to 7.2 V when the charge is coupled back into the floating node, corresponding to a swing on the output node from 15.2 V to 10.4 V, or ΔV_{n+} =4.8 V. The total amount of charge transferred into the floating node as calculated from Fig. 4.17 is Q_N =-q (2.25x10^7) C, which is equivalent to a charge density of -q (1.12x10^{11}) C/cm^{-2}. Since this is only a fraction of the total charge residing under V_2, the storage region was not completely drained by the preset voltage (16.5 V). This simply means that the effective channel capacitance under V_2 is much larger than C_{out}.

A variation in the output voltage swing was achieved in this measurement by reducing the well depth in the channel under V_2. A set of output waveforms in Fig 4.20 demonstrate this effect. The same ΔV_o is observed for all V_2 biases above 6.5 V, but the signal changes dramatically as the channel voltage moves closer to 10 V (V_2=6.0 and 5.5 V). Finally, we see that no change in output voltage is observed (except for the same capacitive coupling) for V_2<5.0 V. This corresponds to a channel voltage that is less than 10 V, which is lower than the input pulse, meaning that no charge is stored.

A demonstration of charge sharing between the output node and the channel under V_{OG} is shown in Fig. 4.21. V_2 is set at <5 V, so as to not receive charge. The voltage change observed when V_{OG} "sloshes" charge corresponds to a charge in the n-channel of about Q_N =-q (1.14x10^7) C (or 2.85x10^{11} cm^{-2}) under the 20 x 200 µm output gate.



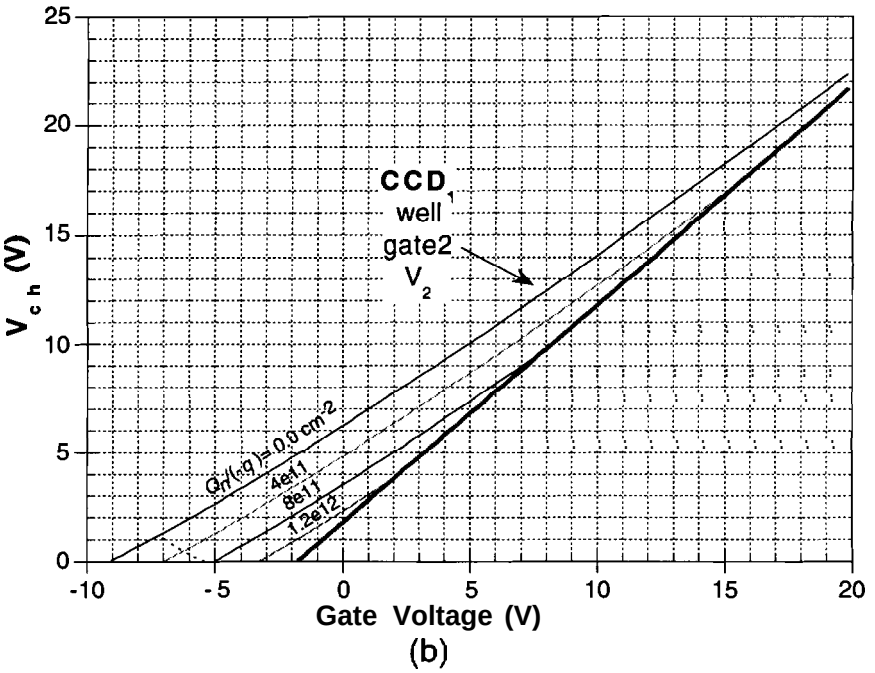


Figure 4.18

Operating domain plots for both gate levels on CCD_1. Relevant parameters were extracted mostly from CV measurements of the buried-channel GCD in Fig. 4.9: N_A =1.7x10^{16} cm^{-3}, N_D =1.6x10^{17} cm^{-3}, x_j =1830 Å, t_{ox1} =708 Å, V_{FB1} =-5 V, t_{ox2} =645 Å, and V_{FB2} =0.5 V.

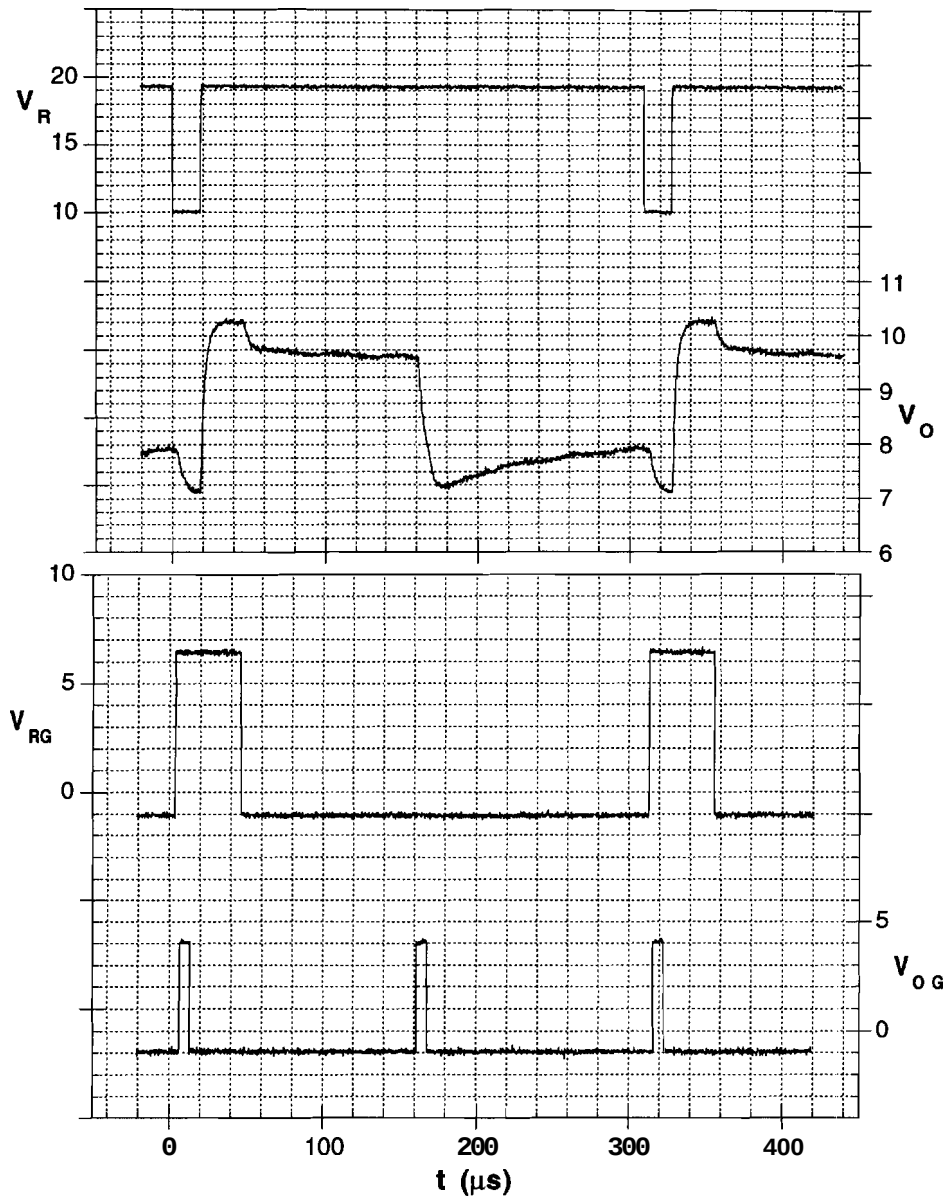


Figure 4.19

Demonstration of charge storage and transfer in a SiC buried-channel charge transfer device. The principle of this measurement is shown in Fig. 4.5.

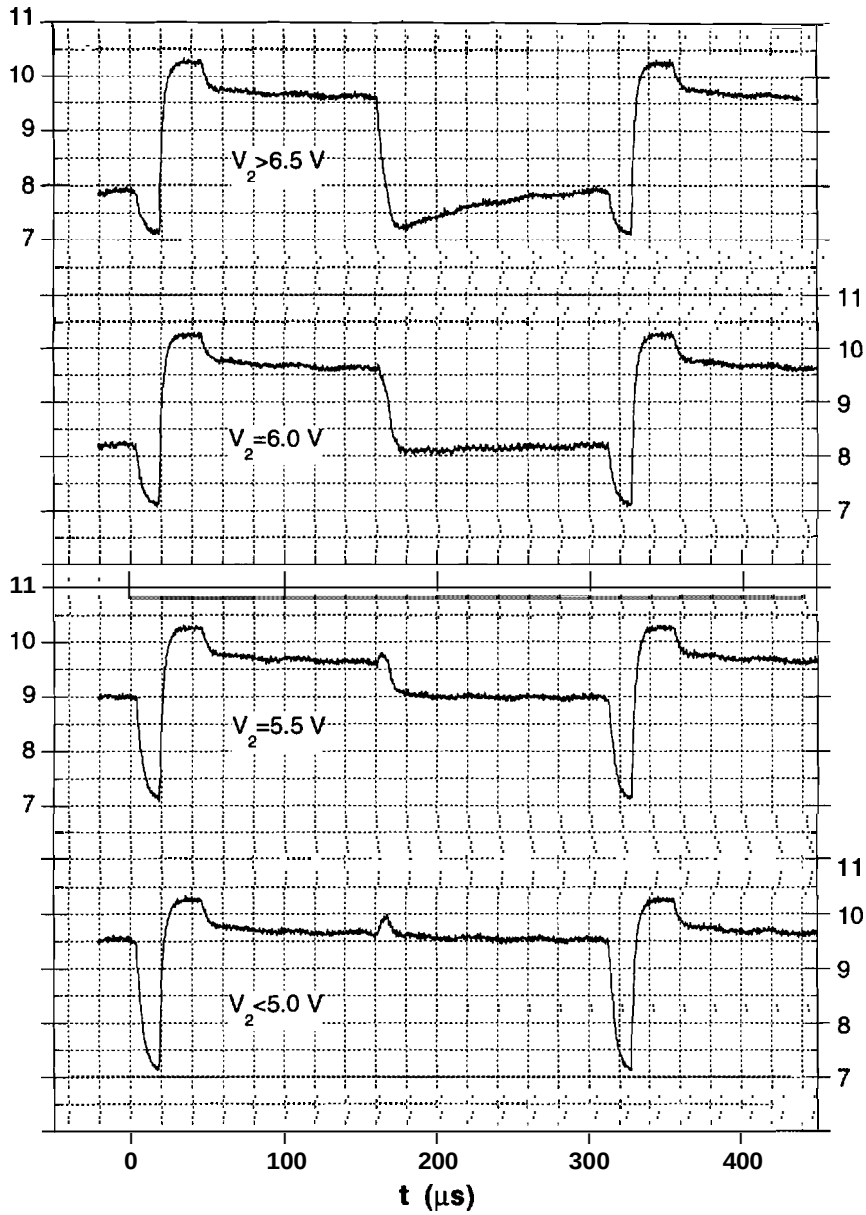


Figure 4.20

A variation in output voltage swing of the CTD measurement for several biases on the :storage node V2. The reset gate and output gate waveforms are exactly the same as in Fig. 4.19.

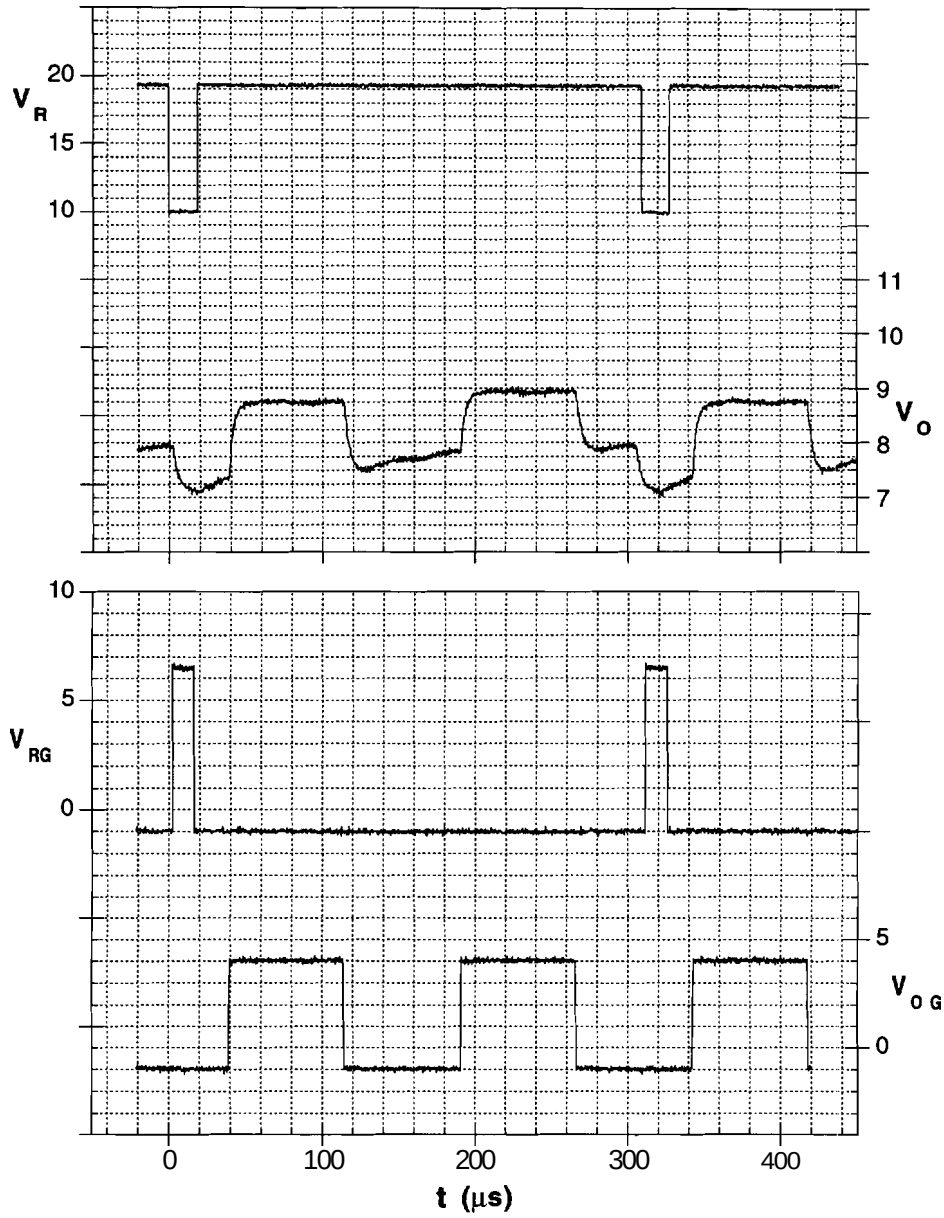


Figure 4.21

Demonstration of charge sharing between the output node and the channel under V_{OG}. V_2 is set at <5 V, so as to not receive charge. The voltage change observed when V_{OG} "sloshes" charge corresponds to a charge density in the n-channel of about 2.85×10^{11} cm^{-2}, assuming V_{OG} has an area of 20 x 208 pm.

4.5 CCD Operation

4.5.1 Experimental Method

The linear CCD designed for this experiment is a thirteen terminal device (Fig. 4.3), including substrate contact. In order to expedite device characterization, however, three of these terminals were connected to other parts of the CCD by on-chip metallization. At the expense of some flexibility in charge input and output techniques, the input, output, and reset gates were tied to Φ_1 and Φ_2 clocking voltages as shown in Fig. 4.22. This approach facilitated probe testing and avoided extra complications involved with die saw-apart, packaging, and bonding. Also, the number of required clock waveforms was reduced.

The choice of clocking voltages was based solely on the operating domain plots in Fig. 4.18. The waveform voltages are listed in Table 4.5 with the corresponding well and barrier channel voltages (note: we interchange the terms "channel potential" and "channel voltage" with $\phi = V + V_{bi}$). The expected charge packet size is q (5.4×10^{11}) C/cm^2, which is calculated by using Eq. (3.28) with gate level 2 biased at $V_{lo}+V_{dc}$. Recall for the maximum charge, the channel potential in the storage area is equilibrated with the empty well of an adjacent barrier as is depicted in Fig. 3.2 (b). Waveforms were supplied to the chip by three function generators configured as in the CTD measurement. The dc offset voltage was supplied for each phase by a simple voltage divider circuit.

Charge transfer was examined in three different frequency ranges. The highest frequency was conservatively chosen as 34.5 kHz in order to avoid being limited by the output amplifier. The reset voltage V_R had a strong influence on the precharge value of the floating node due to the leakage mechanism demonstrated in Section 4.4.2. So, the charge transfer to be described in the next section was measured for two different values of V_R to show its relevance.

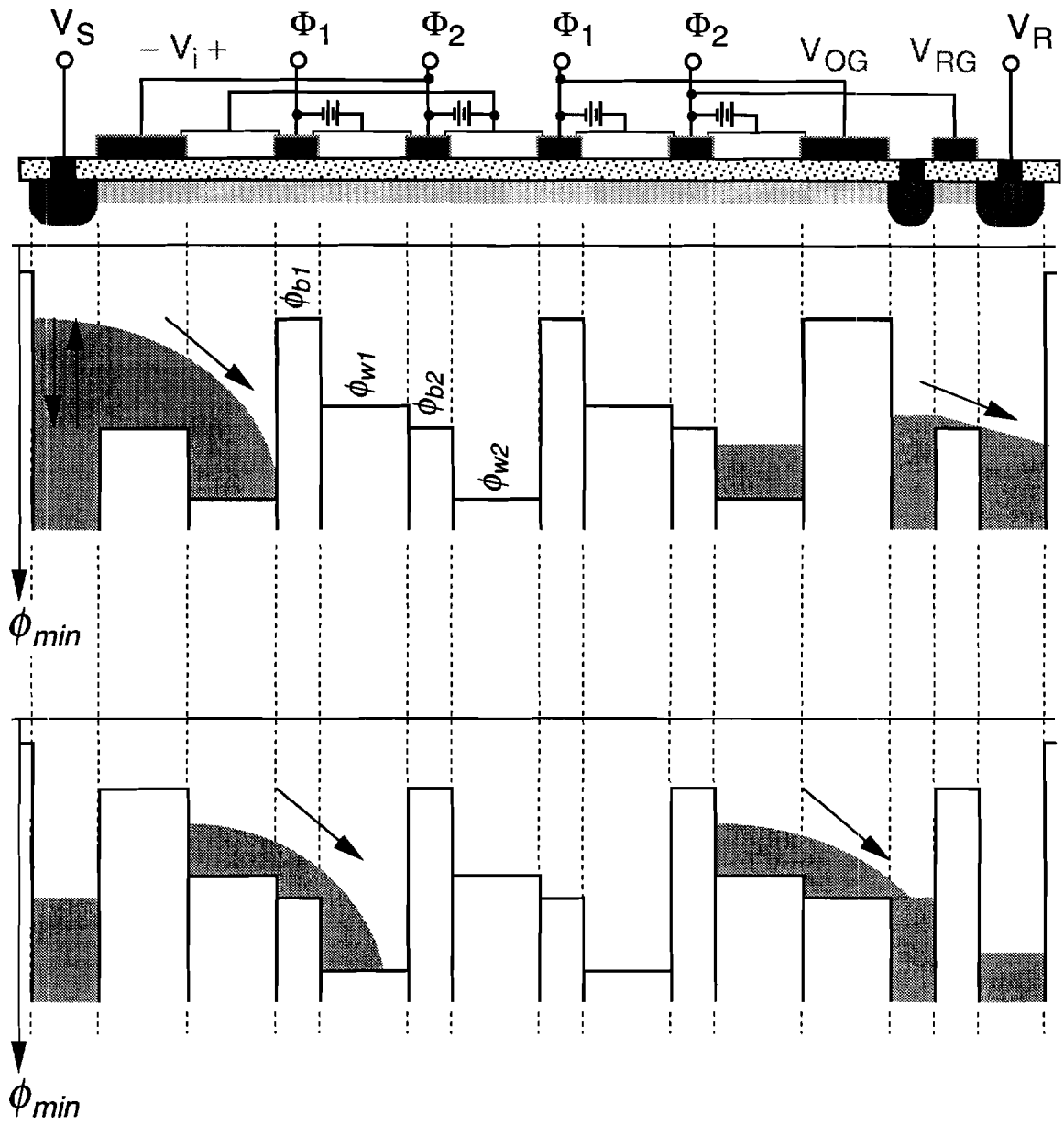


Figure 4.22

Configuration of the SiC linear CCD for characterization. The two input gates, the reset gate, and the output gate were tied to phases 1 and 2 as shown. Only a constant amount of charge can be injected with this configuration, and there is a possibility of charge sharing between the output node and the channel under V_{OG}.

Table 4.5

Summary of the clocking voltages used to drive the CCD (in volts). The numbers correspond to V_{lo}=0 V , V_{hi}=4 V, and V_{dc}=8.5 V, and the charge packet size! is $q(5.4x10^{11})$ C/cm^2. The corresponding well and barrier channel voltages are listed.

PHASE	V_b	V_w	$(\phi_b - V_{bi})$	$(\phi_w - V_{bi})$
sending	0	8.5	11	13
receiving	4	12.5	14	16

Two detrimental effects resulted from merging the input, output, and reset gates with the CCD phases. These drawbacks must be considered when interpreting the output signals of the device. First, since the input gates were wired as an additional CCD phase, the input voltage V_i was fixed at V_{dc}, and the size of the injected charge packet was constant; charge could either be injected or excluded, depending on the input bias. This is acceptable, however, for simple demonstration of charge transfer.

Second, proper interpretation of output voltage swing may be affected by charge sharing with the channel under the output gate. By wiring the reset gate to the Φ_2 clocking potential, the maximum potential to which the floating node can be precharged is the same as the adjacent well under V_{OG}. It is obvious from the diagram in Fig. 4.22 that output charge cannot be completely drawn out of the channel, meaning that the output voltage swing cannot reflect the proper magnitude of the signal charge.

The load resistor on the output amplifier was increased slightly to 51.8 kΩ for the CCD measurement. The measured transfer characteristic is shown in Fig. 4.22 with the capacitance and charge characteristics of the 30x108 μm output floating node. The stray capacitance was about 0.22 pF. This figure was used to graphically determine charge packet sizes directly from voltage swings observed in the measurement.

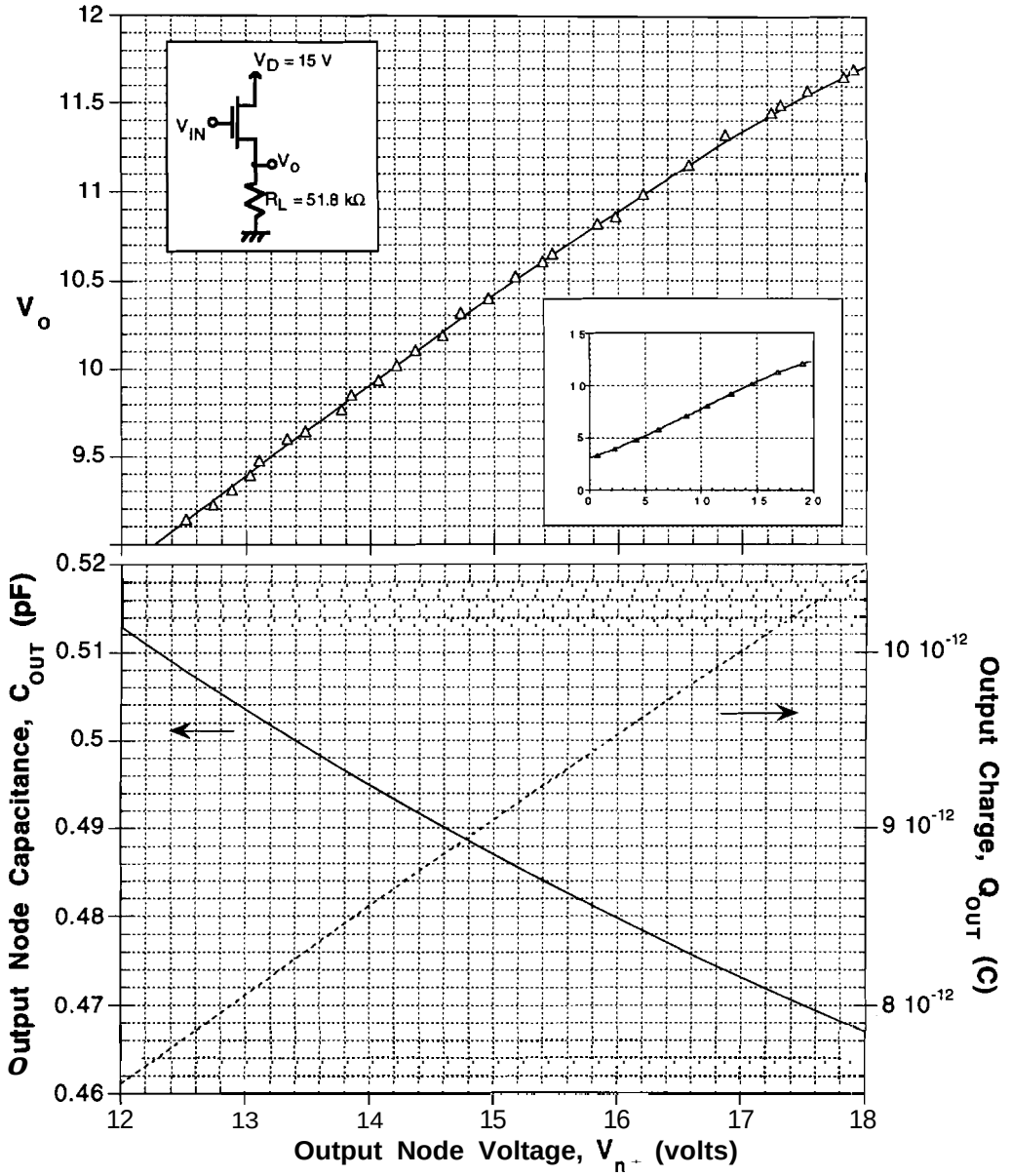


Figure 4.23

Transfer characteristic of the source follower amplifier at the output of the CCD_1. Variable capacitance and output charge of the floating n+ island at the CTD output. The stray capacitance C_W is about 0.22 pF, the diode area is 30 x 208 μm, and the p-side doping is 1.7×10^{16} cm^{-3}.

4.5.2 Results

A set of clocking waveforms and output voltage are shown in Fig. 4.24 for no injection at the CCD input. According to Table 4.5, the bias pulse should be less than 14 V in order to fill charge into the well of the first phase. The output voltage rests at 11 V, corresponding to the reset voltage of 16.5 V. The parasitic leakage at the reset transistor is strong enough to almost equilibrate V_{n+} with V_R.

Charge transfer becomes evident in Fig. 4.25 for an input pulse low enough to inject charge. The pulse width is only about 10 µs long and occurs entirely within a half clock cycle that Φ_2 is high, which is the only part of the cycle that the CCD should receive charge. The output response is very subtle, but it arrives after the proper number of clock cycles. For this device, there are 34 gates of the CCD proper, giving 17 phases and 8.5 stages for the pseudo-two phase configuration. Unfortunately, the magnitude of the delayed signal is much smaller than we might expect for a charge packet arriving at the 0.4 pF (roughly) floating node. This has to be explained by: (a) the width of the pulse is not long enough to "fill" charge completely into the CCD, or (b) leakage of charge back into the source when its voltage is returned to its rest value of 20 V.

If the pulse is maintained for more than half the clock cycle, a much larger signal is observed as seen in Fig. 4.26. Several charge packets arrive at the output in response to injecting charge for two clock cycles. The floating node is "charged" to a less positive potential by the two (or three) successive charge packets. For the injection of charge over four clock cycles in Fig. 4.27, five output pulses are seen. The charging seems to saturate somewhat at a minimum value around 10 V, corresponding to 14.2 V on the n^+ node. Note that V_{n+} is always more positive than the channel under V_{RG}, meaning that the floating node is never in communication with the reset diode through the n-channel. Rather, the parasitic leakage allows the output n^+ to drift back toward V_R on the half cycle that Φ_2 is high. This is in agreement with the current measurement previously shown in Fig. 4.13, where the residual current was strongly gate bias dependent.

Fig..4.27 shows that for a series of charge packets dumped onto the output, the first few are consumed in "charging" the node to a less positive potential. Therefore, the reset voltage was lowered to 15 V in order to reduce

the amount of charging necessary. The two output waveforms in Fig. 4.28 contrast the effect of the reset voltage, and show that the magnitude of the first charge packet is different for each condition. Again, we see charge output for more cycles than the input charge was available at the input, indicating a *charge smearing effect* [67]. The charge magnitude corresponding to the largest output voltage swing is about 3.86×10^6 electrons, which corresponds to a channel charge density of q (1.93×10^{11}) C/cm^2, assuming the storage region area as roughly equal to the size of the well electrode, 20 x 100 μm.

A representative output waveform for charge transfer at 17.2 kHz is shown in Fig. 4.29, where the input pulse is available for eight clock cycles. Charge smearing is present, but the output pulse magnitude does not saturate right away due to the probable feedback of signal charge into the well of the last CCD phase. After the third cycle, the charge magnitude is large enough to recluce the voltage on the output below 9.8 V. This breaches the channel voltage under the output gate, which is at about 14 V, and part of the signal charge is shared. Furthermore, part of the charge under the output gate can spill back into the CCD (and add to the next signal), when Φ_1 returns to it's low value. This is similar to the addition of superfluous charge at a CCD input in the *diode cut-off technique.*

Finally, the charge transfer is demonstrated for a step input over four clock cycles at 5.5 kHz in Fig. 4.30. Also, the reset voltage is at the higher value. Between transfers, the floating node leaks almost all the way to V_R before the arrival of the next clock transition. Comparing to the output waveform for 34.5 kHz in Fig. 4.28, we see the magnitudes of the leading charge packets are essentially the same. This may indicate that the behavior of charge transfer along the CCD is relatively the same over the frequency range we are able to probe, including charge smearing effects, but interpretation of the output pulse traiins depends heavily on the output configuration. Unfortunately, this provides a very inconsistent scenario to calculate and compare charge transfer efficiencies.

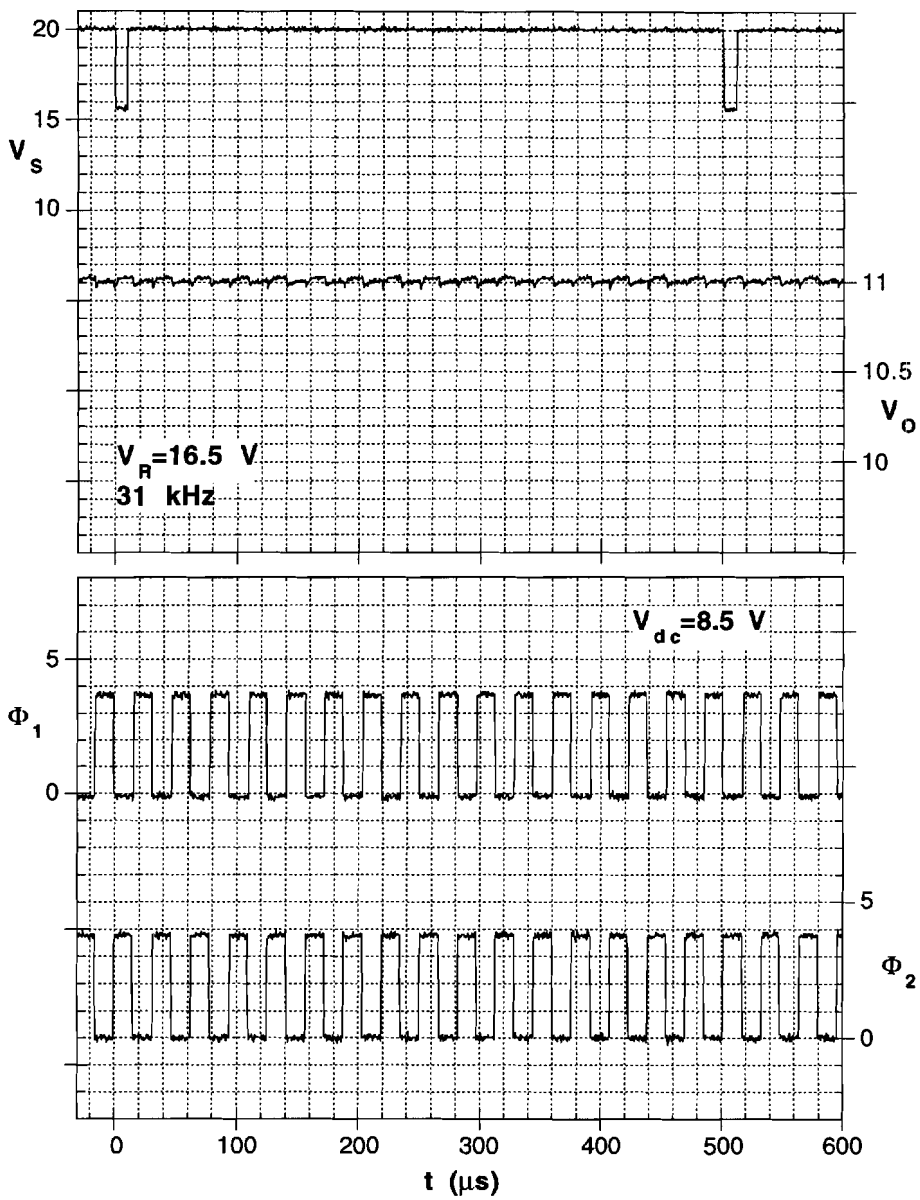


Figure 4.24

Sample waveform of CCD operation in the case of no charge injection. The clock frequency is 31 kHz, and the reset potential is 16.5 V.

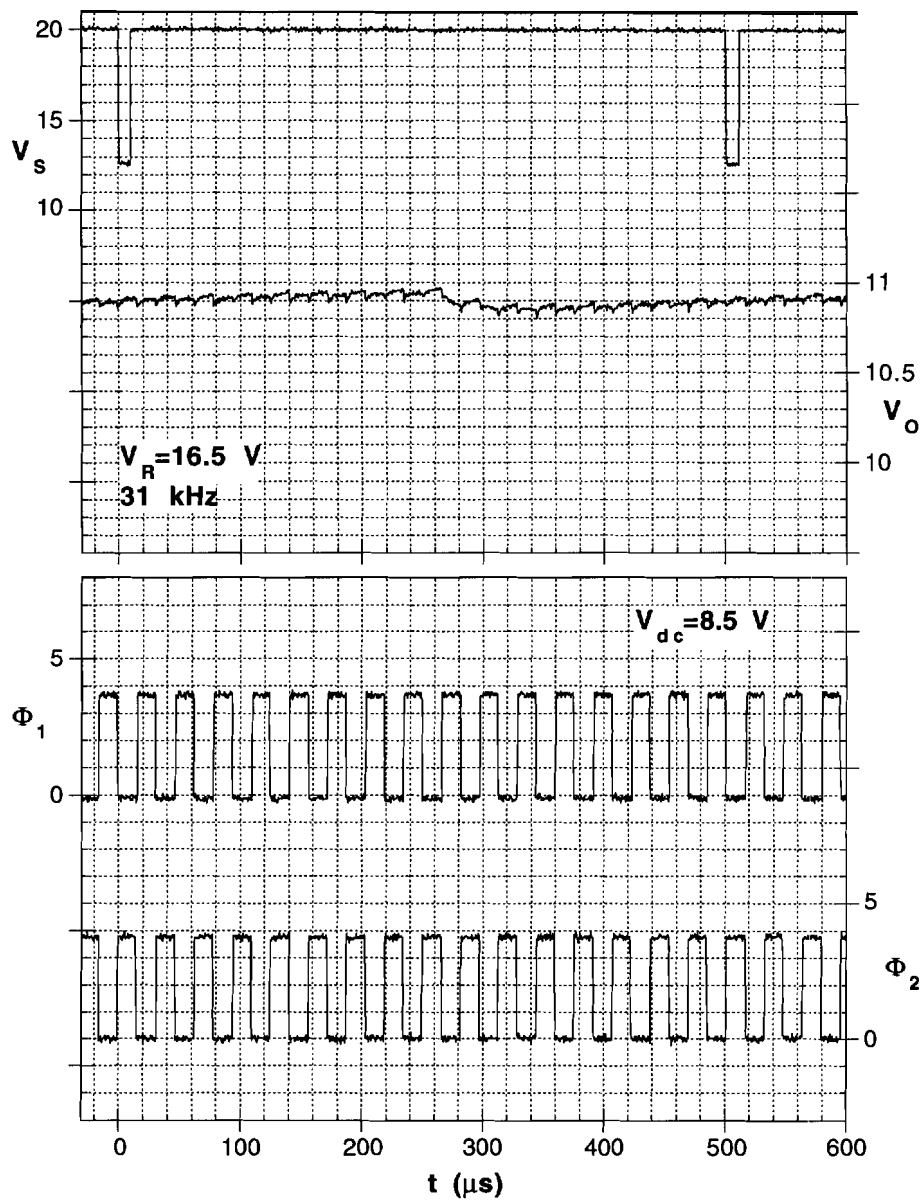


Figure 4.25

Demonstration of charge transfer in the CCD where the input charge is available for only one clock cycle. The clock frequency is 31 kHz, and the resel potential is 16.5 V. The response is very subtle, but arrives at the output after the proper number of cycles.

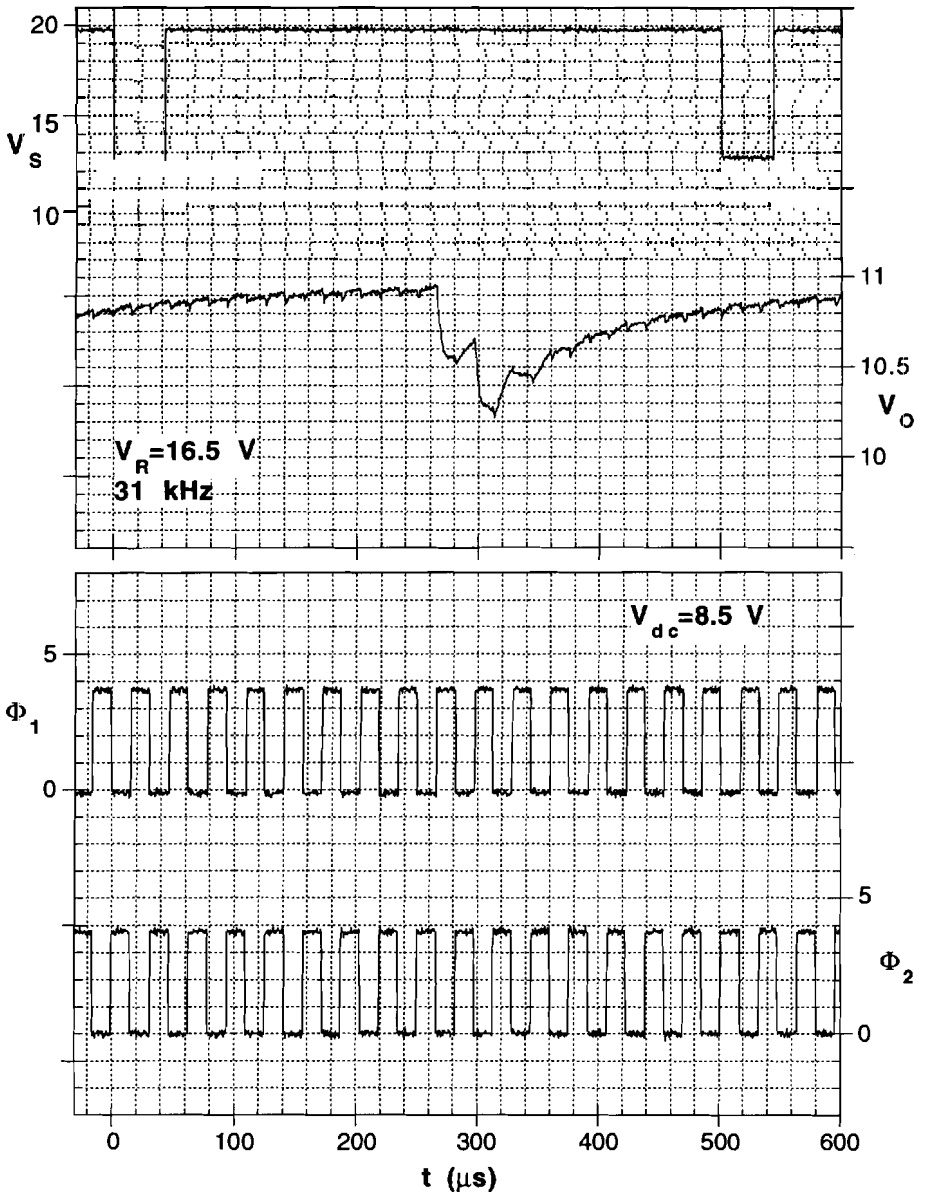


Figure 4.26

Charge transfer when the input charge is available for two clock cycles. The clock frequency is 31 kHz, and the reset potential is 16.5 V.

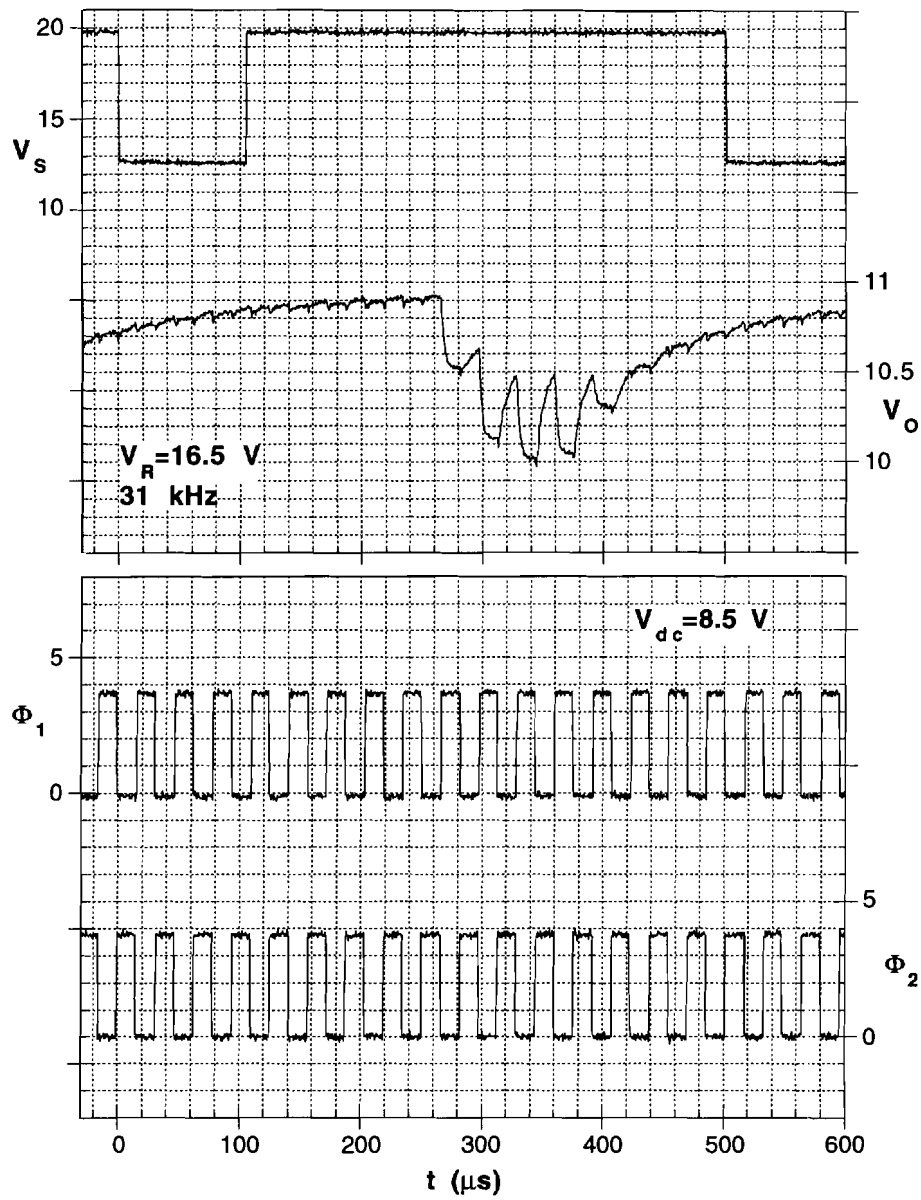


Figure 4.27

Charge transfer when the input charge is available for four clock cycles. The clock frequency is 31 kHz, and the reset potential is 16.5 V. The first two packets are "consumed" in charging up the floating node. An extra (5th) output pulse could be due to charge smearing effects along the CCD channel.

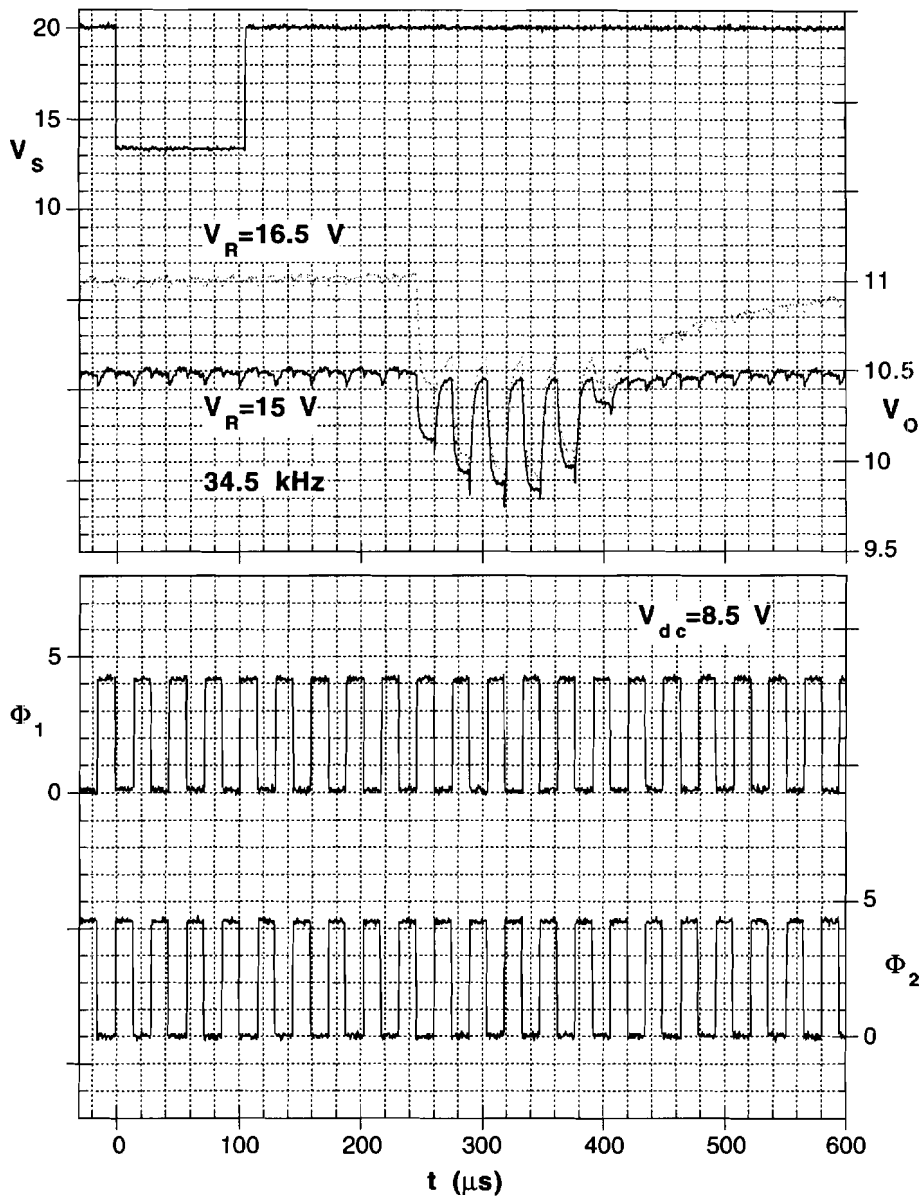


Figure 4.28

Comparison of CCD outputs for different reset voltages 15 V and 16.5 V.

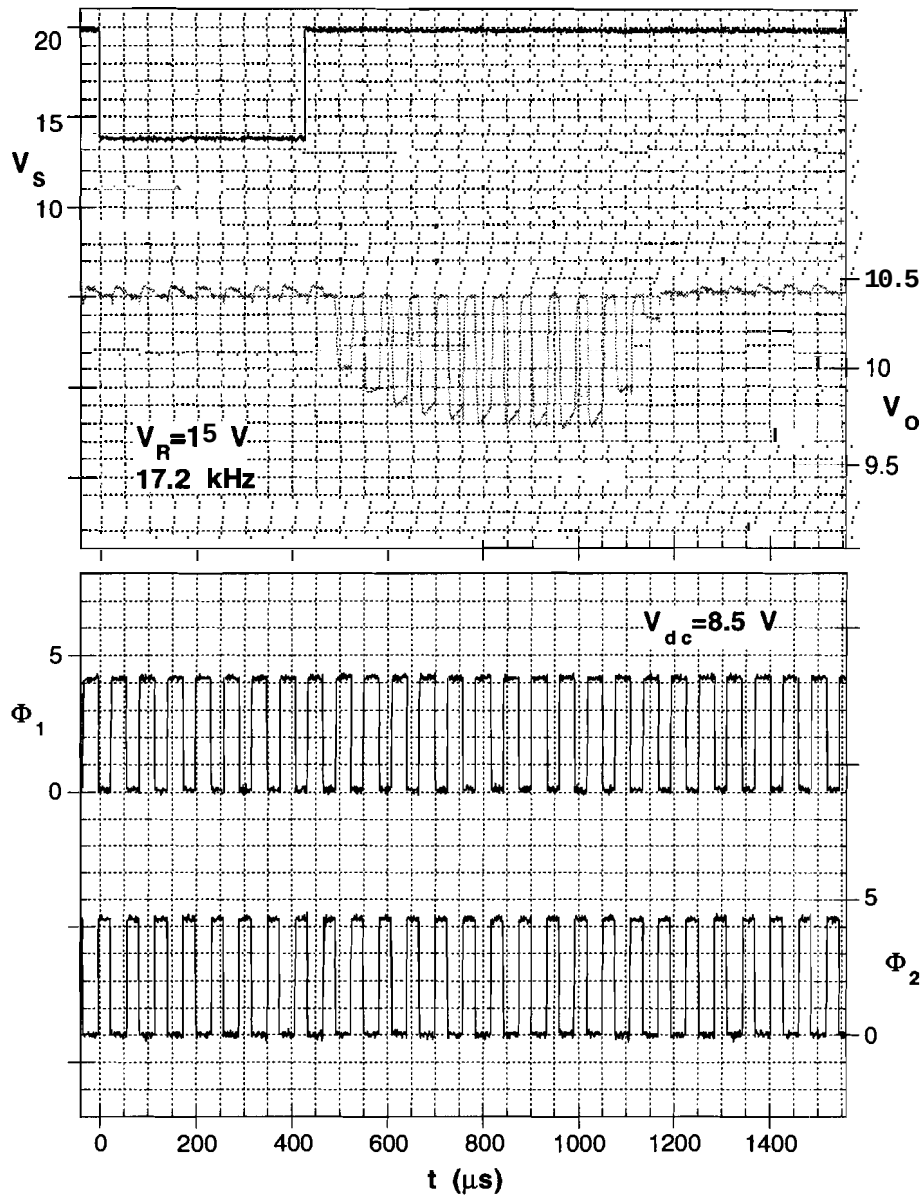


Figure 4.29

Output pulse train for input charge of 8 cycles. The frequency is 1'7.2 kHz.

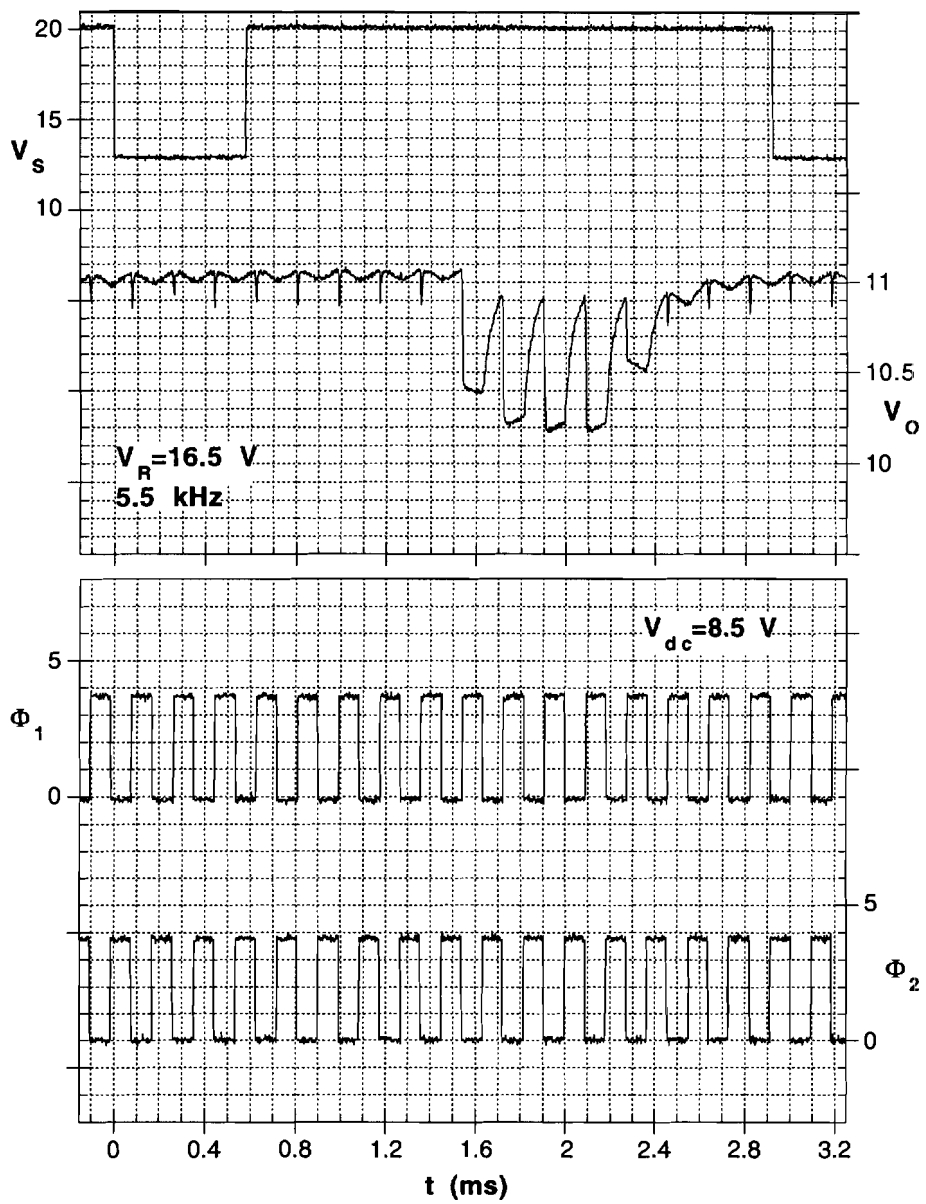


Figure 4.30

Demonstration of charge transfer at 5.5 kHz. The floating node leaks practically all the way to V_R during the long half-clock cycle that Φ_2 is high.

CHAPTER 5 - EPILOGUE

5.1 Recommendations for Future Work

The successful operation of the SiC buried-channel CCD in the last chapter shows great promise for further development of a UV imager. However, there are several issues that must be addressed in any future work with this device. A number of these topics are outlined below.

5.1.1 Fabrication Items

Most of the difficulties encountered with the CCD characterization are directly attributed to SiC process technology and can be especially related to the poor oxide-semiconductor characteristics encountered. Any 'further work involving SiC CCDs must have better MOS characteristics because the observed high surface state densities make any long-term or elevated-temperature stable operation unlikely. Information in Section 5.1.1.1 explains thalt improved oxides are possible on SiC and can be adapted to a double-level polysilicon process. Other pertinent issues regarding device isolation are mentioned in Section 5.1.1.2.

5.1.1.1 Improved SiC - SiO_2 interfaces

Monumental improvements in the quality of SiC-SiO_2 interfaces have been achieved recently [13]. Amicable surface state densities in the low 10^{11} $cm^{-2}eV^{-1}$ have been achieved on moderately doped p-type 6H-SiC, which is more than an order of magnitude improvement over the results reported in this thesis. Fixed charge values were also improved over previous results [109] to

0.9×10^{12} cm^{-2}. These ameliorated interface characteristics were achieved by using careful surface preparation and a special slow furnace loading technique. Typically, the oxidations were performed in "wet" oxygen at 1150 °C for 4-4.5 hours ancl then followed by 30 minute Ar anneal. Aluminum gated MOS-capacitors were used for all of these experiments.

These improved surface preparation and oxidation procedures were used during the CCD processing, so equally good oxide interface qualities had been expected. However, transferring the improved oxides to a polysilicon gate process posed some difficulty. After the poor results for the oxides reported in Chapter 4 were known, a side experiment was conducted to determine why 'the polysilicon gated devices had poor characteristics [110], and what procedures are necessary to improve them. The procedure and findings are summarized as follows.

Three moderately doped ($1\text{-}2 \times 10^{16}$ cm^{-3}) p-type SiC pieces were prepared and oxidized with the aforementioned optimum procedures. To avoid atmospheric contamination, two of the samples were immediately loaded from the oxidation furnace into a horizontal hot-wall low pressure chemical vapor deposition (LPCVD) reactor, and 4000 Å of polysilicon was deposited at 150 mtorr and 620 °C. Al was evaporated onto the third sample from a resistively heated alumina-lined tungsten boat.

Part of this experiment was to verify if the excessive 1050 °C dopant drive-in anneal was the cause of poor oxide characteristics on the CCDs (see App. I). Therefore, one of the polysilicon gated samples was stressed at 1050 °C for 10 minutes in argon immediately after the polysilicon deposition. Then, the polysilicon gated samples were doped using a phosphorus contamiinated spin-on insulator. The phosphorus was diffused into the poly-Si at 900 °C in a 25%/75% N_2/Ar ambient for 60 minutes. Finally, MOS capacitor gates were patterned on all three samples and appropriately etched with RIE in SF_6 or wet etching. The three oxides were characterized with high-frequency CV measurements at room temperature, where photoexcitation was used to populate interface states and determine rough N_{IT} values. The results are summarized in Table 5.1.

The poly-gated devices that were not stressed have virtually the same characteristics as the Al gate control sample. The results seen on the stressed poly-gatecl sample confirm that the characteristics reported on gate level 1 of

Table **5.1**

Interface characteristics from 6H-SiC MOS capacitors showing two significant results: (1) polysilicon gate devices can be made with the same quality interfaces achieved with Al gates, (2) higher temperatures used in the process after the polysilicon gate deposition cause degradation of the SiC - SiO_2 interface.

	Al Gate Control	Poly-Si Gate 900 °C doping	Poly-Si Gate 1050 °C stress 900 °C doping
Q_f (cm^{-2})	$8.4x10^{11}$	$9.7x10^{1}$	$2.2x10^{12}$
N_{IT} (cm^{-2})	$3.3x10^{11}$	$3.3x10^{11}$	$1.1x10^{12}$

the CCDs were due to the high temperature drive-in conditions. These are significant results for the CCD process, showing that excellent quality interfaces are possible under both gate levels as long as the processing temperatures are kept low subsequent to the deposition of polysilicon level 1.

A related experiment was conducted to determine if the irrrproved MOS characteristics could be maintained through further processing steps that are necessary to complete a SiC MOSFET. Transistors were fabricated with the basic MOSFET process used in Section 2.2.1, including n^+ source/drain implantation, 1500 °C activation anneal in argon, nickel source/drain contacts, platinum backside contact, 925 °C contact anneal in nitrogen, and gate oxide and polysilicon gates processed with the optimized conditions above. The results were unmistakably positive. Along with interface characteristics similar to those in column 2 of Table 5.1, the inversion channel mobility was measured at 41 cm^2/Vs on these carefully processed devices, which is a twofold improvement over previously reported results in Section 2.2.1.2 [84]. Therefore, the outlook is good for building another buried-channel CCD with agreeable insulator and interface attributes.

It is unclear from these experiments at what temperature between 900 and 1050 °C does the degradation become significant. Further studies in this area can be important to the development of a self-aligned technology in SiC.

5.1.1.2 Elin- ina at ion of parasitic transistor leakage current

Obviously, the other most important problem to be addressed is the leakage current observed on the transistors of the CCD samples (Sect. 4.4.2). Not only did it make interpretation of the output waveforms more difficult, but this type of leakage can also contribute to crosstalk amongst the potential wells along the CCD. Whether this extraneous current can be attributed to (a) strong surface inversion in the area around the device or (b) to parasitic inversion-channel transistor action in the small n-channel edge region, it is a problem of device isolation. In silicon monolithic circuit technology, deep-diffused p^+ channel stop areas are used to prevent communication between isolated n^+ islands. Formation of a heavily doped p^+ chan-stop in SiC must be achieved by ion implantation. Unfortunately, electrical activation of implanted acceptors (Al, B) in SiC has proved to be spurious [111], [112], [113]. Some attempts at using heavy Al implants have been successful [114], but not consistently. This technology may require more development.

5.1.2 Device Design Issues

5.1.2.1 Signal "breakthrough" at floating node outputs

The problem of capacitive coupling of the floating node to either V_{RG} or V_{OG} clocking signals was experienced during CTD and CCD measurements. In retrospect, this problem could have been eliminated by placing an extra DC-biased gate between the floating node and the reset gate. The output gate is actually supposed to perform this shielding function against signal breakthrough from the last phase in the CCD, but the choice to measure the CCD under probe test (with the minimum number of connections) precluded the use of V_{OG} in this manner.

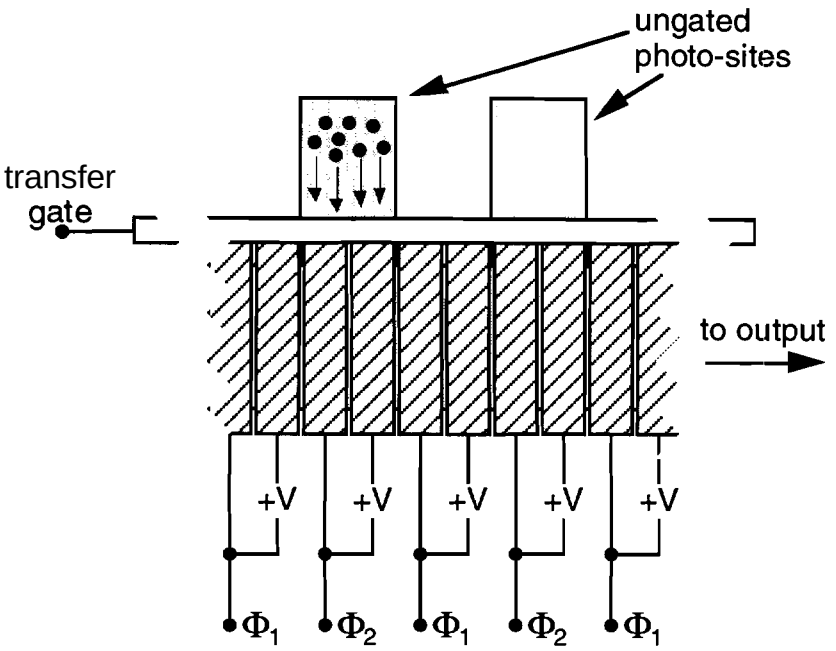


Figure 5.1

Structure suitable for linear UV imaging. The photo-sites are charge-induced field regions as described in Section 1.3. Photogenerated electrons are collected under one of the CCD phases and shifted to an output circuit.

5.1.2.2 Integration of **UV** photosensors with CCD readout

The schematic diagram in Fig. **5.1** represents a linear array of **UV** sensitive photo-sites (only two elements are shown) with an adjacent pseudo two-phase CCD for readout. This seems to be the most practical arrangement for the SiC imager in its next stage of development. During the integration period, the transfer gate is biased high, and the signal charge is collected under phase **2** in the CCD. Note that the phases are not being clocked at this time, but are held constant with $\Phi_2 > \Phi_1$. When the signal packets are being shifted to the output, the transfer gate is biased to disconnect the photo-sites from the CCD phases. Since most gate materials absorb wavelengths below 400 nm, **UV** light falling on the device during readout cannot distort or smear the signal. However, the entire area of the device (except for the integration areas) should be shielded from light with a metal cap layer. This can prevent any unwanted photogeneration of carriers at critical spots. For example, below bandgap light

should be precluded from the CCD shift register area to prevent photo-population of interface states.

The problem remains of how to integrate the ungated photodiode described in Section 1.3 with the implanted-channel CCD. Essentially, the part of the imager circuit containing the shift register has to have an insulator with optimal qualities, while the adjacent photosensitive "pixels" require oxides with large amounts of fixed charge in order to have a "charge-induced" electric field at the surface.

It may be possible using the information we have found on thermal stress of polysilicon-covered oxides, which was discussed previously in this chapter. The results suggest that an extra polysilicon layer can be used to selectively make a "crummy" oxide over the pixel areas, which is needed for the idea of "charge-induced photocollection" introduced in Chapter 1. This extra poly-level would be inserted into the process before level 5 (Table 4.1), patterned, and etched to define the area of the UV photosensors. Before proceeding, the wafer could be subjected to a short, high-temperature (1150 °C) oxidation, that would damage only the selected areas. After the rest of the process, the dumrny polysilicon can be etched away to form the ungated photosensor. This is, of course, a very general idea, and much investigation is needed to deterrnine if it is viable.

5.2 Conclusion

The work detailed in this thesis has laid the groundwork for further development of a UV imager in silicon carbide. Successful demonstratiion of charge transfer was achieved in a buried-channel CCD, despite many problems imposed by non-optimal fabrication steps. Process technologies for SiC are being improved at impressive rates and can contribute to future success of such a compliciated MOS device, especially recent breakthroughs in thermal oxidation techniques.

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APPENDIX I - BCCD RUN SHEET

Table A1.1

Outline of the BCCD fabrication process at the mask level. All mask polarities are listed for use of positive photoresist.

	Fabrication Step	Mask Polarity	Process
1	Registration Etch	darkfield	Al Wet Etch and SiC RIE
2	S/D Implant Mask	lightfield	Ti/Au Liftoff
3	Channel Implant Mask	lightfield	Ti/Au Liftoff
4	GOX Area definition	darkfield	Poly-silicon Dry Etch
5	Gate Level 1 definition	lightfield	Poly-silicon Wet or Dry Etch
6	Gate Level 2 definition	lightfield	Poly-silicon Wet or Dry Etch
7	S/D Contact Window	darkfield	SiO_2 Wet Etch and Ni Liftoff
8	Dielectric, Via	darkfield	SiO_2 Wet Etch and Al Liftoff
9	Top Level Interconnect	lightfield	Al Etch

INITIAL MATERIAL CLEAN: samples cleaned of packaging contamination.

1.) SOLVENT CLEAN: use designated non-oxidation solvent beaker.
5 minutes each: acetone, TCA, acetone, and methanol. DIW rinse*. N_2 dry.
Also, clean the tweezers and a pyrex Petri dish for handling of the 'clean" sample.

2.) PIRANHA CLEAN: use designated non-oxidation H_2SO_4 beaker.
10 minutes in $1H_2O_2$:$1H_2SO_4$. DIW rinse*. N_2 dry.

3.) PIRANHA CLEAN: see step (2).

LEVEL 1: ETCH REGISTRATION MARKS

4.) PRE-OXIDATION CLEAN: use designated "oxidation clean" beakers.
SOLVENT CLEAN (see step 1)
PIRANHA CLEAN (see step 2)
BHF OXIDE ETCH: 10 minutes in BHF. DIW rinse*. N_2 dry.

5.) OXIDATION: wet O_2, 1150 °C, 30 minutes; should yield about 200 Å.

6.) Al EVAPORATION: NRC evaporator, 5V tap, Al_2O_3-W boat, three 0.5 cm bars of Al. Clean boat, Al, and electrodes in solvents before loading.

7.) PRE-BAKE: 15 minutes @ 120 °C (inside the covered Petri dish). Cool to RT.

8.) HMDS TREATMENT: Place samples in uncovered Petri dish into the dessicator containing the HMDS. Evacuate and wait 2-3 minutes before venting.

9.) APPLY POSITIVE PHOTORESIST: Shipley 1350JSF, 5500 RPM, 30 seconds.

10.) POST-BAKE: 12-15 minutes @ 85-90 °C (inside the covered Petri diish). Cool to RT.

11.) ALIGN and EXPOSE, LEVEL 1: KSMJB3, High Precision, 7.5 seconds, 23 mW/cm^2.

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* Flush with deionized water and decant at least 10 times. Soak for 1 minute. Flush and dry.

12.) DEVELOP PHOTORESIST: Mix 5:1 DIW:AZ351 developer. Stir!
Dip sample for 15 seconds. Rinse under flowing DIW for 1 minute. N_2 dry. Inspect.

13.) HARDBAKE: 15 minutes @ 120 °C (inside the covered Petri dish). Cool to RT.

14.) Al ETCH: Premixed $100H_3PO_4$:$100H_2C_4O_2$:$25HNO_3$:25DIW. Etch sample at RT.
Shine light through the sample to know when Al is etched. DIW rinse*. N_2 dry. Inspect.

15). STRIP PHOTORESIST: Soak in ACE, 2 minutes. Repeat.
Rinse in methanol 2 minutes. DIW rinse*. N_2 dry.

16.) DRY ETCH SiC: PlasMa Technobgy RIE, (0.26)x10 sccm SF_6, 100 W, 100 mTorr,
10 minutes. The low pressure causes more uniform etching with no micromasking!

17.) REMOVE Al & OXIDE: Use a Teflon beaker designated for stripping metals.
Soak in 1HF:1HNO_3, 10 minutes. DIW rinse*. N_2 dry. Inspect. Repeat, if necessary.

LEVEL 2: SOURCE/DRAIN SELECTIVE IMPLANTATIONi

18.) PRE-OXIDATION CLEAN: use designated 'oxidation clean" beakers.
SOLVENT CLEAN (see step 1)
PIRANHA CLEAN (see step 2)
BHF OXIDE ETCH: 10 minutes in BHF. DIW rinse*. N_2 dry.

19.) OXIDATION: wet 02,1150 °C, 60 minutes; should yield about 300 Å.

20.) PRE-BAKE: 15 minutes @ 120 °C (inside the covered Petri dish). Cool to RT.

21.) HMDS TREATMENT: Place samples in uncovered Petri dish into the dessicator containing the HMDS. Evacuate and wait 2-3 minutes before venting.

22.) APPLY POSITIVE PHOTORESIST: Shipley 1350JSF, 5500 RPM, 30 seconds.

23.) POST-BAKE: 12-15 minutes @ 85-90 °C (inside the covered Petri dish). Cool to RT.

24.) ALIGN and EXPOSE, LEVEL 2: KSMJB3, High Precision, 6.5 seconds, 23 mW/cm^2.

25.) CHLOROBENZENE SOAK: Soak each sample in chlorobenzene for 15-17 minutes.
Remove and promptly blow dry. DO NOT RINSE SAMPLE WITH DIW !!

26.) DEVELOP PHOTORESIST: Mix 5:1 DIW:AZ351 developer. Stir!
Dip sample for 20-25 seconds. Rinse under flowing DIW for 1 minute. N_2 dry. Inspect.
DO NOT HARDBAKE A LIFTOFF PATTERN.

7 . Ti/Au EVAPORATION: Varian e-beam evaporator, 2E-7 Torr, 1000 Å Ti + 3000 Å Au.
Perform the evaporation in steps to keep the pressure < 5E-6 Torr.

8 .) LIFTOFF: Soak samples in ACE. Squirt ACE to remove unwanted metal.
Rinse under flowing DIW for 1 minute. N_2 dry. Inspect. If unsuccessful, immerse sample into a beaker of ACE that is being agitated in the ultrasonic cleaner.

9 .) ION IMPLANTATION, N+ SOURCE/DRAIN: Leonard Kroko§ , nitrogen specie, 650 °C.
Calculate a multiple energy/dose schedule for a rectangular profile.

0 . METAL MASK REMOVAL: use a designated Tefbn beaker for etching metals.
Soak in aqua regia, 1HCl:1HNO_3, 10 minutes. DIW rinse*. Leave sample in beaker.
Soak in piranha, 1H_2O_2:H_2SO_4, 10 minutes. DIW rinse*. Leave sample in beaker.

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* Flush with deionized water and decant at least 10 times. Soak for 1 minute. Flush and dry.
i A polysilicon implant mask can also be used.
§ Tustin, CA.

31.) POST IMPLANT SURFACE CLEAN: use a designated Teflon beaker for etching metals.
Soak in 1HF:1HNO_3, 10 minutes. DIW rinse*. Repeat rinse. N_2 dry.
Inspect - do not proceed until the whole sample has been cleared of residual metal.

LEVEL 3: BURIED NCHANNEL SELECTIVE IMPLANTATION AND IMPLANT ACTIVATION ANNEAL

32.) PRE-OXIDATION CLEAN: use designated "oxidation clean" beakers..
SOLVENT CLEAN (see step 1)
PIRANHA CLEAN (see step 2)
BHF OXIDE ETCH: 10 minutes in BHF. DIW rinse*. N_2 dry.

33.) OXIDATION: wet O_2, 1150 °C, 60 minutes; should yield about 300 Å.

34.) PRE-BAKE: 15 minutes @ 120 °C (inside the covered Petri dish). Cool to RT.

35.) HMDS TREATMENT: Place samples in uncovered Petri dish into the dessicator containing the HMDS. Evacuate and wait 2-3 minutes before venting.

36.) APPLY POSITIVE PHOTORESIST: Shipley 1350JSF, 5500 RPM, 30 seconds.

37.) POST-BAKE: 12-15 minutes @ 85-90 °C (inside the covered Petri dish). Cool to RT

38.) ALIGN and EXPOSE, LEVEL 3: KSMJB3, High Precision, 6.5 seconds, 23 mW/cm^2.

39.) CHLOROBENZENE SOAK: Soak each sample in chlorobenzene for 15-17 minutes.
Remove and promptly bbw dry. DO NOT RINSE SAMPLE WITH DIW !!

40.) DEVELOP PHOTORESIST: Mix 5:1 DIW:AZ351 developer. Stir!
Dip sample for 20-25 seconds. Rinse under flowing DIW for 1 minute. N_2 dry. Inspect.
DO NOT HARDBAKE A LIFTOFF PATTERN.

41.) Ti/Au EVAPORATION: Varian e-beam evaporator, 2E-7 Torn, 1000 Å Ti + 3000 Å Au.
Perform the evaporation in steps to keep the pressure < 5E-6 Torn.

42.) LIFTOFF: Soak samples in ACE. Squirt ACE to remove unwanted metal.
Rinse under flowing DIW for 1 minute. N_2 dry. Inspect. If unsuccessful, immerse sample into a beaker of ACE, which is being agitated in the ultrasonic cleaner.

43.) ION IMPLANTATION, N-CHANNEL: Leonard Kroko§, nitrogen specie, 650 °C.
Calculate a multiple energy/dose schedule for a rectangular profile.

44.) METAL MASK REMOVAL: use a designated Teflon beaker for etchirg metals.
Soak in aqua regia, 1HCl:1HNO_3, 10 minutes. DIW rinse*. Leave sample in beaker.
Soak in piranha, 1H_2O_2:H_2SO_4, 10 minutes. DIW rinse*. Leave sample in beaker.

45.) POST IMPLANT SURFACE CLEAN: use a designated Teflon beaker for etching metals.
Soak in 1HF:1HNO_3, 10 minutes. DIW rinse*. Repeat rinse. N_2 dry.
Inspect - do not proceed until the whole sample has been cleared of residual metal.

46.) IMPLANT ACTIVATION ANNEAL: Lindberg Tube Furnace, 1500 °C, 12 minutes.
Load into boat at end of furnace under a high Ar flow @ 900 °C. Flush for 10 minutes.
Push into center of heat zone, taking 4-5 minutes.
Ramp to 1500 °C @ 20 °C/minute. Wait 12 minutes. Ramp to 900 °C @ 20 °C/minute.
Pull to end of furnace, taking 4-5 minutes. Cool for 10 minutes. Unload. Inspect.

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* Flush with deionized water and decant at least 10 times. Soak for 1 minute. Flush and dry.
§ Tustin, CA.

47.) POST ACTIVATION CLEAN: use a designated Teflon beaker for etching metals.
Soak in 1HF:1HNO3, 10 minutes. DIW rinse*. Repeat rinse. N_2 dry.
Inspect - repeat if necessary.

LEVEL 4: ACTIVE AREA DEFINITION IN FIELD OXIDE

48.) PRE-OXIDATION CLEAN: use designated 'oxidation clean" beakers.
SOLVENT CLEAN (see step 1)
PIRANHA CLEAN (see step 2)
BHF OXIDE ETCH: 10 minutes in BHF. DIW rinse*. N_2 dry.

49.) RCA PRE-OXIDATION CLEAN: use designated "RCA clean" beakers.

50.) OXIDATION, FIELD OXIDE BASE: wet 02,1150 °C, 60 minutes; 30 minutes Ar anneal.
Slow load* . Wet 02,1150 °C, 60 minutes. 30 minutes Ar anneal. Slow pull* .

51.) LPCVD POLYSILICON FOR FIELD OXIDE: proceed immediately from (50).
Deposit 2000-2500 Å of polysilicon, to be oxidized later to form the FOX.

52.) PRE-BAKE: 15 minutes @ 120 °C (inside the covered Petri dish). Cool to RT.

53.) HMDS TREATMENT: Place samples in uncovered Petri dish into the dessicator containing the HMDS. Evacuate and wait 2-3 minutes before venting.

54.) APPLY POSITIVE PHOTORESIST: Shipley 1350JSF, 5500 RPM, 30 seconds.

55.) POST-BAKE: 12-15 minutes @ 85-90 °C (inside the covered Petri dish). Cool to RT.

56.) ALIGN and EXPOSE, LEVEL 4: KSMJB3, High Precision, 7.5 seconds, 23 mW/cm^2.

57.) DEVELOP PHOTORESIST: Mix 5:1 DIW:AZ351 developer. Stir!
Dip sample for 15 seconds. Rinse under flowing DIW for 1 minute. N_2 dry. Inspect.

58.) HARDBAKE: 15 minutes @ 120 °C (inside the covered Petri dish). Cool to RT.

59.) DRY ETCH POLYSILICON: PlasMa Technology RIE, (0.26)x10 sccm SF_6, 30 W, 320 mTorr. Turn power up to 30 W over 20 seconds, then etch for 20 seconds.

60.) OXIDE ETCH: remove the underlying oxide in the windows of polysilicon.
Etch in BHF 60 seconds. DIW rinse . N_2 dry. Inspect.

61.) STRIP PHOTORESIST: Soak in ACE, 2 minutes. Repeat.
Rinse in methanol 2 minutes. DIW rinse*. N_2 dry.

LEVEL 5: GATE OXIDATION AND FIRST LEVEL GATE DEFINITION

62.) PRE-OXIDATION CLEAN: use designated 'oxidation clean" beakers.
SOLVENT CLEAN (see step 1)
PIRANHA CLEAN (see step 2)
BHF OXIDE ETCH: 10 minutes in BHF. DIW rinse*. N_2 dry.

63.) RCA PRE-OXIDATION CLEAN: use designated 'RCA clean" beakers,.

64.) OXIDATION, GATE OXIDE: wet 02,1150 °C, 300 minutes; 30 minutes Ar anneal.
Slow load* . Wet 02, 1150 °C, 300 minutes. 30 minutes Ar anneal. Slow pull* .

---

* Load at 800 °C in dry O_2; switch to wet O_2; after 15 minutes, ramp to temperature @ -15 °C/min.
Ramp to 800 °C in Ar @ -10 °C/min; use about 4-5 minutes to pull the sample out to RT.
• Flush with deionized water and decant at least 10 times. Soak for 1 minute. Flush and dry.

65.) LPCVD POLYSILICON GATES: proceed immediately from (64).
Deposit 4500-5000 Å of polysilicon for the first level gate electrode.

66.) APPLY SPIN-ON DOPANT: Filmtronics As-353 SOD, thaw to RT before using.
A special Teflon chuck and Petri dish must be cleaned 2x with piranha before starting.
Begin to heat the very clean Petri dish on a hot-plate to about 150 °C.
PIRANHA CLEAN SAMPLES (see step 2): grows a native oxide on poly surface.
Samples must be stored in a very clean Petri dish after this step.
SPIN: Attach very clean Teflon chuck to existing chuck. Spin 3000 RPM, 15 seconds.
CURE: Place sample into the Petri dish on the hot plate for 5-10 minutes.

67.) DRIVE-IN DOPANT: Use the furnace designated for dopant drive-in.
For 5000 Å poly-Si, drive at 1050 °C for 60 minutes in a 25% O_2, 75% N_2 ambient.
Use very slow push and pull times of about 3-4 minutes each.

68.) OXIDE ETCH, REMOVE SOD: remove the SOD from the surface of polysilicon.
Etch in BHF 2-3 minutes. DIW rinse*. N_2 dry. Inspect.

70.) PRE-BAKE: 15 minutes @ 120 °C (inside the covered Petri dish). Cool to RT.

7'1.) HMDS TREATMENT: Place samples in uncovered Petri dish into the dessicator containing the HMDS. Evacuate and wait 2-3 minutes before venting.

72.) APPLY POSITIVE PHOTORESIST: Shipley 1350JSF, 5500 RPM, 30 seconds.

73.) POST-BAKE: 12-15 minutes @ 85-90 °C (inside the covered Petri dish). Cool to RT

74.) ALIGN and EXPOSE, LEVEL 5: KSMJB3, High Precision, 6.5 seconds, 23 mW/cm^2.

75.) DEVELOP PHOTORESIST: Mix 5:1 DIW:AZ351 developer. Stir!
Dip sample for 15 seconds. Rinse under flowing DIW for 1 minute. N_2 dry. Inspect.

76.) HARDBAKE: 15 minutes @ 120 °C (inside the covered Petri dish). Cool to RT.

77.) DRY ETCH POLYSILICON: PlasMa Technology RIE, (0.26)x10 sccm SF_6, 30 W, 320 mTorr. Turn power up to 30 W over 20 seconds, then etch for 20 seconds.

OR

WET ETCH POLYSILICON: Premixed 50HNO_3:40DIW:3HF. Use magnetic stirrer.
Holding the sample with Teflon tweezers, dip into briskly stirring etchant for 15-20s.
Rinse under flowing DIW for 1 minute. N_2 dry. Inspect. Negative PR also works well.
Etch rates: 350-430 Å/s for poly-Si, 310 Å/min for SiO_2.

78.) STRIP PHOTORESIST: Soak in ACE, 2 minutes. Repeat.
Rinse in methanol 2 minutes. DIW rinse*. N_2 dry.

LEVEL 6: INTERGATE DIELECTRIC AND SECOND LEVEL GATE DEFINITION

9 .) PRE-OXIDATION CLEAN: use designated "oxidation clean" beakers.
SOLVENT CLEAN (see step 1)
PIRANHA CLEAN (see step 2)

80.) OXIDATION, INTERGATE DIELECTRIC: dry O_2, 1000 °C, # minutes;
30 minutes Ar anneal. Modified Slow load! . Oxidize. Anneal. Slow pull¥

---

* Flush with deionized water and decant at least 10 times. Soak for 1 minute. Flush and dry.
¶ Load at 800 °C in Ar; ramp to desired temperature @ -15 °C/min.
¥ Ramp to 800 °C in Ar @ -10 °C/min; use about 4-5 minutes to pull the sample out to RT.

81.) LPCVD POLYSILICON GATES: proceed immediately from (80).
Deposit 4000-4500 Å of polysilicon for the second level gate electrode.

82.) APPLY SPIN-ON DOPANT: see step (66).

83.) DRIVE-IN DOPANT: Use the furnace designated for dopant drive-in.
For 4000 Å poly-Si, drive at 950 °C for 20 minutes in a 25% O_2, 75% N_2 ambient.

84.) OXIDE ETCH, REMOVE SOD: remove the SOD from the surface of polysilicon.
Etch in BHF 2-3 minutes. DIW rinse* N_2 dry. Inspect.

86.) PRE-BAKE: 15 minutes @ 120 °C (inside the covered Petri dish). Cool to RT.

87.) HMDS TREATMENT: Place samples in uncovered Petri dish into the dessicator containing the HMDS. Evacuate and wait 2-3 minutes before venting.

88.) APPLY POSITIVE PHOTORESIST: Shipley 1350JSF, 5500 RPM, 30 seconds.

89.) POST-BAKE: 12-15 minutes @ 85-90 °C (inside the covered Petri dish). Cool to RT.

90.) ALIGN and EXPOSE, LEVEL 5: KSMJB3, High Precision, 6.5 seconds, 23 mW/cm^2.

91.) DEVELOP PHOTORESIST: Mix 5:1 DIW:AZ351 developer. Stlr!
Dip sample for 15 seconds. Rinse under flowing DIW for 1 minute. N_2 dry. Inspect.

92.) HARDBAKE: 15 minutes @ 120 °C (inside the covered Petri dish). Cool to RT.

93.) DRY ETCH POLYSILICON: PlasMa Technology RIE, (0.26)x10 sccm SF_6, 30 W, 320 mTorr. Turn power up to 30 W over 20 seconds, then etch for 20 seconds.

OR

WET ETCH POLYSILICON: Premixed $50HNO_3$:40DIW:3HF. Use magnetic stirrer. Holding the sample with Teflon tweezers, dip into briskly stirring etchant for 15-20s. Rinse under flowing DIW for 1 minute. N_2 dry. Inspect. Negative PR also works well. Etch rates: 350-430 Å/min for poly-Si, 310 Å/min for SiO_2.

94.) STRIP PHOTORESIST: Soak in ACE, 2 minutes. Repeat.
Rinse in methanol 2 minutes. DIW rinse*. N_2 dry.

LEVEL 7: SOURCE/DRAIN OXIDE WINDOW AND CONTACT DEPOSITION

95.) PRE-BAKE: 15 minutes @ 120 °C (inside the covered Petri dish). Cool to RT.

96.) HMDS TREATMENT: Place samples in uncovered Petri dish into the dessicator containing the HMDS. Evacuate and wait 2-3 minutes before venting.

97.) APPLY POSITIVE PHOTORESIST: Shipley 1350JSF, 5500 RPM, 30 seconds.

98.) POST-BAKE: 12-15 minutes @ 85-90 °C (inside the covered Petri dish). Cool to RT.

99.) ALIGN and EXPOSE, LEVEL 7: KSMJB3, High Precision, 7.5 seconds, 23 mW/cm^2.

100.) DEVELOP PHOTORESIST: Mix 5:1 DIW:AZ351 developer. Stlr!
Dip sample for 15 seconds. Rinse under flowing DIW for 1 minute. N_2 dry. Inspect.

101.) HARDBAKE: 15 minutes @ 120 °C (inside the covered Petri dish). Cool to RT.

102.) OXIDE WINDOW ETCH: Dip sample in BHF for 120 seconds. DIW rinse*. N_2 dry.
Inspect. Repeat for lower etch times until SiC surface is reached.

---

* Flush with deionized water and decant at least 10 times. Soak for 1 minute. Flush and dry.

103.) Ni EVAPORATION: Varian e-beam evaporator, 2E-7 Torr, 500 Å Ni.
Repeat step (102) with a 20 seconds dip and proceed immediately (do not inspect).
Load sample and pumpdown.

104.) LIFTOFF: Soak samples in ACE. Squirt ACE to remove unwanted metal.
Rinse under flowing DIW for 1 minute. N_2 dry. Inspect.

105.) APPLY POSITIVE PHOTORESIST: Shipley 1350JSF, 5500 RPM, 30 seconds.

106.) HARDBAKE: 15 minutes @ 120 °C (inside a covered Petri dish). Cool to RT.

107.) ETCH BACKSIDE: Remove oxide and polysilicon layers with wet etching (see step 93).

108.) DEPOSIT BACKSIDE CONTACT: Sputter deposit 1000 Å Pt.

109.) STRIP PHOTORESIST: Soak in ACE, 2 minutes. Repeat.
Rinse in methanol 2 minutes. DIW rinse*. N_2 dry.

110.) CONTACT ANNEAL: RTA 900 °C, 2 minutes, Ar ambient. No O_2 should be present!

LEVEL 8: INTERCONNECT DIELECTRIC AND VIA ETCH

111.) APPLY SOG INSULATOR: AccuGlass 311 SOG, thaw to RT before using.
A special Teflon chuck and Petri dish must be cleaned 2x with piranha before starting.
Begin to heat the very clean Petri dish on a hot-plate to about 150 °C.
SOLVENT CLEAN SAMPLES (see step 1).
Samples must be stored in a very clean Petri dish after this step.
SPIN: Attach very clean Teflon chuck to existing chuck. Spin 3000 RPM, 15 seconds.
CURE: Place sample into the Petri dish on the hot plate for 5-10 minutes.

112.) CURE SOG INSULATOR: 450 °C, 60 minutes, N_2 ambient.

113.) HMDS TREATMENT: Place samples in uncovered Petri dish into the dessicator containing the HMDS. Evacuate and wait 2-3 minutes before venting.

114.) APPLY POSITIVE PHOTORESIST: Shipley 1350JSF, 5500 RPM, 30 seconds.

115.) POST-BAKE: 12-15 minutes @ 85-90 °C (inside the covered Petri dish). Cool to RT.

116.) ALIGN and EXPOSE, LEVEL 8: KSMJB3, High Precision, 7.5 seconds, 23 mW/cm^2.

117.) DEVELOP PHOTORESIST: Mix 5:1 DIW:AZ351 developer. Stir!
Dip sample for 15 seconds. Rinse under flowing DIW for 1 minute. N_2 dry. Inspect.

118.) HARDBAKE: 15 minutes @ 120 °C (inside the covered Petri dish). Cool to RT.

119.) OXIDE WINDOW ETCH: Dip sample in BHF for 120 seconds. DIW rinse*. N_2 dry.
Inspect. Repeat for lower etch times until polysilicon and Ni are reached.

120.) Al EVAPORATION: NRC evaporator, 5V tap, Al_2O_3-W boat, three 0.5 cm bars of Al.
Clean boat, Al, and electrodes in solvents before loading. Deposit only 1000-2000 Å!

121.) LIFTOFF: Soak samples in ACE. Squirt ACE to remove unwanted metal.
Rinse under flowing DIW for 1 minute. N_2 dry. Inspect.

LEVEL 9: INTERCONNECT DEPOSITION AND ETCH

122.) Al EVAPORATION: NRC evaporator, 5V tap, Al_2O_3-W boat, three 0.5 cm bars of Al.
Clean boat, Al, and electrodes in solvents before loading. Deposit only 4000-5000 Å!

---

* Flush with deionized water and decant at least 10 times. Soak for 1 minute. Flush and dry.

123.) HMDS TREATMENT: Place samples in uncovered Petri dish into the dessicator containing the HMDS. Evacuate and wait 2-3 minutes before venting.

124.) APPLY POSITIVE PHOTORESIST: Shipley 1350JSF, 5500 RPM, 30 seconds.

125.) POST-BAKE: 12-15 minutes @ 85-90 °C (inside the covered Petri dish). Cool to RT.

126.) ALIGN and EXPOSE, LEVEL 9: KSMJB3, High Precision, 6.5 seconcls, 23 mW/cm^2.

127.) DEVELOP PHOTORESIST: Mix 5:1 DIW:AZ351 developer. Stir! Dip sample for 15 seconds. Rinse under flowing DIW for 1 minute. N_2 dry. Inspect.

128.) HARDBAKE: 15 minutes @ 120 °C (inside the covered Petri dish). Cool to RT.

129.) Al ETCH: Premixed $100H_3PO_4$:$100H_2C_4O_2$:$25HNO_3$:25DIW. Etch sample at RT. Etch until Al is gone. DIW rinse*. N_2 dry. Inspect.

130.) Al BACKSIDE DEPOSITION: An additional thick layer of metal can be deposited on the backside. Follow any of the Al deposition steps.

131.) ELECTRICAL CHARACTERIZATION

* Flush with deionized water and decant at least 10 times. Soak for 1 minute. Flush and dry.

APPENDIX II - PROGRAM LISTING FOR MULTIPLE IMPLANT CALCULATIONS

```
# This is a maple function which will plot a profile of a multiply
#  implanted ion into 6H-SiC.  One simply has to call 'multi_implant'
#  from within maple with the proper arguments.  An example is:
#
# multi-implant([[30,50,75],[2.2e11,2.4e11,2.6e11]],`N`,4000,600,`lin`);
#
#  where the energies are in keV and doses are in atoms/cm^2.
#  Depending on the atomic specie identified in the second argument,
#  a set of formulas will be used to calculate the four central moments
#  of the PearsonIV distribution that describes the profile.  The data
#  used here are from emperical fits reported by T.W. Sigmon [94].
#  THESE DATA ARE ONLY QUALIFIED FOR ENERGIES LESS THAN 300 KEV!
#  The value of No, which is the peak value of a single distribution, is
#  calculated by normalizing the area under the curve to the dose, Q.
#  The second argument in call must have a value of `B`, `Al`, or `N`
#  depending on the ion specie used for the simulation.
#  The third argument, d, just describes the depth of the window viewed
#  in this profile calculation.  The number is given in Angstroms.
#  Argument four, tox, is just a horizontal shift of the whole
#  distribution corresponding to the thickness of the screen layer.

readlib(`ln`): readlib(`evalf/int`):

multiTWS:=proc(eq,specie,d,tox,plotype)
depth:=d*1.0;
EQ:=convert(eq,matrix);
npoints:=100;
x:=linalg[vector](npoints+1,i->(i-1)*depth/npoints);  #x-axis array
y:=linalg[vector](npoints+1,0);                       #y-axis array
Nmax:='Nmax':
for i from 1 to linalg[coldim](EQ)
do
  EG := EQ[1,i]*1.0;
  Q := EQ[2,i];
  if specie-'Al` then
    c1:=15.8e-8:   m1:=0.945:       #Empirical eqns. for Al ions into
    c2:=19.8e-8:   m2:=0.699:       # SiC by T.W.Sigmon.
    c3:=4.24:   c4:=0.682:
    c5:=1.24;
    c6:=0.0: c7:=70.09e-09: c8:=8.303e-06: c9:=7.404e-06:
    c10:=119.5e+00;
  elif specie=`B` then
    c1:=49.0e-8:   m1:=0.824:       #Empirical eqns. for B ions into
    c2:=54.4e-8:   m2:=0.511:       # SiC by T.W.Sigmon.
    c3:=2.47:   c4:=0.551:
    c5:=1.35:
    c6:=0.0: c7:=94.15e-09: c8:=6.687e-06: c9:=5.084e-06:
    c10:=31.24e+00;
```

```
  else
    c1:=23.9e-8:   m1:=0.885:        #Empirical eqns. for N ions into
    c2:=29.1e-8:   m2:=0.552:        # SiC by T.W.Sigmon.
    c3:=2.05:   c4:=0.533:
    c5:=1.03:
    c6:=79.54e-12: c7:=32.42e-09: c8:=5.001e-06: c9:=4.378e-06:
    c10:=23.54e+00;
  fi:

  lp:=c1*EG^m1:          #calculate the moments
  sigma[p]:=c2*EG^m2:
  gama:=c3-c4*ln(EG):
  beta[0]:=(39*gama^2+48+6*(gama^2+4)^(3/2))/(32-gama^2):
  beta:=c5*beta[0];
  `Q'`:=c6*EG*EG+c7*EG+c8-c9*exp(-EG/c10);  #normalized area in (cm)

  C:=1/(2*(5*beta-6*gama^2-9)):
  b0:=-sigma[p]^2*(4*beta-3*gama^2)*C:
  b1:=-gama*sigma[p]*(beta+3)*C:
  b2:=-(2*beta-3*gama^2-6)*C:

# Using Pearson IV distribution;
  m:=-1/2/b2:
  r:=2*(m-1):
  n:=-r*b1/sqrt(4*b0*b2-b1*b1):
  A:=m*r*b1/n:
  K:='K':
  f:=x->K*(1+((x-Rp)/A-n/r)^2)^(-m)*exp(-n*arctan((x-Rp)/A-n/r)):
  f(Rp)=1:                       #normalize PearsonIV curve.
  K:=(solve(",K));
  No:=Q/`Q'`;                    #calculate peak from dose.
  if No>Nmax or type(Nmax,name)=true then
    Nmax:=No:
  fi:
  K:=K*No;                 #normalize to peak value.
  y:=linalg[vector](npoints+1,i->f(x[i]*1e-8)+y[i]);
od;
x:=evalm(x-tox);

# format and plot the profile to the screen.
Title:="".specie.'  -> SiC:\t[[`:
for i from 1 to linalg[coldim](EQ)-1 do
Title:=cat(Title,FFF(EQ[1,i],e,3),.,`);
od:
Title:=cat(Title,FFF(EQ[1,linalg[coldim](EQ)],e,3),`],[`):
for i from 1 to linalg[coldim](EQ)-1 do
Title:=cat(Title,FFF(EQ[2,i],e,3),.,`);
od:
Title:=cat(Title,FFF(EQ[2,linalg[coldim](EQ)],e,3),`]],tox = `,tox,`Å`);

if plotype=`lin` then
  plot(convert(zip(<[a,b]|a,b>,x,y),list),'depth (A)`=-tox..depth-tox,\
       `N (1/cm^3)`=Nmax/1e4..2*Nmax,title=Title);
else
  plots[logplot](convert(zip(<[a,b]|a,b>,x,y),list),`depth (A)`=-
tcx..depth-to~,\
         `N (1/cm^3)`=Nmax/1e4..10*Nmax,title=Title,axes=normal);
```

```
fi;

end:


#
#--> FFF(z); convert an integer, float (complex) to Fortran E notation
#
# If x is Maple integer, float, complex integer or complex float,
# the result returned is a string in Fortran readable E notation.
# The output is normalized to contain one leading digit
# before the decimal point, but the number of significant digits
# can be specified in the third argument.
# If a single letter is given as a 2nd optional argument, it will
# be used instead of e (the default).  I.e. typically you will want to
pass
# D for double precision, and H for quadruple precision.
#
# F'FF(0.0123);          `1.23e-2`
# FFF(3.1+2.2*I); `(3.1e0,2.2e0)`
# E'FF(1.23,D);          `1.23D0`
# FFF(1.23,E);           `1.23E0`
#
# Author: MBM May/91; revised RKW Aug/92; revised STS Jan/94
#

FFF := proc(f)
local mantissa,exponent,letter,prefix,iota;

    if nargs = 1 then letter := 'e'
    elif type(args[2],string) and length(args[2]) = 1 then. letter :=
args[2]
    else ERROR(`2nd argument must be a letter')
    fi;

    iota:=Digits:
    if nargs = 3 then
      if not type(args[3],integer) then
        ERROR(`3rd argument must be an integer')
      else
        iota:=args[3];
        Digits:=iota;
      fi;
    fi;

    if type(f,integer) then mantissa := f; exponent := 0
    elif type(f,float) then
      mantissa := op(1,evalf(round(f*10^iota)/10^iota));
      exponent := op(2,evalf(round(f*10^iota)/10^iota));
    elif type(f,complex(numeric)) then
      RETURN( cat( ``(``, FFF(evalc(Re(f)),letter), ``,``,
                   FFF(evalc(Im(f)),letter), ``)`` ) )
    else ERROR(`integer, float or complex float expected')
    fi;

    if mantissa = 0 then prefix := ``0``
    elif mantissa < 0 then prefix := ``-``; mantissa := -mantissa
```

```
    else prefix := ``'
    fi:

    # Normalize so that 1 digit appears before the decimal point
    if mantissa <> 0 then
        exponent := exponent+length(mantissa)-1;
        mantissa := "".mantissa; # convert to string
        prefix := cat(prefix, substring(mantissa,1..1));
        mantissa := substring(mantissa,2..length(mantissa));
    fi;

    if exponent>=4 then
        cat(prefix,``.`',mantissa,letter,exponent)
    else
        mantissa:=convert(evalf(round(f*10^iota)/10^iota),string);
    fi;

end:

`type/complex` := proc(x,t)
    type(x,t) or x=I or
    type(x,`+`) and nops(x)=2 and procname(op(1,x),t)
                    and procname(op(2,x),t) or
    type(x,`*`) and nops(x)=2 and type(op(1,x),t)
                    and op(2,x)=I
end:
```