ECE 340
Lecture 34 : MOS Capacitor II

Class Outline:

- Effects of Real Surfaces
- Threshold Voltage
- MOS Capacitance-Voltage Analysis

Key Questions

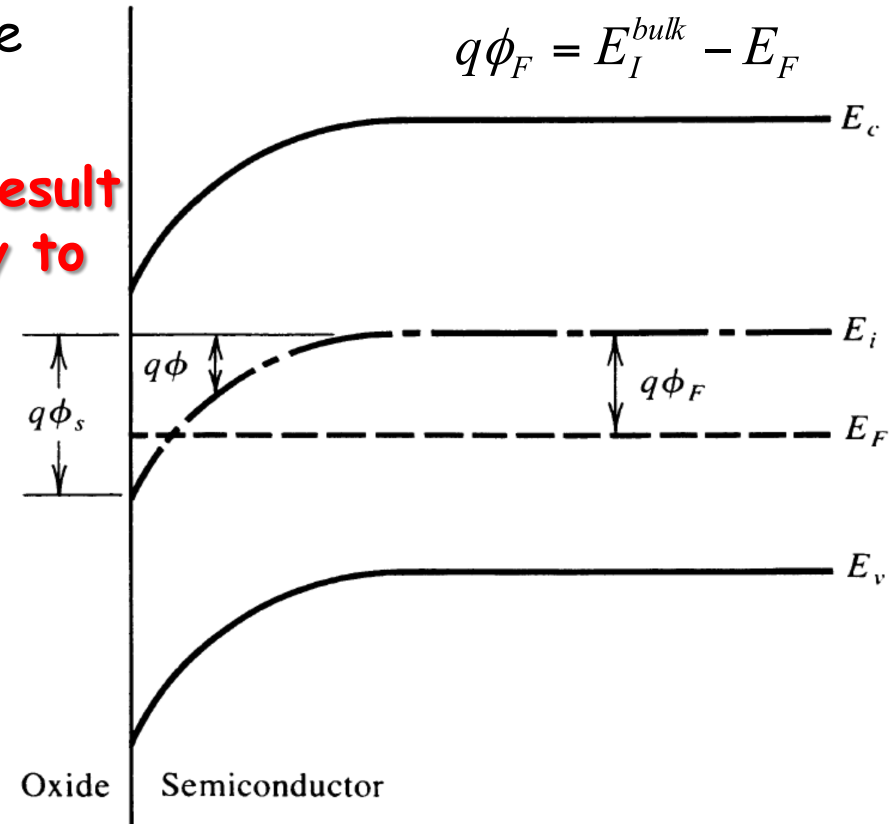
- What are the effects of real surfaces on the MOS capacitor?
- How does the threshold voltage change when real surfaces are considered?
- What information can I get from MOS capacitance – voltage plots?

Effects of Real Surfaces

During the last lecture, we discussed the **ideal MOS capacitor**…

The n-type surface that forms as a result of the applied electric field is the key to transistor operation!

- Define a potential $q\varphi_S$ which determines how much band bending there is at the surface.
- When $q\varphi_S = 0$ we are in flat band condition.
- When $q\varphi_S < 0$ we have hole accumulation at the surface.
- When $q\varphi_S > 0$ we have electron depletion at the surface.
- When $q\varphi_S > q\varphi_F$ we have inversion at the surface.
- **Surface should be as strongly n-type as the body is p-type.**



$$\phi_S^{INV} = 2\phi_F = 2\frac{k_bT}{q}\ln\left(\frac{N_A}{n_i}\right)$$

$$\phi_S^{INV} = 2\phi_F = 2\frac{k_bT}{q}\ln\left(\frac{N_D}{n_i}\right)$$

Effects of Real Surfaces

We understand the **surface charge**: $$Q_s = -\varepsilon_s \xi_s$$

So what does the **surface charge density** look like?

- At φ_s = 0 there is no space charge.
- When φ_s is negative we accumulate majority holes at the surface.
- When φ_s is positive initially the linear term in the electric field solution dominates as a result of the exposed, immobile dopants.
- Depletion extends over several hundred nm until we reach strong inversion and the exponential field term dominates.

p-type Si (300 K)
$N_a = 4 \times 10^{15}$ cm^{-3}

$$\mathscr{E}_s = \frac{\sqrt{2}kT}{qL_D}\left[\left(e^{-\frac{q\phi_s}{kT}} + \frac{q\phi_s}{kT} - 1\right) + \frac{n_0}{p_0}\left(e^{\frac{q\phi_s}{kT}} - \frac{q\phi_s}{kT} - 1\right)\right]^{\frac{1}{2}}$$

~ exp $(-q\phi_s/2kT)$ (Strong inversion)

~ exp $(-q\phi_s/2kT)$ (Accumulation)

Holes

Electrons

Ionized acceptors

$2\phi_F$

$p_s > N_a$

$n_s > N_a$

Flat band

$\sim \sqrt{\phi_s}$

$n_s < N_a$, $p_s < N_a$: Depletion

$n_s < N_a$, $n_s > p_s$: Weak inversion

E_v E_i E_c ϕ_F

Q_s (coul/cm^2): 10^{-4}, 10^{-5}, 10^{-6}, 10^{-7}, 10^{-8}, 10^{-9}

ϕ_s (volt): −0.4, −0.2, 0, 0.2, 0.4, 0.6, 0.8, 1.0

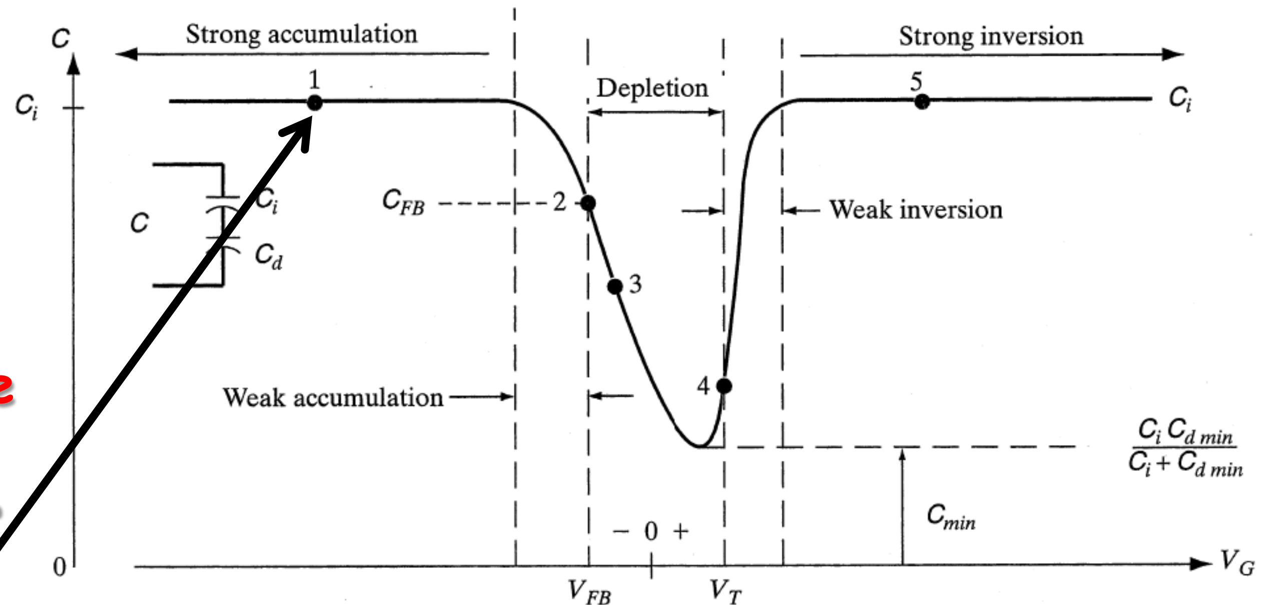
Effects of Real Surfaces

We understand the system capacitance…

The **capacitance** depends on the voltage…

$$C_s = \frac{dQ}{dV} = \frac{dQ_s}{d\phi_s}$$

MOS Capacitor is the **series combination of the oxide and the voltage dependent semiconductor capacitances**.



In accumulation:

- The capacitance is huge.
- Structure acts like a parallel plate capacitor piling holes up at the surface. $C_i = \varepsilon_i / d$

Effects of Real Surfaces

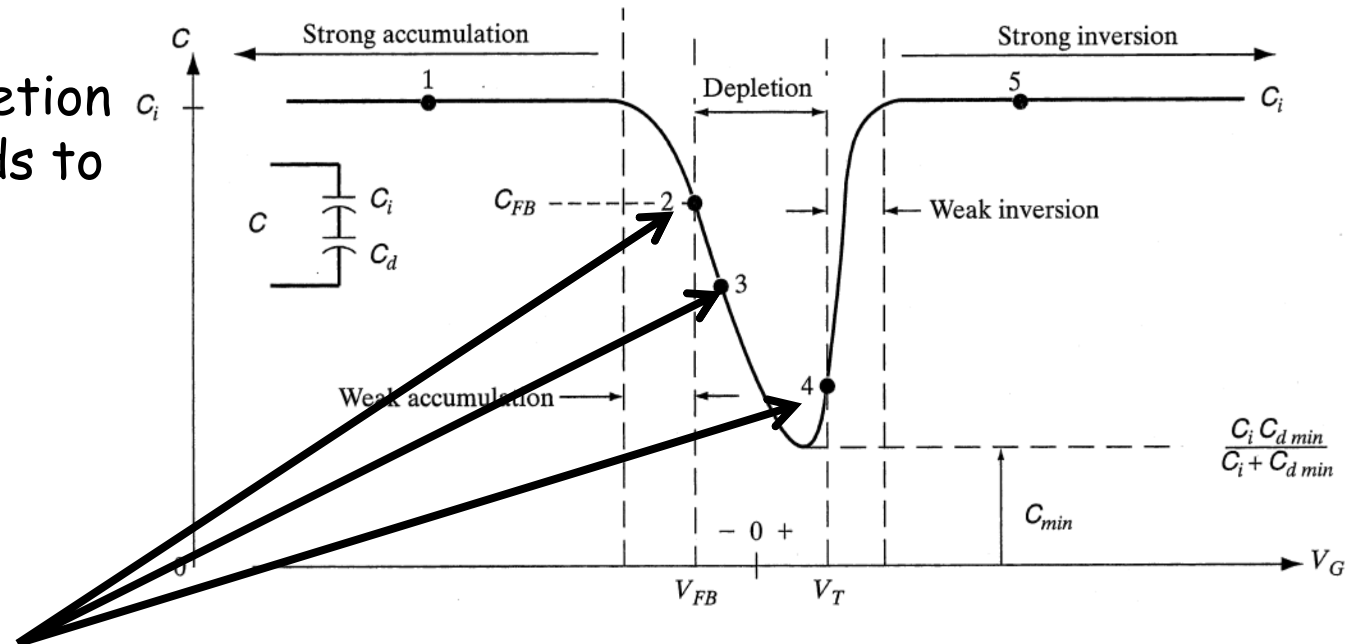
And how the capacitance behaves as we **vary the bias**...

The surface becomes depleted and the depletion layer capacitance needs to be added in...

$$C_d = \varepsilon_s / W$$

Total capacitance:

$$C = \frac{C_i C_d}{C_i + C_d}$$



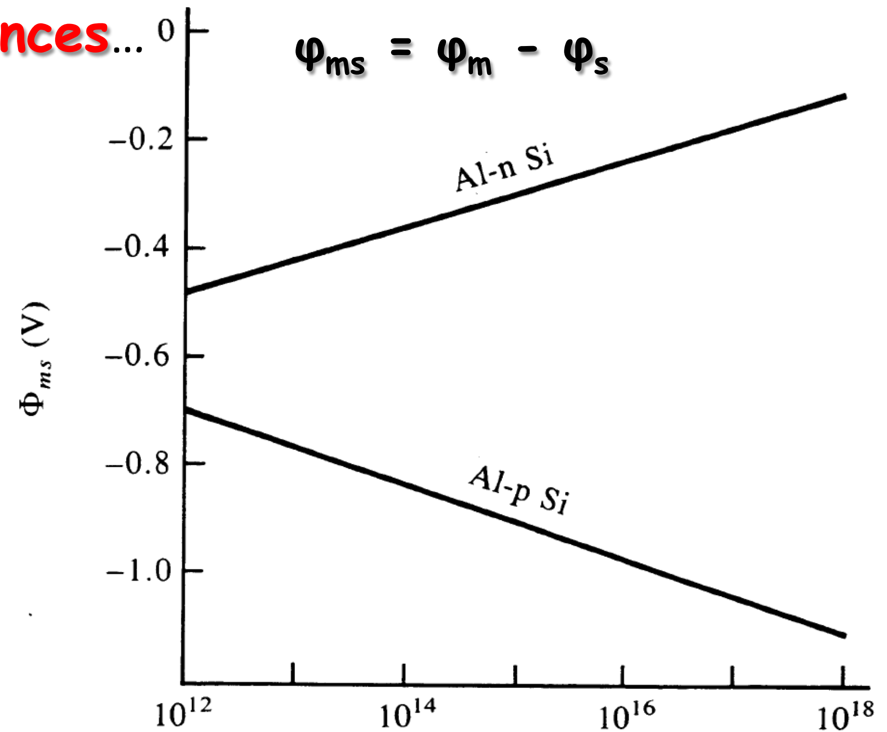
In depletion:

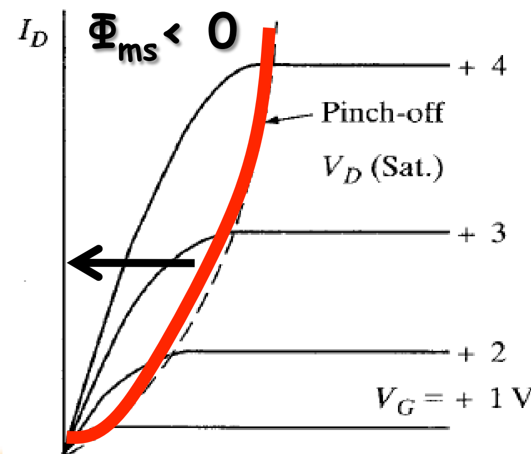
- Capacitance decreases as W grows until inversion is reached.
- Charge in depletion layer of MOS capacitor increases as ~ $(\varphi_S)^{1/2}$ so depletion capacitance decreases as the inverse.
- **If signal applied to make measurement is too fast, inversion layer carriers can't respond and do not contribute.**
- Slowly varying signals allow time for minority carriers to be generated, drift across depletion region, or recombine.
- Majority carriers in the accumulation region respond much faster.

Effects of Real Surfaces

Real surfaces have **workfunction differences**…

- Workfunction differences can significantly affect V_T and other properties.
- The difference is always negative and is most negative for heavily p-type Si.
- This is reminiscent of the work on the metal-semiconductor contacts.





Tends to decrease the threshold voltage…

Effects of Real Surfaces

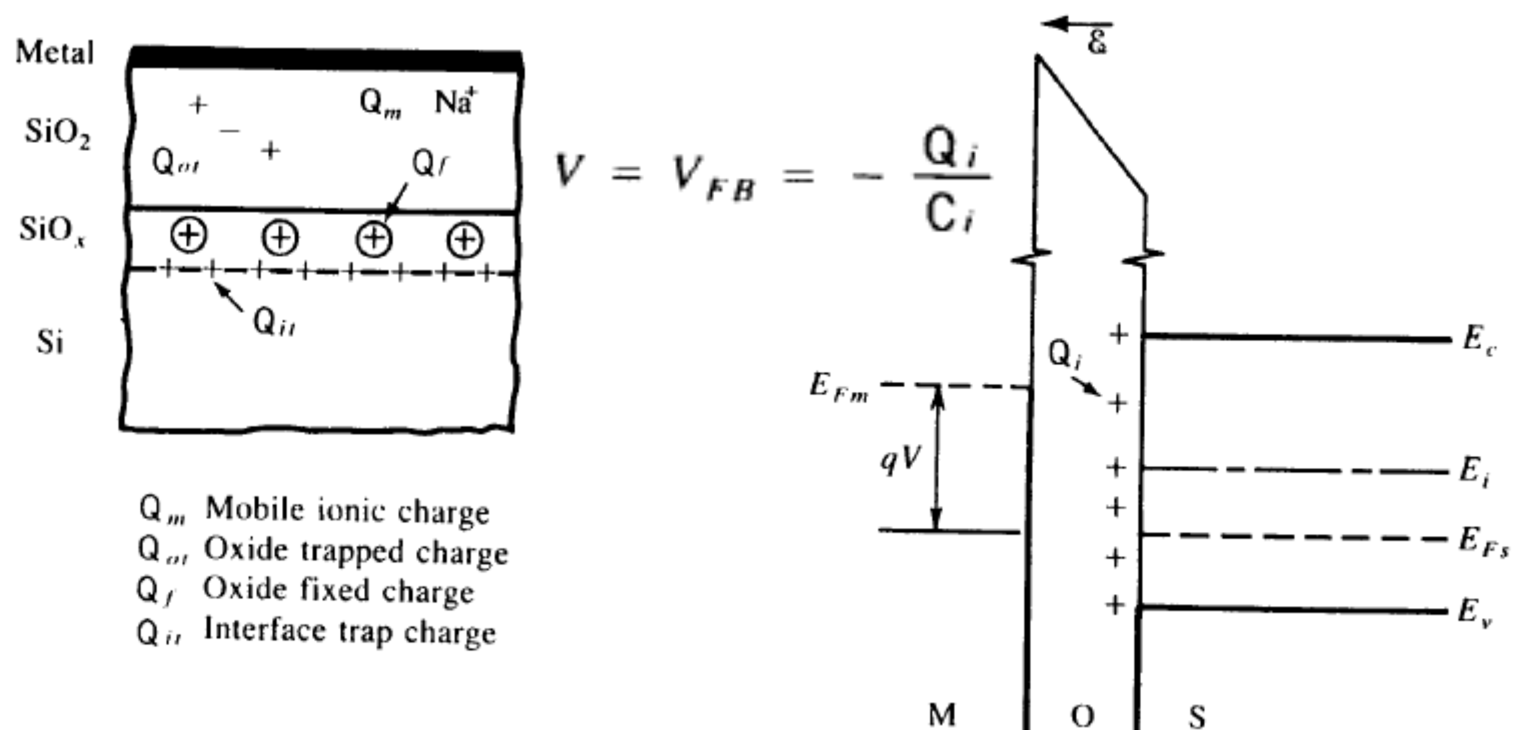
So what does this mean for our band diagrams…

$V = V_{FB} = \Phi_{ms}$

- The negative workfunction difference causes the bands to be pulled down farther in equilibrium.
- To achieve flatband conditions, we must apply a positive voltage to overcome the inherent bending in the bands,
- **Clearly, this behavior will lead to shifts in the threshold voltage.**

Effects of Real Surfaces

What about the effects of **trapped oxide charges**?

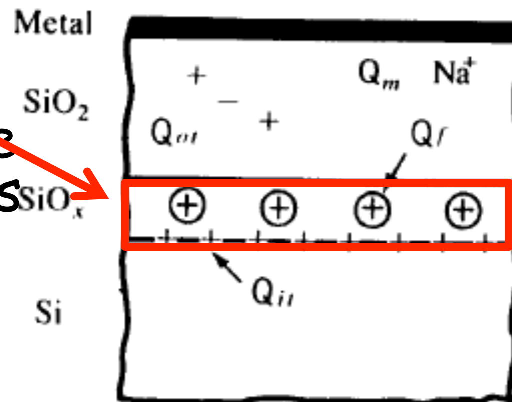


- Alkali metals can easily be incorporated in the oxide during the fabrication process.
- These metals induce positive charges in the oxides which induce negative charges in the semiconductor.
- **The magnitude of the effect depends on the number of sodium atoms and their distance from the surface.**
- **The atoms may drift in applied fields which leads to a continuous change in the threshold voltage.**

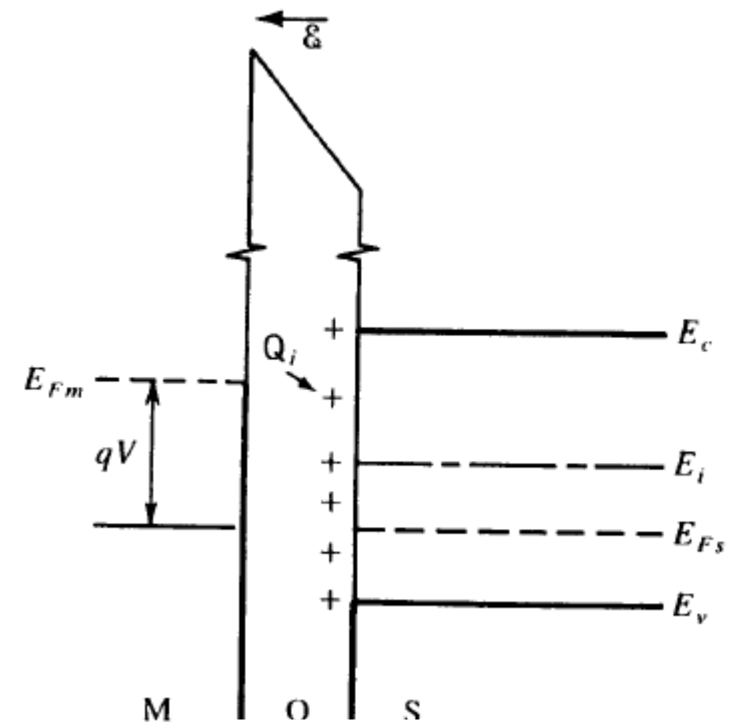
Effects of Real Surfaces

What about **oxide charges**?

- Positive charges arise from interface states at the Si-SiO2 interface.
- When oxidation is stopped, some ionic silicon is left near the surface.
- These ions along with other uncoupled bonds forms a sheet of positive charge at the interface.
- The charges depend on oxidation rate, heat treatment, and crystal orientation.



Q_m Mobile ionic charge
Q_{ot} Oxide trapped charge
Q_f Oxide fixed charge
Q_{it} Interface trap charge



$$V = V_{FB} = -\frac{Q_i}{C_i}$$

Why are devices made on [100] instead of [111]?

- **Because interface charges are 10x higher on [111] relative to [100].**

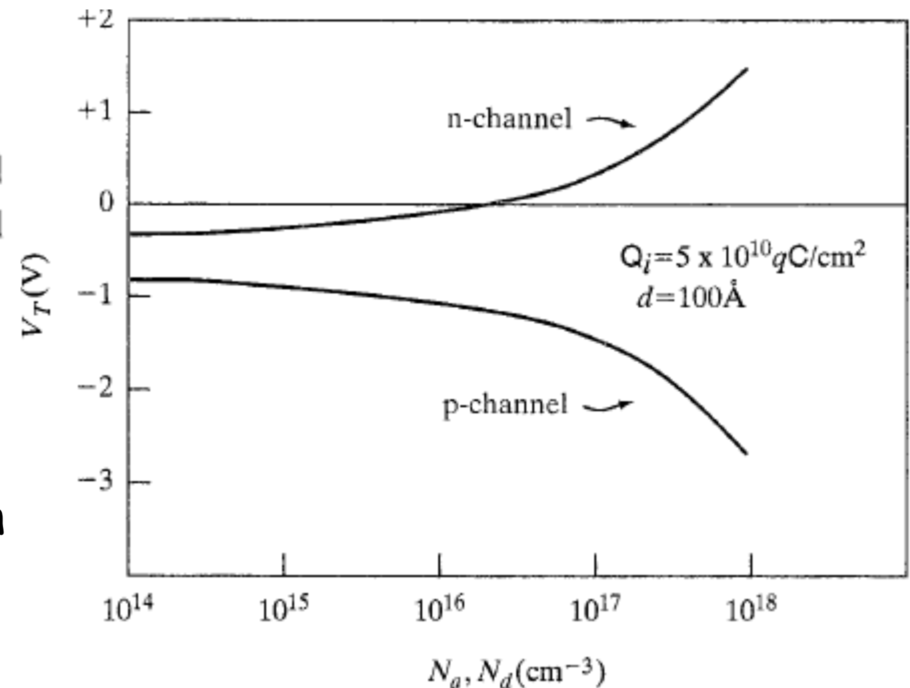
Threshold Voltage

Based on our knowledge of real surfaces, we must rethink the **threshold voltage**…

The **threshold voltage** becomes: $V_T = \Phi_{ms} - \frac{Q_i}{C_i} - \frac{Q_d}{C_i} + 2\phi_F$

Thus, the threshold voltage must be strong enough to **achieve flatband**, **accommodate the charge in the depletion region**, and **induce the inverted region**.

$V_T =$	Φ_{ms}	$-\frac{Q_i}{C_i}$	$-\frac{Q_d}{C_i}$	$+2\phi_F$
	(−)	(−)	(+) n channel (−) p channel	(+) n channel (−) p channel



Here we show the signs corresponding to each of the different effects on the threshold voltage. The total result is shown to the right for n-channel and p-channel.

MOS Capacitance-Voltage Analysis

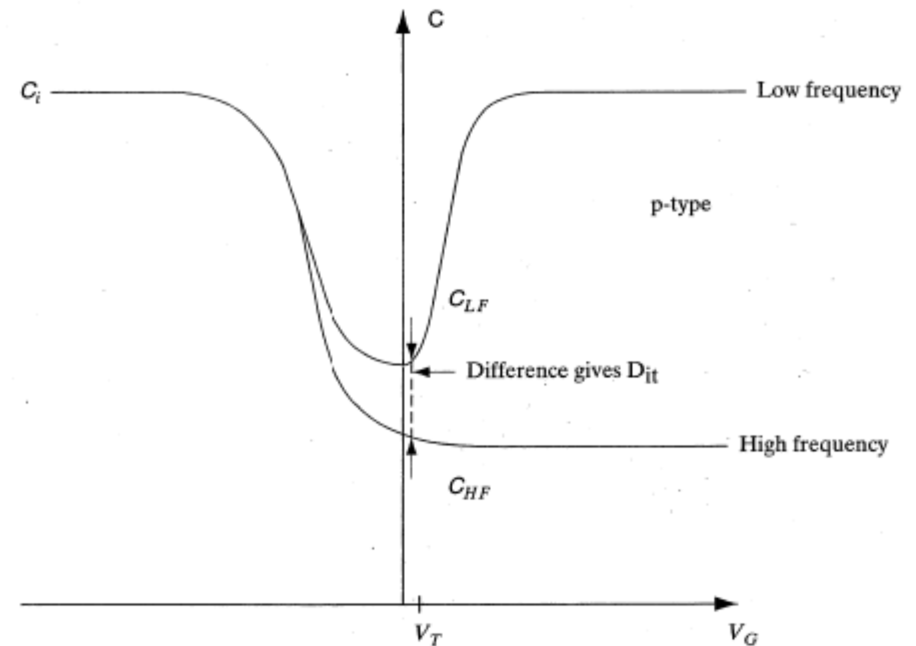
Can't we get more information from the capacitance-voltage data?

We can get a lot of information from the capacitance-voltage (C-V) data.

- Insulator thickness
- Substrate doping
- Threshold voltage

Shape of the C-V curve depends on the type of substrate doping.

- P-type:
  - High frequency capacitance: large for negative gate bias and small for positive bias
  - Low frequency C-V curve: as gate bias becomes more positive (or negative) C goes down slowly in depletion and raises quickly in inversion

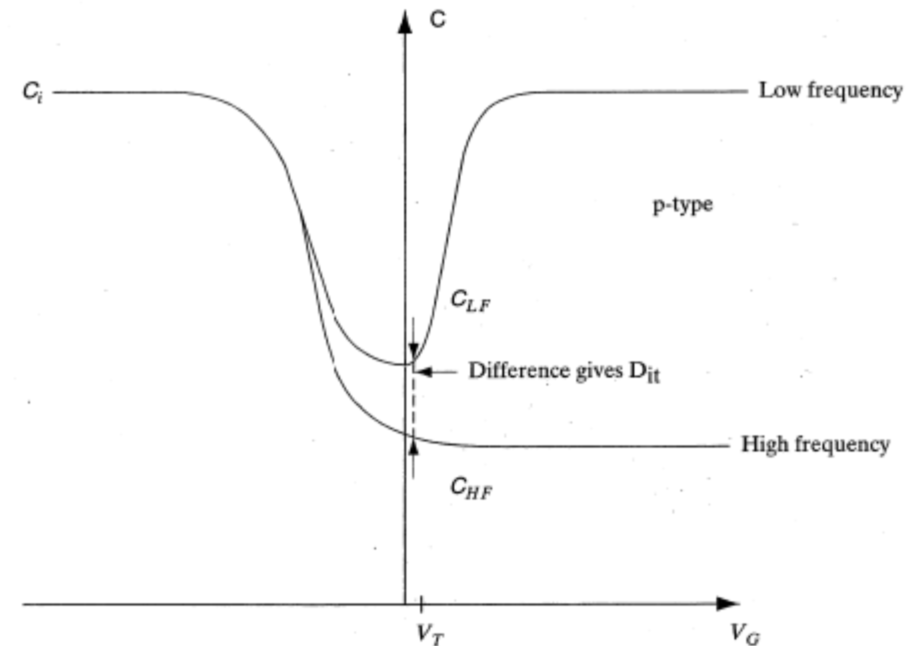


- **Remember: that majority carriers respond faster to changes in V_G and minority carriers respond more slowly**

MOS Capacitance-Voltage Analysis

Let's find the **insulator thickness** and the **depletion width**…

- By using the capacitance ($C_i = \varepsilon_i/d$) in accumulation or strong inversion at low-frequency will give us the **insulator thickness**.
- The capacitance C_{min} is the series combination of the capacitance C_i and the minimum depletion capacitance $C_{dmin} = \varepsilon_s/W_m$.
- This will give us the **maximum depletion width**.



$$W_m = \left[\frac{2\varepsilon_s \phi_s(inv.)}{qN_a}\right]^{1/2} = 2\left[\frac{\varepsilon_s kT \ln(N_a/n_i)}{q^2 N_a}\right]^{1/2}$$

This is a transcendental equation which requires a numerical solution. **It's solution gives N_A in terms of C_{dmin}.**

MOS Capacitor-Voltage Analysis

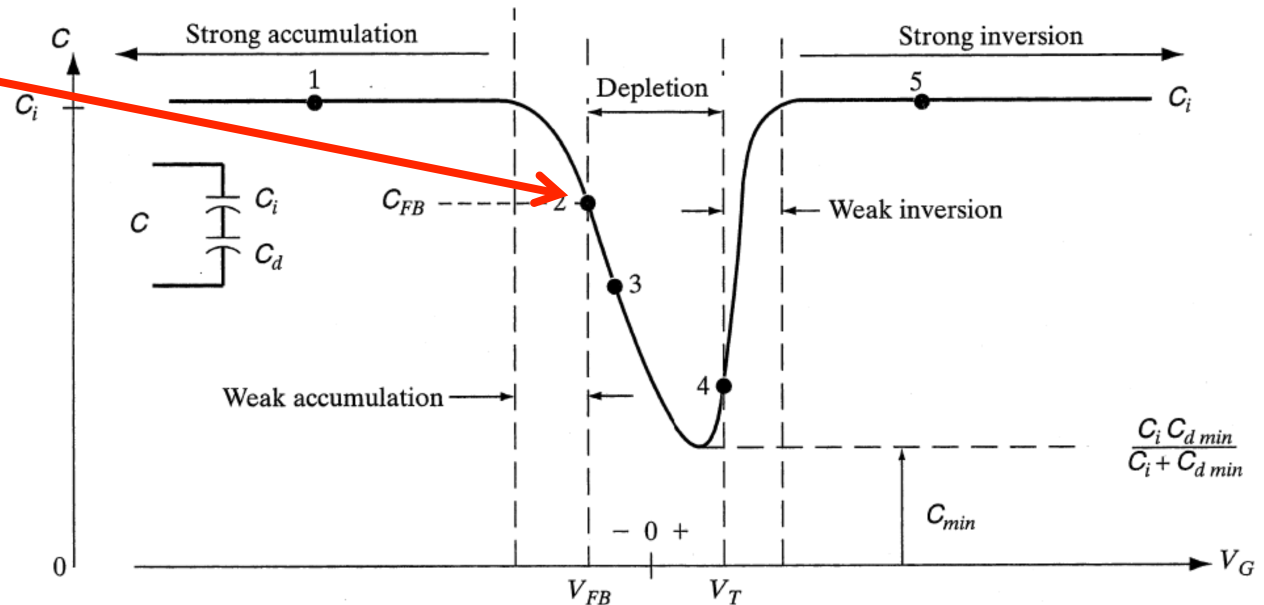
Once we know the substrate doping, we can find the **flatband capacitance**…

The flatband capacitance is determined from the Debye length capacitance…

$$C_{debye} = \frac{\sqrt{2}\varepsilon_s}{L_D}$$

The Debye length depends on the doping…

$$L_D = \sqrt{\frac{\varepsilon_s kT}{q^2 p_o}}$$



- **The overall MOS FB capacitance C_{FB} is the series combination of C_{debye} and C_i. From these values we can determine V_{FB} the corresponds to C_{FB}.**

MOS Capacitor-Voltage Analysis

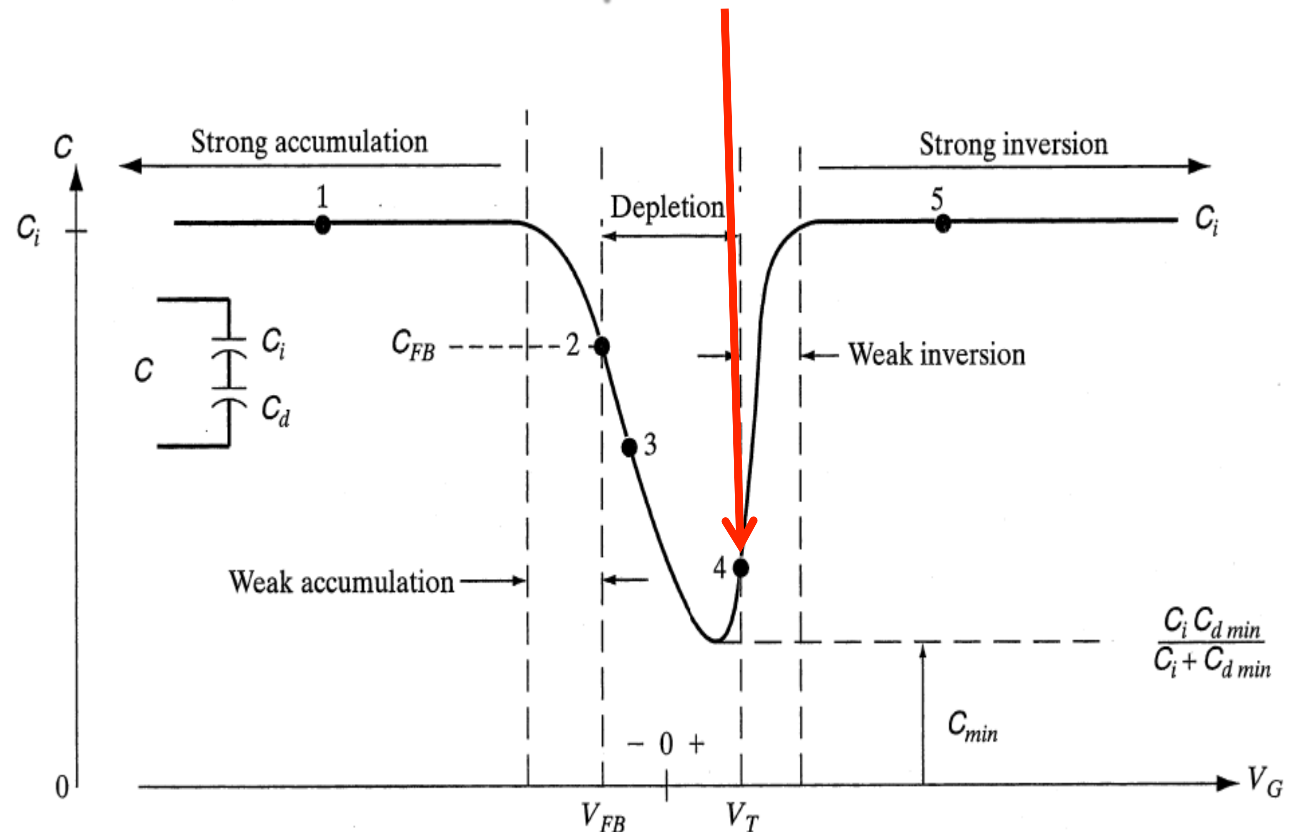
We now have all of the ingredients to calculate the **threshold voltage**…

$$V_T = \Phi_{ms} - \frac{Q_i}{C_i} - \frac{Q_d}{C_i} + 2\phi_F$$

VT does not correspond exactly to C_{dmin} but rather to **point 4** which is located at $C_i + 2\ C_{dmin}$.

Why ??

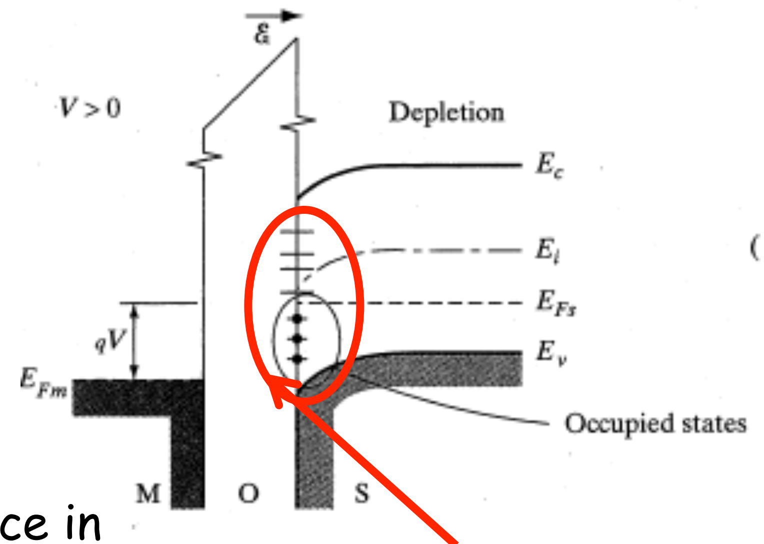
Because change of charge in semiconductor is the sum of the change in the depletion charge and the mobile inversion charge which are equal at onset of strong inversion.



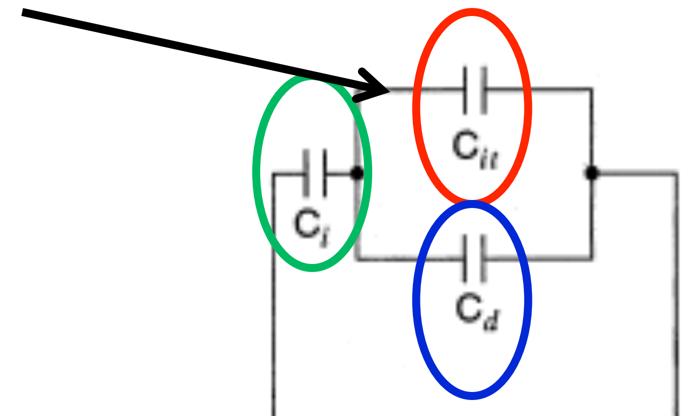
MOS Capacitor-Voltage Analysis

We can gain further information about the **interface states**…

- Fast interface state densities
  - Defect states can change charge state rapidly.
  - Changes in the surface potential can move the Fermi energy above or below states in the bandgap and change their occupancy .



These **fast interface states** give rise to capacitance in parallel with the **depletion capacitance** both of which are in series with the **insulator capacitance**.



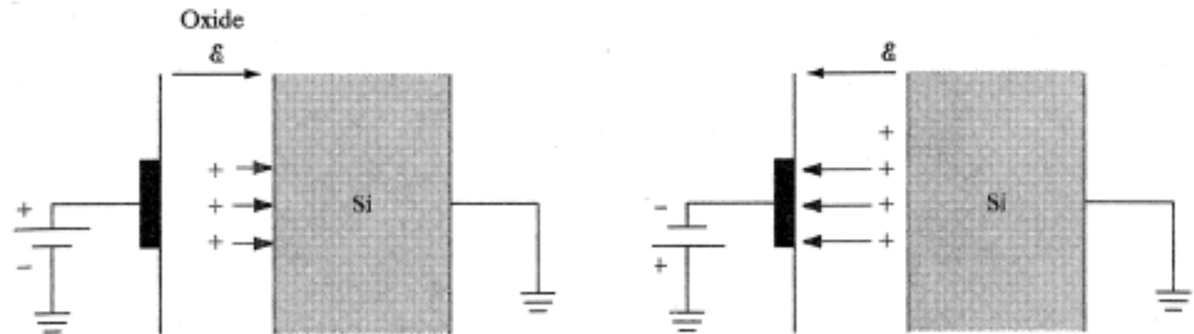
- Fast interface states:
  - Can follow 1 – 1 kHz changes in gate bias but not high frequency (> 1 MHz).
  - They contribute to the low frequency capacitance but not the high frequency.
  - The differences between these two capacitances gives the interface state densities as a function of energy.

$$D_{it} = \frac{1}{q}\left(\frac{C_i C_{LF}}{C_i - C_{LF}} - \frac{C_i C_{HF}}{C_i - C_{HF}}\right) cm^{-2} eV^{-1}$$

MOS Capacitor-Voltage Analysis

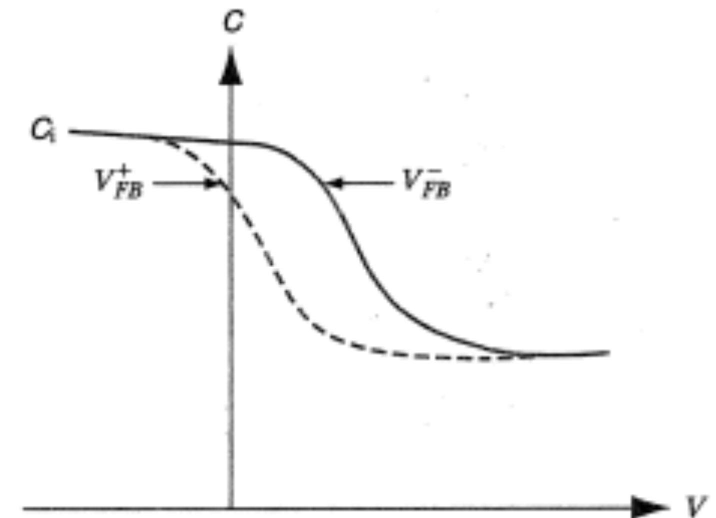
What about **mobile ion charges**?

- Fixed oxide charges do not change charge state.
  - Effects on V_{FB} and V_T depend on location relative to interface.
- Mobile ions can change charge state.



Use **bias-temperature stress test**…

- Heat MOS device to ~ 200 – 300 C
- Apply positive gate voltage (~1 MV/cm in oxide layer)
- Mobile positive ions are repelled to the SiO2-Si interface.
- Make room temperature C-V measurement to determine V_{FB}.
- Switch the bias configuration to negative.
- Now ions drift towards the gate electrode.
- They are now too far away to affect band bending but induce equal and opposite charge on the gate electrode.
- Make another C-V measurement of V_{FB}.



$$Q_m = C_i(V^+_{FB} - V^-_{FB})$$