ECE 340
Lecture 38 : MOS Capacitor I

Class Outline:

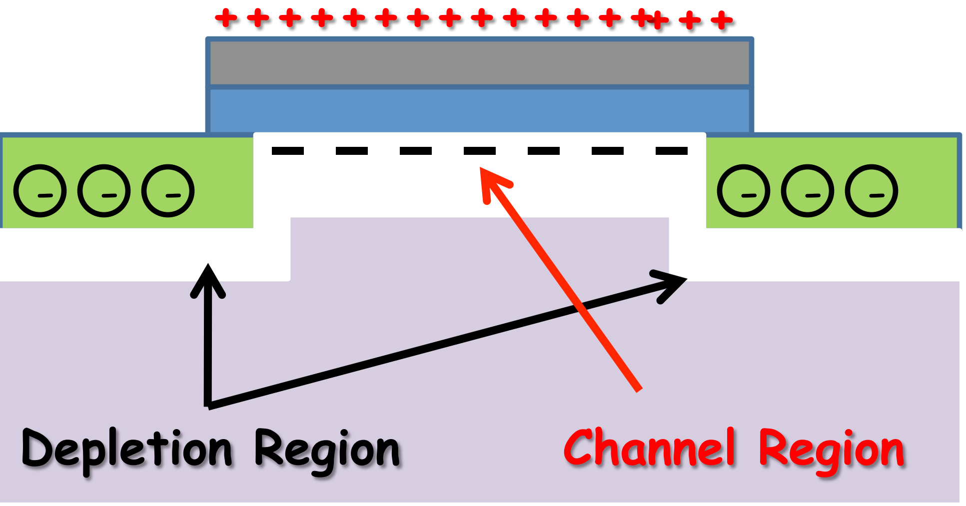
- Ideal MOS Capacitor

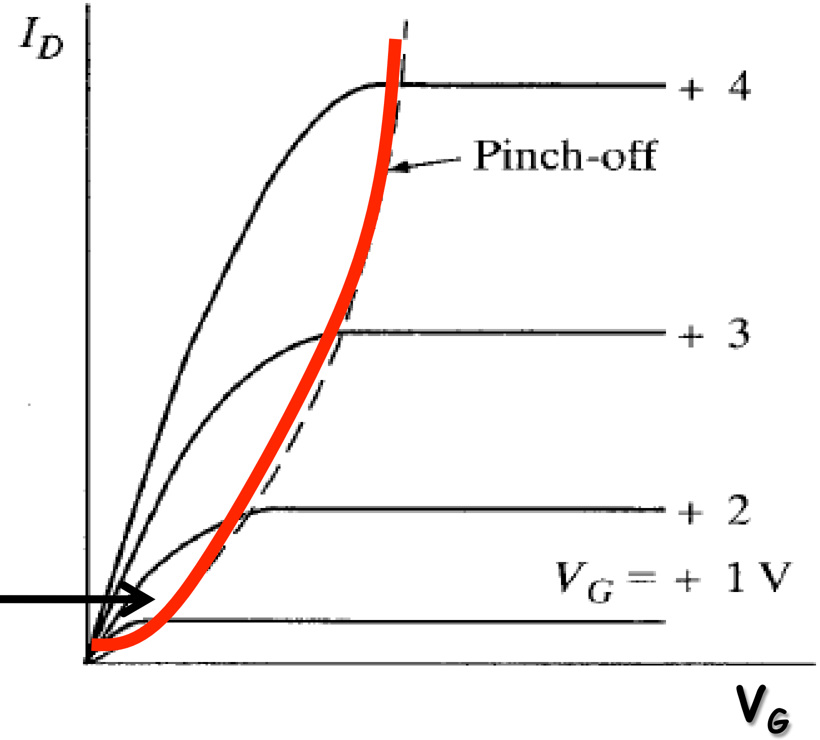
Key Questions

- What are the different bias regions in MOS capacitors?
- What do the electric field and electrostatic potential look like?
- What is the Debye length?
- What does the capacitance look like as a function of bias?

Ideal MOS Capacitor

Last time, we discussed the basic operation of the MOSFET…

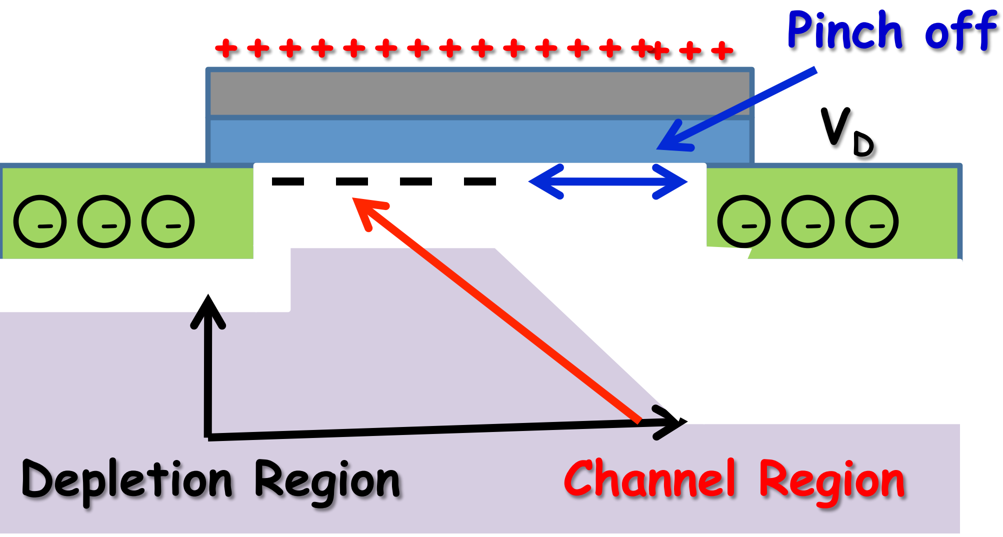


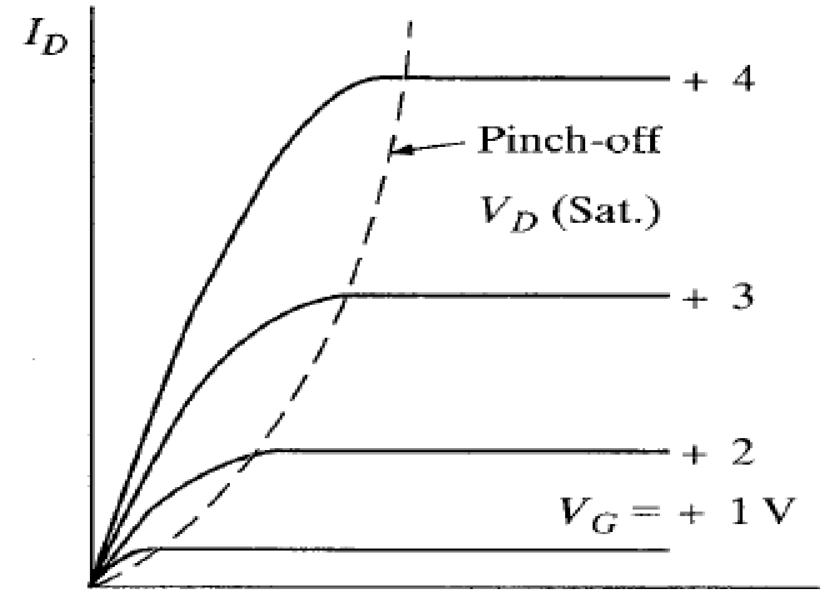


- When the barrier region is sufficiently reduced, then a current flows from the source to the drain.
    - As we put more positive charge on the gate, more holes are repelled depleting the concentration near the surface and populating it with electrons.
    - The point in the gate voltage sweep when significant current begins to flow is the **threshold voltage, V_T**.
    - This corresponds to the point when the channel is formed under the gate.
    - Were we to have made a PNP device the application of a negative VG would repe electrons and attract hole forming a channel.

Ideal MOS Capacitor

And how it operates as we vary V_D…





•With V_D swept in small positive increments, the channel merely acts like a resistor and the drain current is proportional to the drain voltage.

•Past a few tenths of a volt of bias, the voltage drop from the source to the drain associated with current flow begins to negate the inverting effect of the gate.

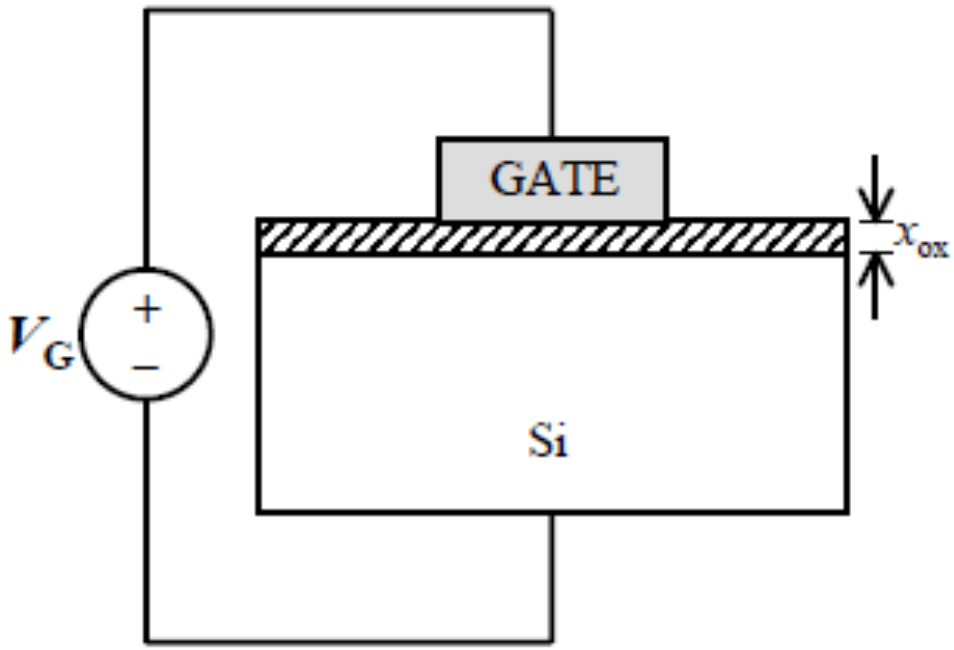
•Channel carriers begins to decrease leading to a reduction in the channel conductivity. This is due to the electron flow not being through the channel but a larger region about the drain.

  •Drain current is said to be in saturation as changes in V_D produce no changes in I_D.

Ideal MOS Capacitor

But we saw that the operation in most regimes was controlled by the channel…

The channel of a MOSFET is an example of a **MOS capacitor**…



What is the structure of a MOS capacitor?

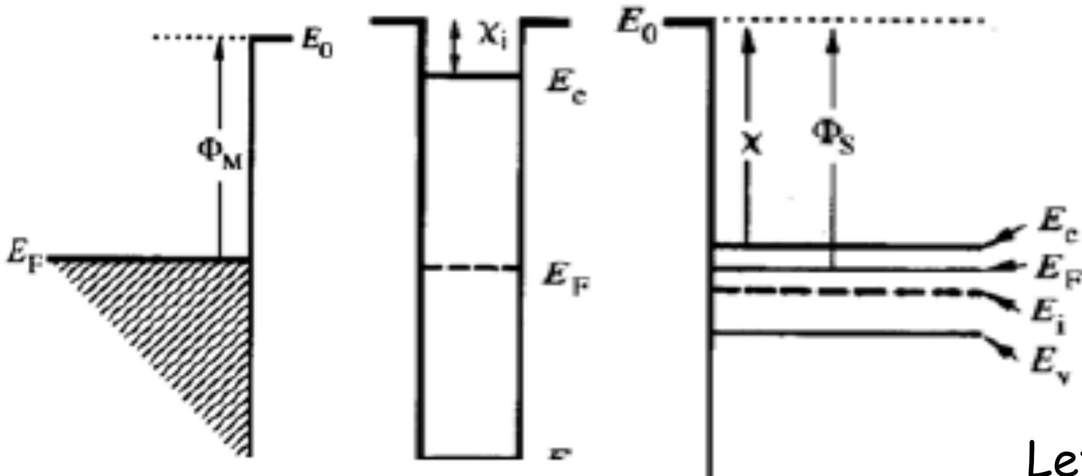
- Heavily doped polycrystalline Si film as the gate electrode material.
  - N-type for "n-channel" transistors (NMOS).
  - P-type for "p-channel" transistors (PMOS).
- SiO_2 as the gate dielectric
  - Band gap = 9 eV.
  - Relative dielectric constant ε_r = 3.9.
- Si as the semiconductor material.
  - P-type for n-channel devices.
  - N-type for p-channel devices.

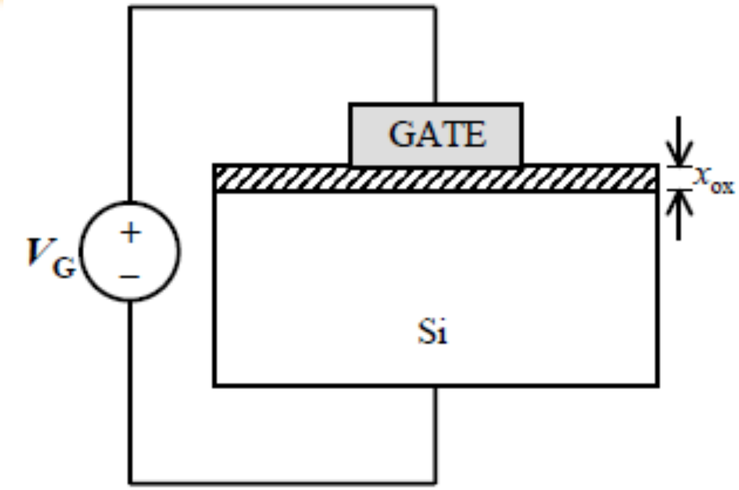
Useful for:

- Digital and analog logic
- Memory functionality
- Imaging (CCD) and displays (LCD)

Ideal MOS Capacitor

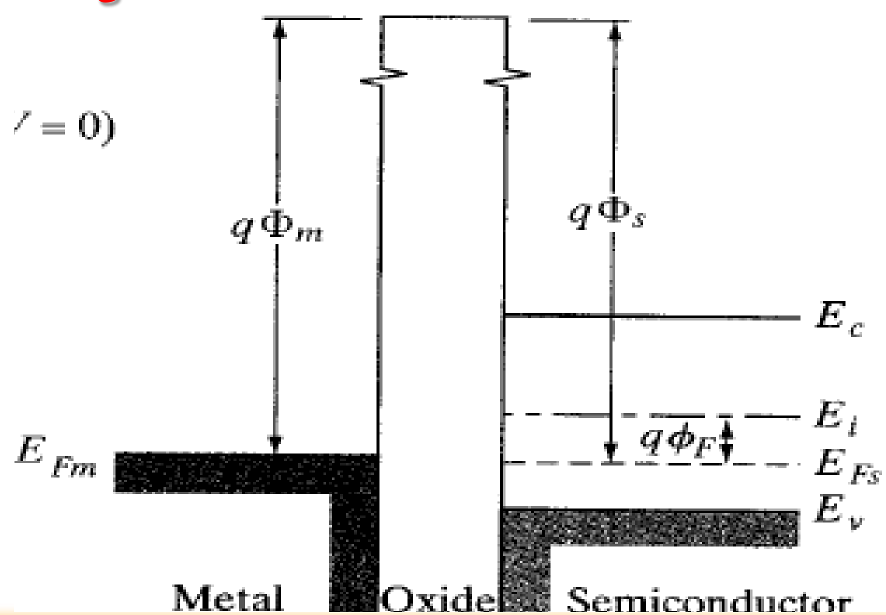
Remember all of the components…





- Charges only exist at the surface of the metal.
- We assume that there are no charges or dopants located in the oxide region.
- We cannot achieve thermal equilibrium through the oxide layer.
- **To achieve thermal equilibrium we need to use a wire to connect the metal to the semiconductor**.

Let's start with the ideal situation, $\Phi_M = \Phi_S$

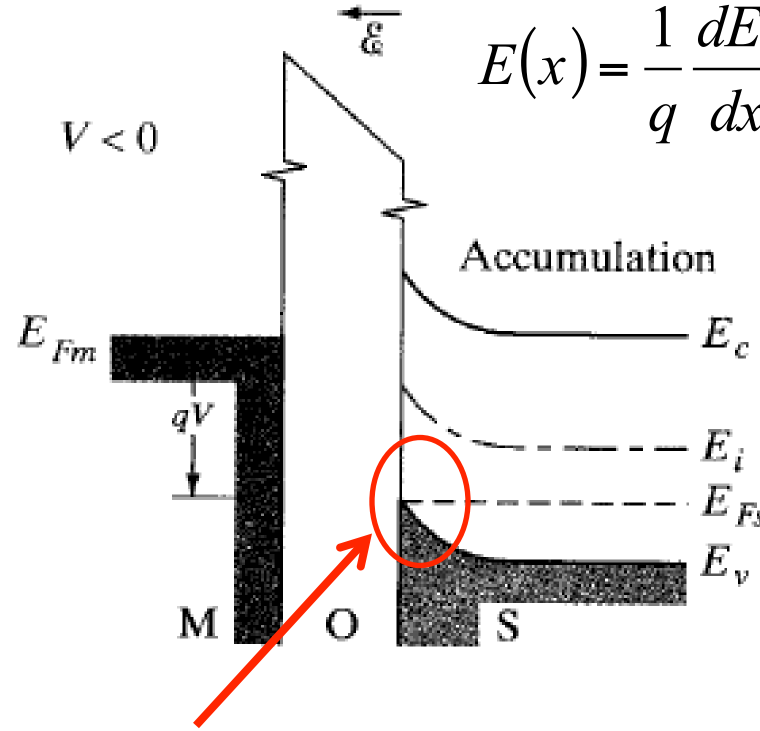


Ideal MOS Capacitor

Let's now apply a **negative gate voltage** to our MOS capacitor…

- Applying a negative gate voltage deposits negative charge on the metal.
- We expect to see this charge compensated by a net positive charge on the semiconductor.
- The applied negative voltage depresses the potential of the metal.
- As a result the electron energies are raised in the metal relative to the semiconductor.
- Moving E_{FM} up causes a tilt in the oxide bands and the semiconductor bands

$$E(x) = \frac{1}{q}\frac{dE_i}{dx}$$



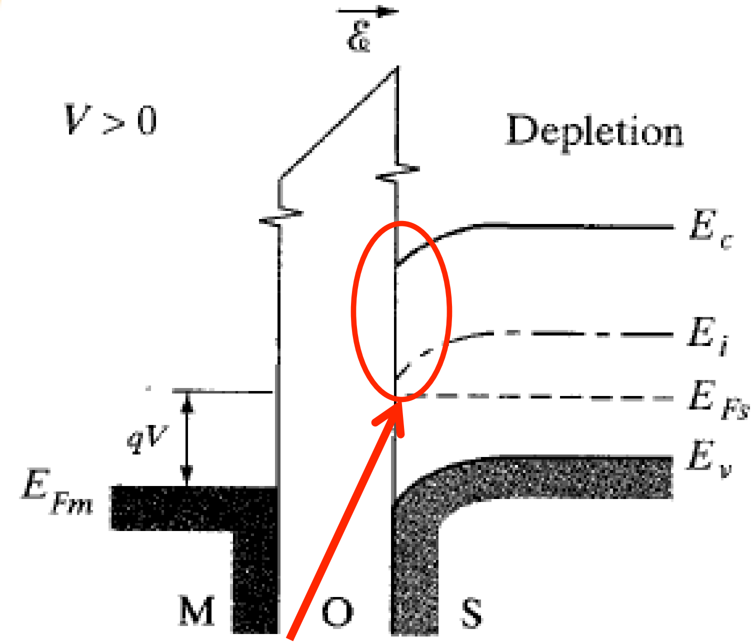
$$p = n_i e^{\frac{E_i - E_F}{k_b T}}$$

More holes accumulate at the surface of the semiconductor.

Ideal MOS Capacitor

Now apply a **positive gate voltage**…

- Deposition of positive charge on the gate requires compensation by negative charges in the semiconductor.
- The negative charge in a p-type semiconductor arises from the depletion of holes from the surface.
- **This leaves behind uncompensated ionized acceptors.**
- The bands bend downward near the semiconductor surface (E_I closer to E_F).



Increased electron concentration

What happens if we keep increasing the amount of positive gate voltage we apply to the metal relative to the semiconductor?

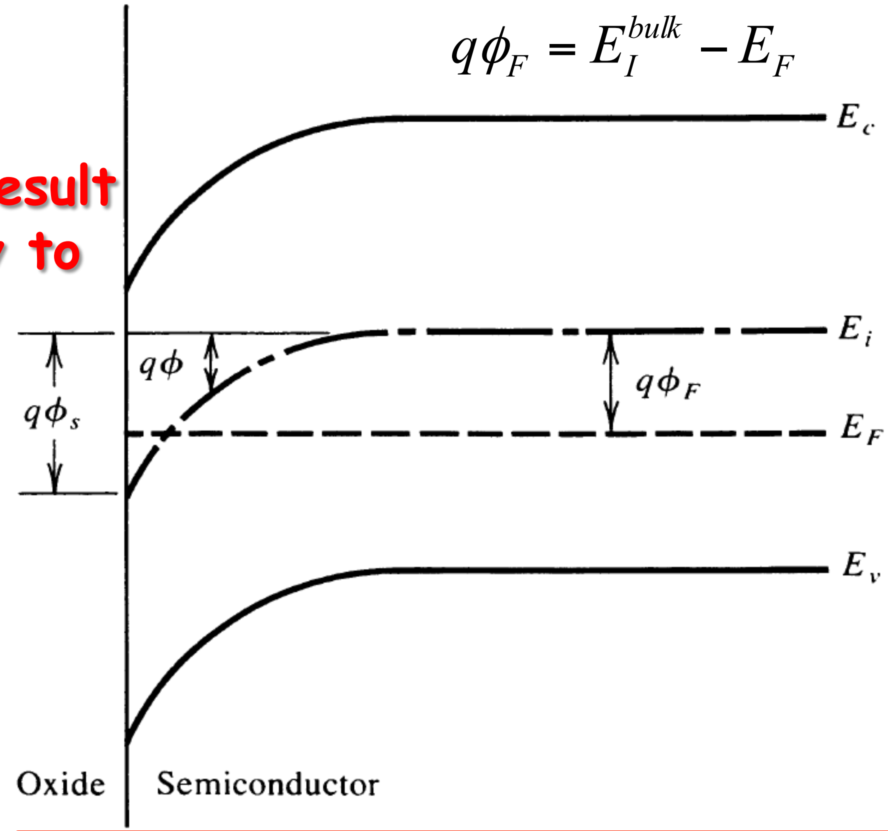
Ideal MOS Capacitor

When V_G is large enough, the surface is **inverted**.

The n-type surface that forms as a result of the applied electric field is the key to transistor operation!

- Define a potential $q\varphi_S$ which determines how much band bending there is at the surface.
- When $q\varphi_S = 0$ we are in flat band condition.
- When $q\varphi_S < 0$ we have hole accumulation at the surface.
- When $q\varphi_S > 0$ we have electron accumulation at the surface.
- When $q\varphi_S > q\varphi_F$ we have inversion at the surface.
- **Surface should be as strongly n-type as the body is p-type.**

$$q\phi_F = E_I^{bulk} - E_F$$



$$\phi_S^{INV} = 2\phi_F = 2\frac{k_bT}{q}\ln\left(\frac{N_A}{n_i}\right)$$

$$\phi_S^{INV} = 2\phi_F = 2\frac{k_bT}{q}\ln\left(\frac{N_D}{n_i}\right)$$

Ideal MOS Capacitor

What other **physical information** can we obtain from this structure?

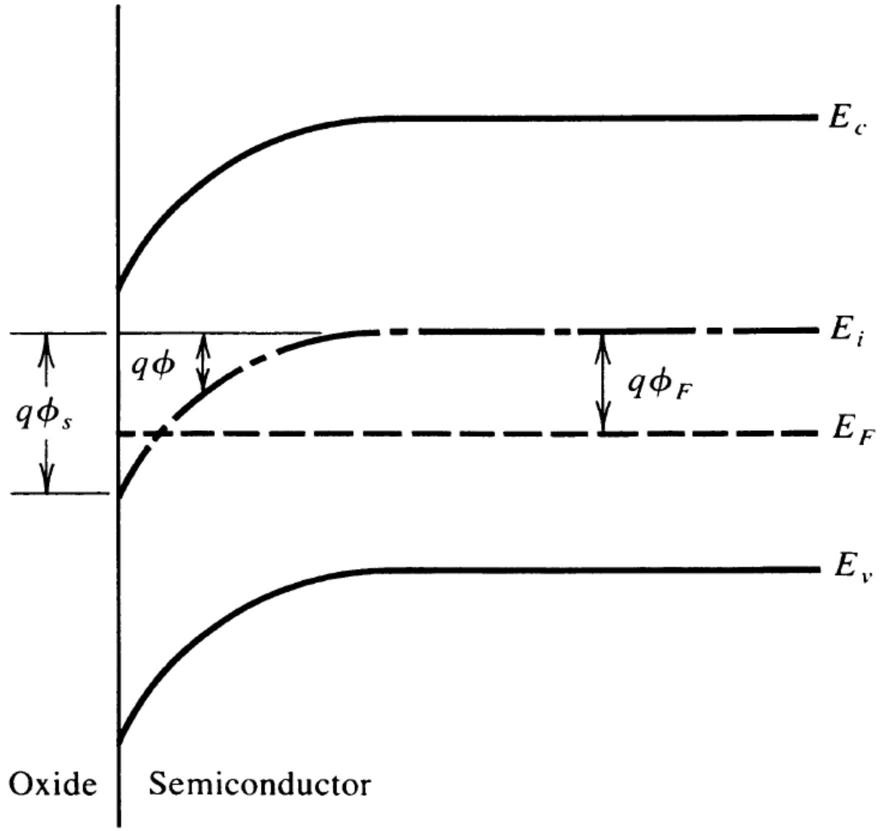
Electron and hole concentrations are related to the potential…

$$n_0 = n_i e^{\frac{E_F - E_I}{k_b T}} = n_i e^{\frac{-q\phi_F}{k_b T}}$$

We then know the electron (hole) concentration at any x…

$$n = n_0 e^{\frac{-q(\phi_F - \phi)}{k_b T}} = n_0 e^{\frac{q\phi}{k_b T}} \quad \text{Electrons}$$

$$p = p_0 e^{\frac{-q\phi}{k_b T}} \quad \text{Holes}$$



But we still need the potential, how do we get it?

$$\frac{\partial^2 \phi}{\partial x^2} = -\frac{\rho(x)}{\epsilon_s} \quad \text{Poisson Equation}$$

Total Charge Density

$$\rho(x) = q(N_d^+ - N_a^- + p - n)$$

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Use Poisson equation and total charge density to get the **total charge**…

Substitute in our knowledge of carrier concentrations and we get…

$$\frac{\partial^2\phi}{\partial x^2} = \frac{\partial}{\partial x}\left(\frac{\partial\phi}{\partial x}\right) = -\frac{q}{\varepsilon_S}\left[p_0\left(e^{\frac{-q\phi}{k_bT}}-1\right)-n_0\left(e^{\frac{q\phi}{k_bT}}-1\right)\right]$$

Electric Field

Integrate from the bulk (where the bands are flat, there are no electric fields, and the doping alone sets the carrier concentrations) towards the surface…

$$\int_0^{\frac{d\phi}{dx}}\left(\frac{\partial\phi}{\partial x}\right)d\left(\frac{\partial\phi}{\partial x}\right) = -\frac{q}{\varepsilon_S}\int_0^{\phi}\left[p_0\left(e^{\frac{-q\phi}{k_bT}}-1\right)-n_0\left(e^{\frac{q\phi}{k_bT}}-1\right)\right]d\phi$$

We now integrate and examine the result at the surface (x = 0) where the perpendicular electric field becomes…

$$\boxed{\mathscr{E}_s = \frac{\sqrt{2}kT}{qL_D}\left[\left(e^{-\frac{q\Phi_s}{kT}}+\frac{q\Phi_s}{kT}-1\right)+\frac{n_0}{p_0}\left(e^{\frac{q\Phi_s}{kT}}-\frac{q\Phi_s}{kT}-1\right)\right]^{\frac{1}{2}}} \qquad \boxed{L_D = \sqrt{\frac{\epsilon_s kT}{q^2 p_0}}}$$

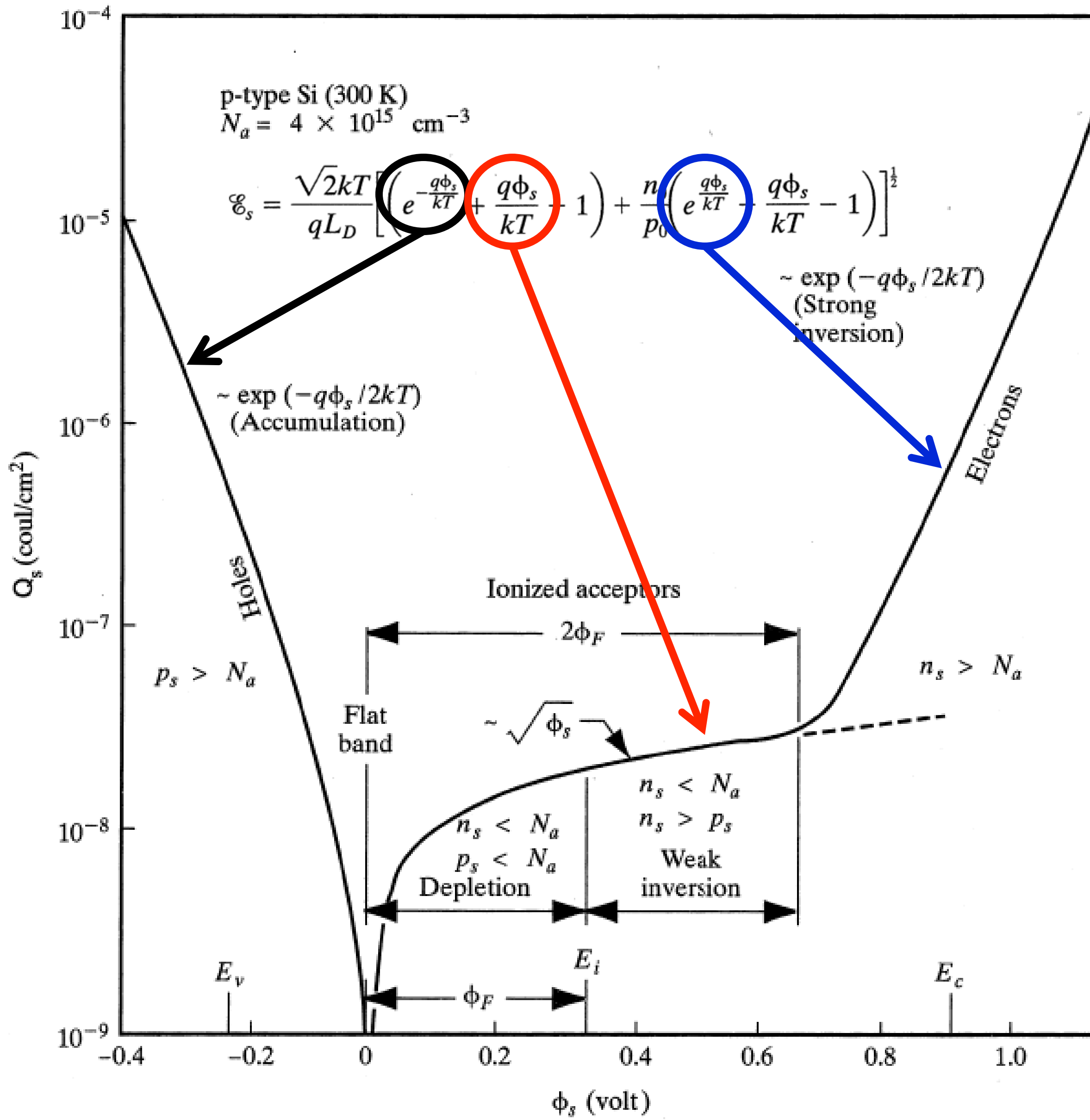
Debye length – distance at which charge fluctuations are screened out to look like neutral entities.

Ideal MOS Capacitor

So what does the **surface charge density** look like?

Use Gauss' Law to find the charge: $Q_s = -\varepsilon_s \xi_s$

- At $\varphi_s = 0$ there is no space charge.
- When φ_s is negative we accumulate majority holes at the surface.
- When φ_s is positive initially the linear term in the electric field solution dominates as a result of the exposed, immobile dopants.
- Depletion extends over several hundred nm until we reach strong inversion and the exponential field term dominates.



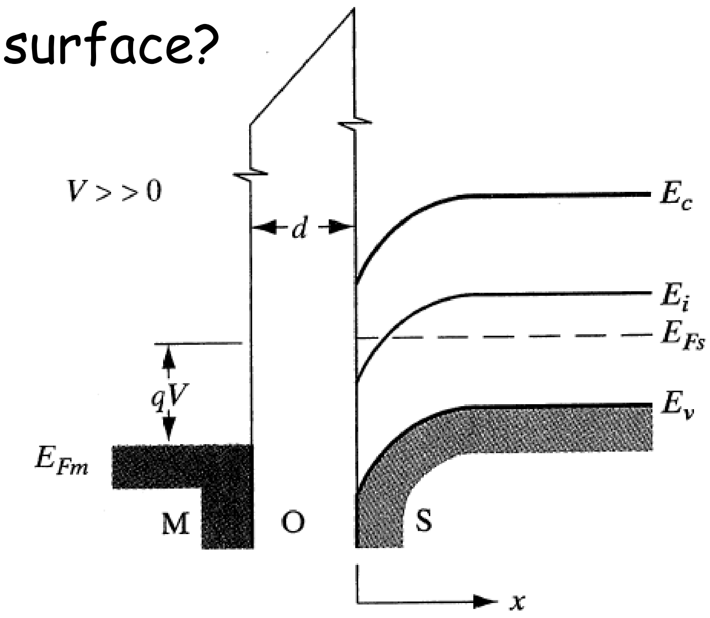
Ideal MOS Capacitor

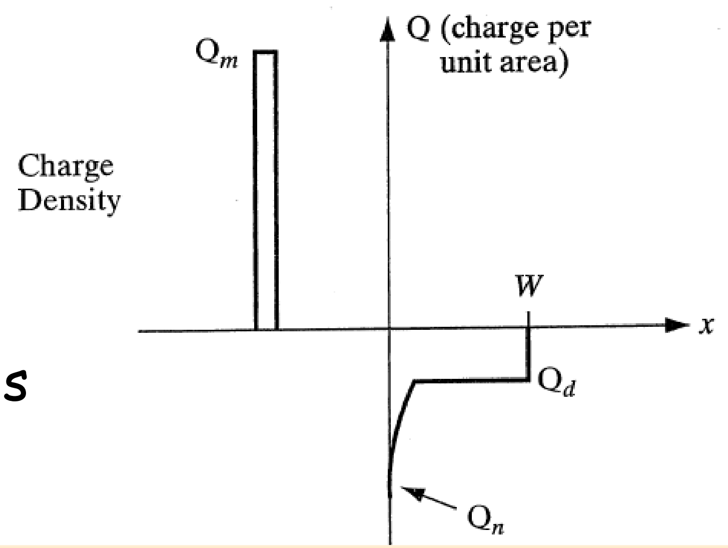
What is the charge distribution on an inverted surface?

- For simplicity, let's assume complete depletion for 0 < x < W and neutral material for x > W.
- Charge due to uncompensated acceptors is $-qN_aW$.
- **Positive charge on the metal Q_M is balanced by negative charge Q_S in the semiconductor which is the depletion layer charge plus the charge due to the inversion region Q_N.**

$$Q_M = -Q_S = qN_aW - Q_N$$

The depletion width here is exaggerated and is typically only on the order of 10 nm.





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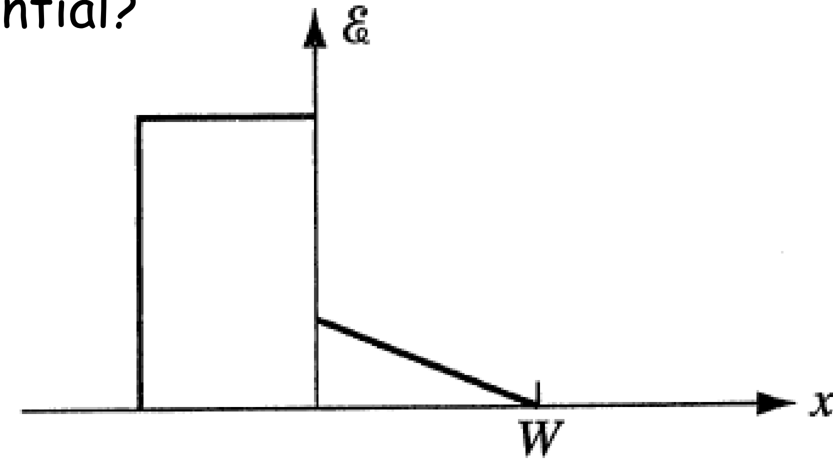
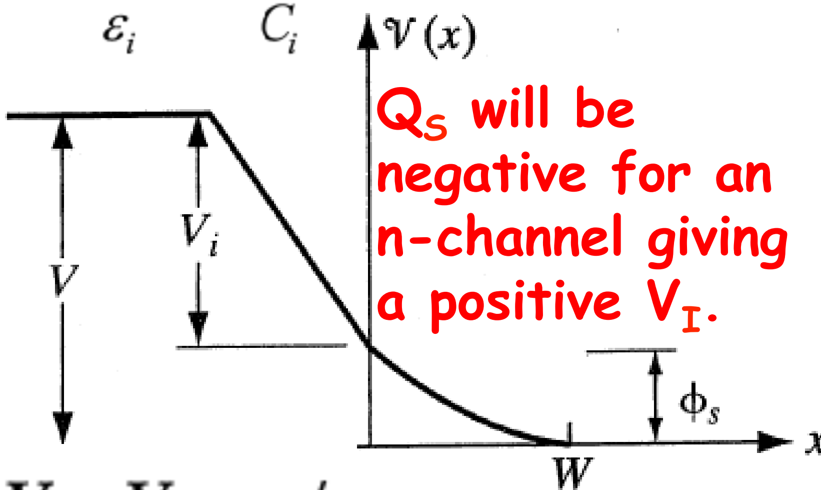
What about the electric field and the potential?



- The electric field does not penetrate the metal.
- It is constant across the oxide as there are no charges or impurities in the oxide.
- The electric field in the semiconductor drops linearly, as we would expect.

$$V_i = \frac{-Q_s d}{\varepsilon_i} = \frac{-Q_s}{C_i}$$

- The potential is constant in the metal.
- It is drops linearly across the oxide (V_I).
- The potential is also dropped across the depletion region of the semiconductor, φ_S.



$$V = V_i + \phi_s$$

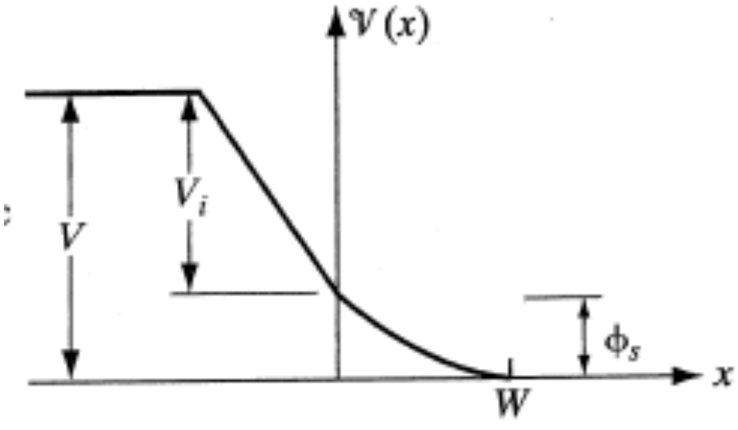
Ideal MOS Capacitor

Let's explore the **depletion region** more…

From considerations based on other systems (p-n junction), we can use the depletion approximation to show that…

$$W = \left[\frac{2\varepsilon_s \phi_s}{qN_a}\right]^{1/2}$$

Length of depletion region



The depletion region grows with voltage until strong inversion is reached. So what is the maximum value of the depletion width?

$$\boxed{W_m = \left[\frac{2\varepsilon_s \phi_s(inv.)}{qN_a}\right]^{1/2} = 2\left[\frac{\varepsilon_s kT \ln(N_a / n_i)}{q^2 N_a}\right]^{1/2}}$$

Which must be driven by an applied voltage. The applied voltage required for strong inversion is…

$$\boxed{V_T = -\frac{Q_d}{C_i} + 2\phi_F}$$

Assumes negative charge at surface is due to depletion charge.

And the charge in the depletion region at strong inversion.

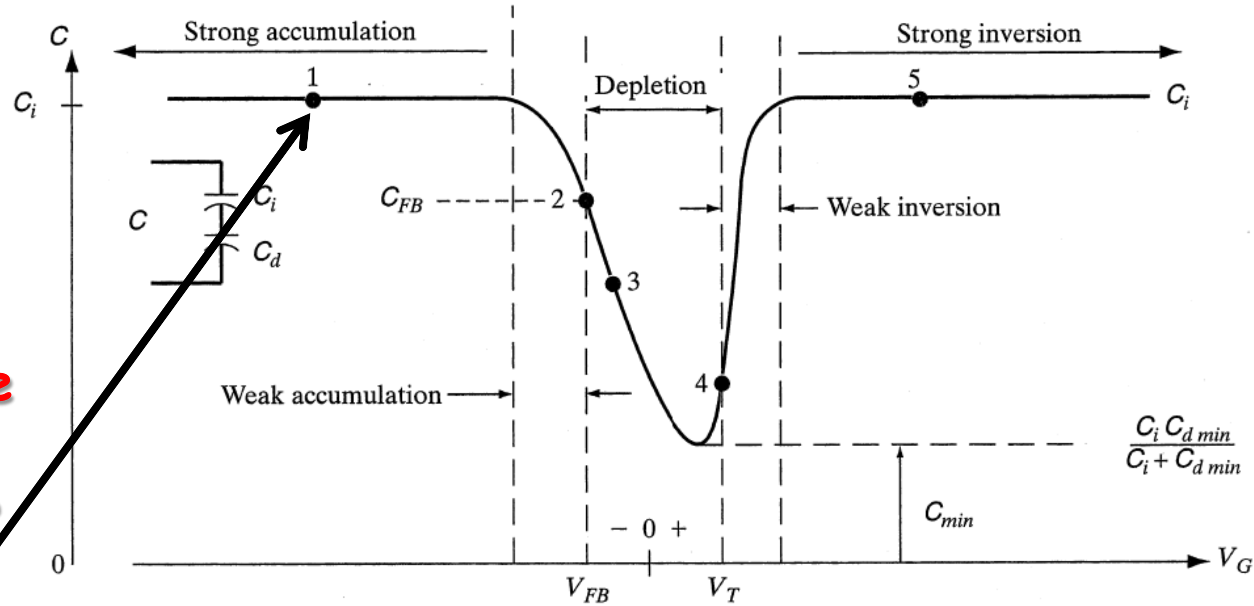
$$\boxed{Q_d = -qN_a W_m = -2(\varepsilon_s qN_a \phi_F)^{1/2}}$$

What about the **capacitance** of our structure?

The **capacitance** depends on the voltage…

$$C_s = \frac{dQ}{dV} = \frac{dQ_s}{d\phi_s}$$

MOS Capacitor is the **series combination of the oxide and the voltage dependent semiconductor capacitances**.



In accumulation:

- The capacitance is huge.
- Structure acts like a parallel plate capacitor piling holes up at the surface. $C_i = \varepsilon_i / d$

Ideal MOS Capacitor

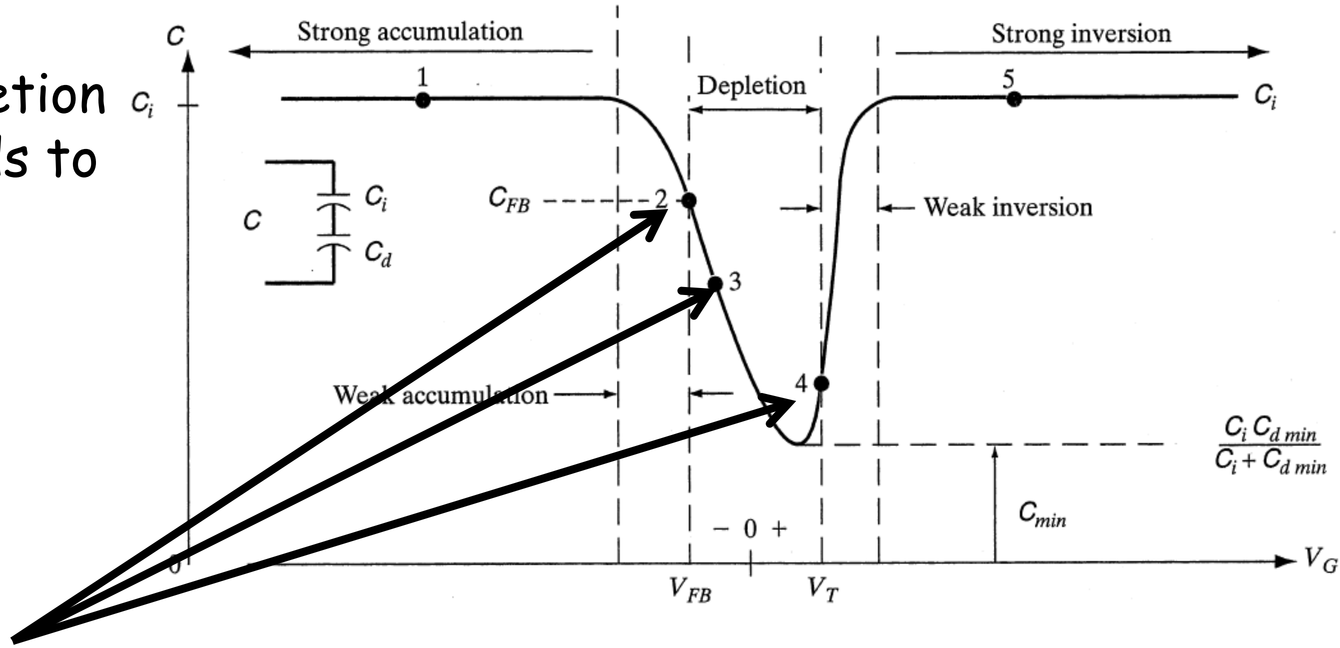
Start increasing the voltage across the capacitor…

The surface becomes depleted and the depletion layer capacitance needs to be added in…

$$C_d = \varepsilon_s / W$$

Total capacitance:

$$C = \frac{C_i C_d}{C_i + C_d}$$



In depletion:

- Capacitance decreases as W grows until inversion is reached.
- Charge in depletion layer of MOS capacitor increases as ~ $(\varphi_S)^{1/2}$ so depletion capacitance decreases as the inverse.
- **If signal applied to make measurement is too fast, inversion layer carriers can't respond and do not contribute.**
- Slowly varying signals allow time for minority carriers to be generated, drift across depletion region, or recombine.
- Majority carriers in the accumulation region respond much faster.