UDC 669 . 782 : 621 . 3 . 049 . 77 : 539 . 219

Influence of Metallic Contamination on LSI Fabrication

Makoto TAKIYAMA*1

Abstract

This paper outlines the influences of metallic contamination on the fabrication of LSI: Initially, the impact of wafer quality on the fabrication yield of LSI and how metallic contamination should be viewed are discussed; then, specific details of their adverse effects are considered. The adverse effects on the LSI quality are divided into abnormity in LSI shapes and deviation in their electrical characteristics. The degree and type of the effects are different depending on the kind of metallic impurity and the occasion of contamination, because they are determined by the solid solubility, diffusibility and reactivity of the contaminant metals with silicon. Three areas are proposed herein where wafer vendors could contribute to solving the metallic contamination problem, besides improving the wafer surface cleanness: development of high performance gettering technologies, amplification of fundamental databases and enhancement of consulting capability.

1. Introduction

The bottom of the silicon cycle that Japan suffered in 1997 after the peak of 4 Mega-DRAMs production was different from similar events in the past. For one thing, Japan lost price competitiveness in its main products, DRAM, due to its heavy overhead cost as Korea and Taiwan made serious efforts to launch[ed] their semiconductor business: The Japanese tax system is somewhat different from that of those two countries. However, the cost for manufacturing the Japanese DRAM is not so different from the cost in those two countries. Another reason is that Japanese LSI manufacturers found it difficult to continue their DRAM business on their own in view of increasing facilities, equipment, and technology development investment that come from the increase in wafer size, and the hesitated to make the necessary investment. Japan's leading LSI manufacturers slimmed down and drastically cut costs to maintain their price competitiveness, added value to their products by anticipating technical trends, or they diversified into niche markets. They were also forced to switch their main product line from DRAMS to system LSI.

The switch in the main product line transferred manpower from "manufacturing technology" to "design technology", and changed the nature of LSI production from "manufacturing" to "service" or from "how to manufacture" to "what to manufacture". Technical trends were anticipated despite this manpower transfer, so out-sourcing was increasingly relied upon for non-core product manufacturing technology. Further, mixed-flow production was adopted as a prerequisite for the total cost reduction, and the awareness that "a manufacturing yield of 100% was natural" was enhanced, therefore no factors were allowed that would cause the quality fluctuations of individual LSI devices. As a result, wafer vendors were demanded:

(1) To promote the cost reduction of silicon wafers (to the lowest possible level);
(2) To promote the quality up of silicon wafers (elimination of any factors to cause LSI manufacturing yield loss); and
(3) To strengthen the cooperative relationship with users (in every possible area).

One example is the 64Mega-DRAM. About 300 chips could be fabricated on one 8-inch wafer (as of 1999). Assuming that the yield loss due to wafer quality fluctuations is 1% and the chip unit price is ¥1,000 (average price as of 1999), the LSI manufacturer suffers a profit loss of ¥3,000 per wafer, depending on the quality of wafers. If the purchase price of 8-inch wafers is ¥9,000 per wafer (average price as of 1999) and the average wafer input per line is 20,000 wa-

*1 NSC ELECTRON CORPORATION, presently Wacker NSCE Corp.

fers/month, the effect of a wafer vendor selection mistake on the profit of the LSI manufacturer amounts to near ¥1 billion/year per line.

Because wafer vendors increased in number after 1987, wafers were always in excess supply except for some periods of time, and LSI manufacturers were free to select their wafer vendors. To ensure their profits, wafer vendors continued to sell wafers at too low prices, to enhance the quality of wafers to an excessive level, or to extend excessive technical service to customers. The aforementioned change in the LSI manufacturing environment then prompted these tendencies further. As the technologies to improve the quality fluctuations of wafers lie scattered in the elemental technologies of wafer manufacture, the problem of metallic contamination described herein is common to the elemental technologies of both wafer and LSI manufacture, and is intimately related to the requirements of (2) and (3) discussed above.

2. Adverse Effects of Metallic Contamination

2.1 Metallic contamination in LSI manufacture

The National Technology Roadmap for Semiconductors (NTRS), 1997 Edition, published by the Semiconductor Industry Association (SIA) of the United States, is excerpted in **Table 1**[1,2]. The latest LSI design rule is shrinking to 0.15-μm. Beyond 0.10-μm generation, the minimum fabrication dimension by using self-alignment technologies will be 0.05 μm or less, and it will not be so difficult to count the atoms present in such fabrication features as lines, trenches, and holes. Since LSI circuits are patterned on the wafer surface by photo-lithography technique, such surplus surface irregularities as to obstruct light interference cause short or open of LSI circuits and it induces yield loss. Because atomic-level fabrication control is demanded of LSI manufacture, the silicon wafer surface that serves as the LSI substrate must be flat, both macroscopically and microscopically, to obtain optimum fabrication shapes of LSI pattern.

LSI stands for a large-scale integration of transistors. In the 0.1-μm generation, the atoms that appear on the transistor gate surface are a mere 10 million or so. To eliminate the electrical property fluctuations of transistors, the presence of substances not considered in the LSI design phase is not allowed. So the minimum requirement imposed on the silicon wafers is the assurance of no fabrication shape and electrical property anomalies on the LSI chips that become end products. Metallic contamination is one factor that hampers this minimum requirement.

"Metallic contamination" means that the silicon wafer has been unintentionally contaminated with metallic impurities. It is classified into bulk contamination determined in the growth process of silicon single crystal ingots and surface contamination of wafers in the fabrication and subsequent process. At present, these two types of metallic contamination are generally controlled about 1E10 atoms/cm^3 and 1E09 to 3E10 atoms/cm^2, respectively. Because the wafer thickness is about 600 to 700 μm, the metallic contamination is predominated by the surface contamination, so it becomes a problem for both wafer vendors and users.

About ten metallic impurities to be monitored are common surface contaminants for the wafer vendors; such as Al, Cr, Cu, Fe, Ni, and Zn as contaminants from semiconductor manufacturing equipment; Ca, K and Na as contaminants from the human body and other sources; and Mo as contaminant from the deposition of silicon epitaxial layer. Co, Mn, Ta, Ti, and W are also controlled when user applies various materials in their manufacture.

2.2 Wafer surface anomalies caused by metallic contamination[3,4,5]

Surface microscopic flatness anomalies that cause fabrication shape anomalies of LSI appear when metallic impurities adhering to wafers go through the wet-cleaning and the following annealing processes. These anomalies are mainly classified into the following types: mounds, cave-ins, hazing, pits, dendrites, and whiskers.

Mounds, cave-ins, and hazing appear after annealing is induced by volume changes caused by such factors as chemical reaction between contaminant metals and silicon (silicide reaction), chemical reaction between contaminant metals and silicon dioxide (SiO_2) (silicate reaction), and lowering the localized glass transition temperature based on dissolution of metals in the SiO_2 layer.

Pits occur in both of the wet-cleaning and annealing processes.

Table 1 Excerpts from National Technology Roadmap for Semiconductors 1997

Starting materials technology requirements								
1	Year of first product shipment	1997	1999	2001	2003	2006	2009	2012
	technology generation	250nm	180nm	150nm	130nm	100nm	70nm	50nm
2	Wafer diameter (mm)	200	300	300	300	300	450	450
3	Critical surface metals*1 (atoms/cm^2)	2.5E+10	1.3E+10	1.0E+10	7.5E+09	5.0E+09	2.5E+09	2.5E+09
4	Other surface metals*2 (atoms/cm^2)	1.0E+11	1.0E+11	1.0E+11	1.0E+11	1.0E+11	1.0E+11	1.0E+11
5	Total bulk Fe*3 (atoms/cm^3)	3E+10	1E+10	1E+10	< 1E+10	< 1E+10	< 1E+10	< 1E+10
6	Recombination lifetime (μs)	300	325	325	325	325	450	450
Surface preparation technology requirements								
	Front end of line							
7	Critical metals*4 (atoms/cm^2)	5.0E+09	4.0E+09	3.0E+09	2.0E+09	1.0E+09	< 1E+09	< 1E+09
8	Other metals*5 (atoms/cm^2)	5.0E+10	2.5E+10	2.0E+10	1.5E+10	1.0E+10	5.0E+09	< 5E+09
	Back end of line							
9	Metals*6 (atoms/cm^2)	1.0E+11	5.0E+10	4.0E+10	2.0E+10	1.0E+10	< 1E+09	< 1E+09

*1 Ca, Co, Cr, Cu, Fe, K, Mn, Mo, Na, and Ni
*2 Al, Ti, V, and Zn
*3 Bulk Fe concentration in silicon wafers
*4 W as well as metals*1
*5 Ba, Sr, and Ta if present in the factory as well as metals*2
*6 K, Li, and Na

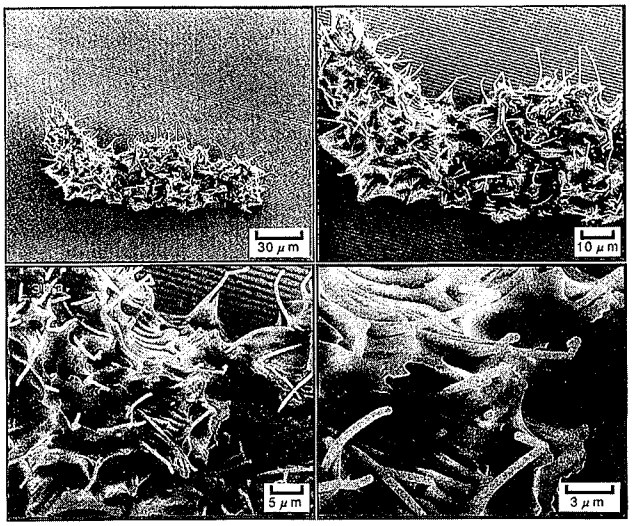

Photo 1 Scanning Electron microscopy images of whiskers induced by metallic contamination in CVD process

In the cleaning process, noble metals, such as Au, Ag, Cu and Pt, have reaction electrochemically, with the silicon wafer surface as electrode in a diluted hydrofluoric acid solution; oxidation of Si and dissolution of the SiO_2 layer by the diluted hydrofluoric acid solution are repeated electrochemically, and pits form at the surface. The width and depth of them are less than 30 nm. In the annealing process, the SiO_2 layer formed for LSI manufacture catalytically reacts with the metallic contaminants during annealing in a ambient of very low oxygen partial pressure (e.g., nitrogen, argon, or vacuum). This catalytic reaction decomposes and sublimes SiO_2 ($SiO_2 + Si \rightarrow 2SiO$), and forms pits. Ca, Fe, Mg, and Sr facilitate the formation. The size of the pits depends on the contamination level, and sometimes exceeds a few micrometers.

Dendrites and whiskers are formed on the SiO_2 layer by the catalytic reaction of metallic impurities. The results of experiments with wafers intentionally contaminated with metallic impurities show that dendrites and whiskers appear when metal oxides locally concentrate in the oxide layer during annealing in an ambient of low oxygen partial pressure (nitrogen, argon, or vacuum). They sometimes coexist with the above-mentioned pits. Fe, Mn, and Ti facilitate the formation of the dendrites and whiskers.

Obstruction of LSI manufacture by these surface microscopic anomalies is plainly shown in **Photo 1**[4]. It is clear that dendrites and whiskers grown in the chemical vapor deposition (CVD) process obstruct the formation of an interconnect pattern and caused their loss, and disabled the normal operation of the circuits.

2.3 Electrical property anomalies caused by metallic contamination[5-7]

Electrical property anomalies may be classified into two main types. One type is caused by fabrication shape abnormality of transistors, which in turn is caused by a microscopic flatness abnormality of a silicon wafer. The other is caused by metallic contaminants that is dissolved and diffused in the transistor structure. The electrical property anomalies caused by former type appear as remarkable anomalies, including circuit shorts and opens, and transistor structure anomalies. The electrical property anomalies of the latter type are not always detected by various in-line inspection equipment, and are mainly detected when LSI are tested for electrical properties before shipment. The former anomalies are generally eliminated relatively early at the start of mass-production, and the latter anomalies remain problematic late in the LSI manufacturing process.

Table 2 Summary of LSI characteristic anomalies due to metallic contamination

Anomaly of LSI characteristics	Crystal defects	Particle contamination	Metallic contamination
Photo-lithography anomaly Microfabrication shape anomaly	○	○	○
Film deposition anomaly Product visual inspection anomaly	○	○	○
Film deposition monitor anomaly Monitor visual inspection anomaly	○	○	○
Threshold voltage deviation Hot electron resistance lowering	(○)	—	○
Gate oxide integrity degradation Capacitor leakage increasing	○	—	○
Mobility lowering Density of interface level increasing	(○)	—	○
Standby leakage increasing Junction leakage increasing	○	—	○
Retention-time failure Disturb failure	(○)	—	○
Field isolation failure	○	—	○
Sheet resistance increasing Contact resistance increasing	(○)	—	○
Interconnect reliability deterioration	—	○	○

○ : Applicable (○) : Probably applicable — : Not applicable

The types of LSI property anomalies due to metallic contamination, among other factors, are summarized in **Table 2**. When metallic impurities diffuse into the bulk of the wafer, they cause the mis-operation of LSI. For example, the standby leakage current of transistors increases, the electrical insulation between adjacent transistors is not maintained, or the charges accumulated in capacitors are lost. When metallic impurities do not diffuse into the bulk of the wafer but remain on the surface of the wafer, they degrade the dielectric breakdown voltage of the SiO_2 layer used as the gate dielectric film of transistors, cause the electrical failure of transistors, or become surplus positive charge to induce the mis-operation of transistors.

The level to which the respective metallic impurities cause the aforementioned electrical property anomalies greatly depends on their physical properties; more concretely, solubility and diffusivity in silicon, chemical reactivity on the silicon surface, saturation vapor pressure, standard formation enthalpy of metal oxides, and impurity levels in the band-gap of silicon. Co, Cu, Fe, Mn and Ni with relatively large solubility and diffusivity in silicon are likely to cause stand-by leakage current anomalies, while Al, Ca, Ta, Ti, and Zn with smaller solubility and diffusivity degrade the dielectric breakdown strength of the gate oxide. K and Na act as positive charge carriers in the SiO_2 layer and shift the transistor operating voltage to a maximum of about 40 V. On the other hand, Cr is likely to sublimate during annealing and does not adversely affect electrical properties unless present in a large amount on the wafer surface.

2.4 Effect of metallic contamination on manufacturing throughput[8]

Besides the surface microscopic flatness and electrical property

anomalies discussed above, metallic contamination may also exert an adverse effect on the throughput of LSI manufacturing factories. LSI are manufactured through 250 to 300 process steps, 30 to 50% of which are concerned with film deposition or thermal treatment. To confirm that product lots are normally treated through a given process step, process monitor wafers are input into the step at the start of production. After the end of processing through the step, film thickness, haze, particle count, and so on are measured by using the process monitor wafer, and the results are used to guarantee the quality of wafers processed through the step. The metallic contamination on these process wafers causes the above-mentioned surface anomalies, which are recognized as lot anomalies and manufacturing equipment trouble. Until the causes of these anomalies are identified, manufacturing equipment trouble is resolved, or necessary measures are taken against them, the lot concerned is withheld and the equipment is stopped. T[t]herefore, if monitor wafers alone are contaminated with metals, the throughput of the LSI manufacturing equipment is reduced.

3. LSI Manufacturing Technology Trend and Allowance of Metallic Contamination Level[1, 2, 9)]

To what level should the amount of metal contamination be reduced? The allowance levels of metallic contamination in the NTRS are given in Table 1. The NTRS uses the number of metallic impurity atoms per unit wafer area as the unit of metallic contamination, and presents the amount of metal impurities on the silicon wafers in the shipment stage and the amount of metallic impurities left on the silicon wafers after cleaning for two groups of metallic impurities. From the results of experiments done by researchers in Japan and abroad, it is commonly recognized that various anomalies start to appear when the amount of metallic impurities on the wafer surface over 1E11 atoms/cm^2 and that the metallic impurities are acceptable if their amount is less than 1E10 atoms/cm^2. These values almost agree with those of the NTRS, and it is general to refer to the NTRS for the metallic contamination requirements.

When considering the trend in LSI manufacturing technology, it is obvious that improvement in wafer surface cleanliness is indispensable[10)]. The trend in LSI performance is toward higher speed and lower power. These conditions are maintained by the reduction in the delay-time of circuit. Because the LSI shrinkage nears its physical limitation, interconnect wiring materials of lower resistivity and inter-layer dielectric materials of lower dielectric constant start to be used for improving the delay-time. So the heat resistance of these materials is not high enough, LSI will be manufactured in shorter time at lower temperature.

When this trend is seen from the view point of metallic contamination, it may be summarized that there is the possibility of silicon wafers being contaminated with metallic impurities inexperienced to date and that metallic impurities are likely to remain on the wafer surface without dissolving and diffusing and to adversely affect the silicon wafer surface. Wafer surface cleanliness at the time of shipment now meets the NTRS, but unless their amount is reduced below that specified in the NTRS, residual metallic impurities are feared to adversely affect the manufacturing of LSI.

4. What Can Wafer Vendors Do?

It was mentioned at the beginning this paper that wafer vendors must contribute to their users or LSI manufacturers as the LSI manufacturing environment is undergoing a sea change. Needless to say, the largest contribution that could be made is to improve the surface cleanliness of silicon wafers we ship to the LSI manufacturers. As far as the issue of metallic contamination is concerned, there are three additional contributions we could possibly make.

The first is to develop highly effective gettering technology. Because the gettering technology is discussed in detail in other articles in this issue of the NSTR, descriptions are omitted here. The development of gettering technology rendering contaminant metals harmless even in a low-temperature, short-time thermal treatment process is the largest contribution to satisfy LSI manufacturers.

The second is to expand a basic database concerning metallic contamination. By what metals are silicon wafers contaminated? What phenomena is silicon wafers suffered in a given thermal treatment? What correlation does the level of degradation in various electrical properties of LSI have with the amount of metallic contamination? At what level should the allowance amount of metallic contamination determine by considering these results? We could contribute to the LSI manufactures in their measures to solve the problem of metallic contamination by putting these items of information into a database.

The last is to provide users with the consulting service to help them solve metallic contamination troubles on their own fabs. If the user has a full understanding of the characteristics of various metallic contamination on the basis of the above-mentioned database, it is not difficult to identify the target contaminant and the process step where the trouble has occurred from the features of the contamination. Wacker NSCE Corporation is already providing its customers with consultation free of charge under the slogan "Silicon Solution Provider", and more effective contribution is able by enriching its consultation service.

Some people may think wafer wet-cleaning technology development as another contribution for wafer vendors to make to LSI manufacturers. Because the LSI manufacturing process imposes many cleaning technology constraints, build-up of an unified wet-cleaning technology is hopeless. Wafer vendors with a poor knowledge about the LSI manufacturing processes have to find it difficult to make any meaningful contribution. So the contribution we could make in this technology field should be focus to enhancement of wafer surface cleanliness in the shipment stage. Therefore, proposal of wafer cleaning technology is considered difficult as a contribution by wafer vendors.

5. Conclusions

The need for shrinkage of LSI and increasing the circuit integration of LSI knows no limits. Despite the fact that the physical limitation nears closely, the speed of technology development continues to accelerate. The effects of any slowdown in the LSI manufacturing technology may have on the overall industry and economy are immeasurable. There are limits to the resources the industry can invest. To avoid an eventual catastrophe, the LSI industry must think about efficiency enhancement and information control about LSI manufacture and peripheral technology development. This calls for the framework where LSI manufacturers and wafer vendors can build a cooperative relationship. Metallic contamination and chemical contamiation[11)] are considered as suitable subjects to tackle together in cooperation.

References

1) Semiconductor Industry Association : The National Technology Roadmap for Semiconductor. America, 1997
2) Takiyama, M.: The Status Quo of Contamination in ULSI Manufacturing. Edited by Ajioka, Ikeno, Yabumoto, REALIZE Inc., 1999, p.161-

170
3) Takiyama, M.: Ultra-precise Surface Control Technology in Silicon Wafer. Edited by Matsusita, Hukaya, Tsuya, Takasu, Science Forum, 2000, p.26-35
4) Takiyama, M.: Clean Technology. 8(5), 39(1998)
5) Takiyama, M.: Ultraclean Surface Processing of Silicon Wafers. Second Edition. Edited by Hattori, T., REALIZE Inc., 2000, Chapter 3-5
6) Takiyama, M.: Ultraclean Surface Processing of Silicon Wafers. Edited by Kasiwagi, M. Hattori, T., REALIZE Inc., 1995, p.24-30
7) Takiyama, M.: The Status Quo of Contamination in ULSI Manufacturing. Edited by Ajioka, Ikeno, Yabumoto, REALIZE Inc., 1999, p.255-272
8) Takiyama, Mizukami, Tanahasi : Extended Abstracts, The 47th Annual meeting, The Japan Society of Applied Physics, 28p-YH-14, 2000-03
9) Takiyama, M.: The Status Quo of Contamination in ULSI Manufacturing. Edited by Ajioka, Ikeno, Yabumoto, REALIZE Inc., 1999, p.181-195
10) Takiyama, M.: Handbook of Amorphous Silica Materials Application. Edited by Kawazoe, Awazu, Ohki, Kuzuu, Todoroki, Hayashi, Hukuda. REALIZE Inc., 1999, p.379-416
11) Takiyama, M.: The Status Quo of Contamination in ULSI Manufacturing. Edited by Ajioka, Ikeno, Yabumoto, REALIZE Inc., 1999, p.374-388