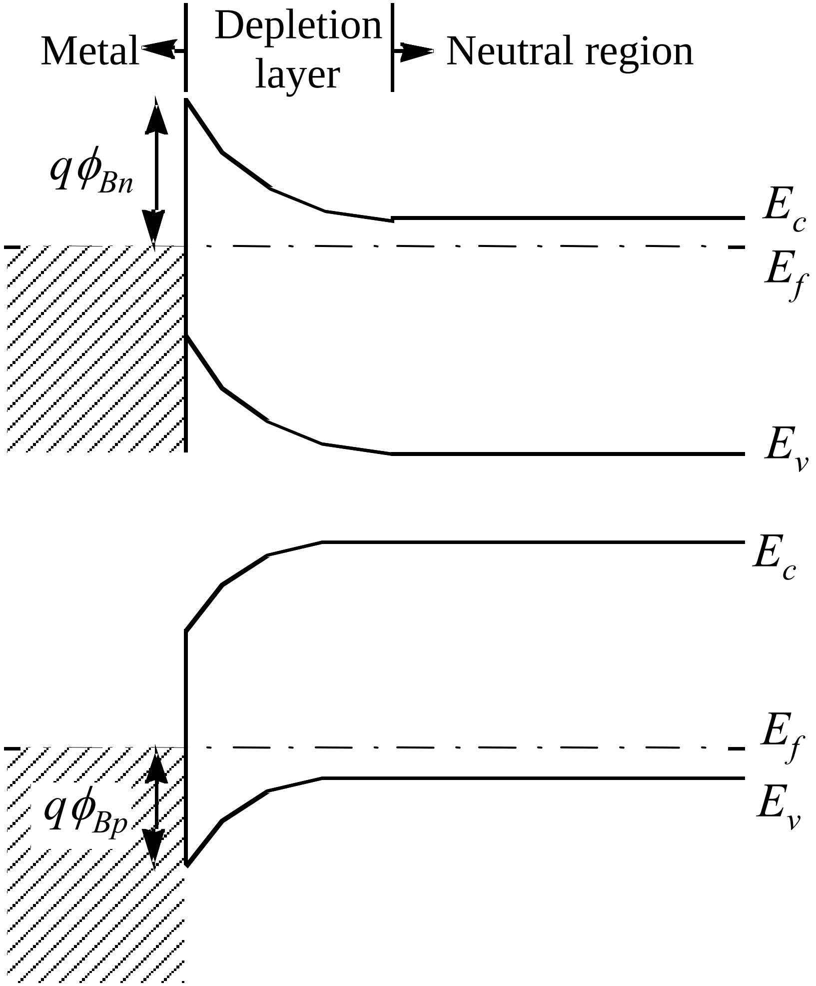
Chapter 9 Metal-Semiconductor Contacts

Two kinds of metal-semiconductor contacts:

- *metal on lightly doped silicon –*
- *rectifying* ***Schottky diodes***
- *metal on heavily doped silicon –*
- *low-resistance* ***ohmic contacts***

9.1 Schottky Barriers

Energy Band Diagram of Schottky Contact



- Schottky barrier height, ϕ_B, is a function of the metal material.

- ϕ_B is the single most important parameter. The sum of $q\phi_{Bn}$ and $q\phi_{Bp}$ is equal to E_g.

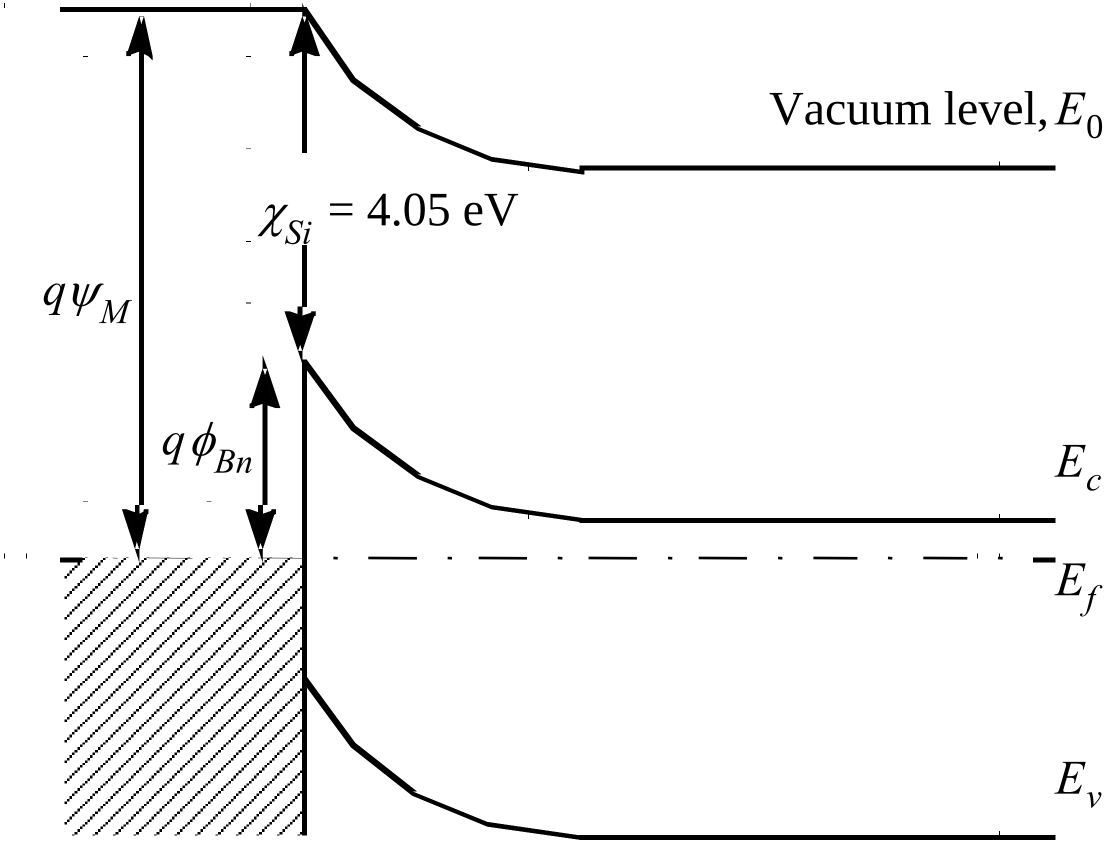
Schottky barrier heights for electrons and holes

Metal	Mg	Ti	Cr	W	Mo	Pd	Au	Pt
ϕ_{Bn} (V)	0.4	0.5	0.61	0.67	0.68	0.77	0.8	0.9
ϕ_{Bp} (V)		0.61	0.5		0.42		0.3	
Work Function ψ_m (V)	3.7	4.3	4.5	4.6	4.6	5.1	5.1	5.7

$$\phi_{Bn} + \phi_{Bp} \approx 1.1\ \text{V}$$

ϕ_{Bn} increases with increasing metal work function

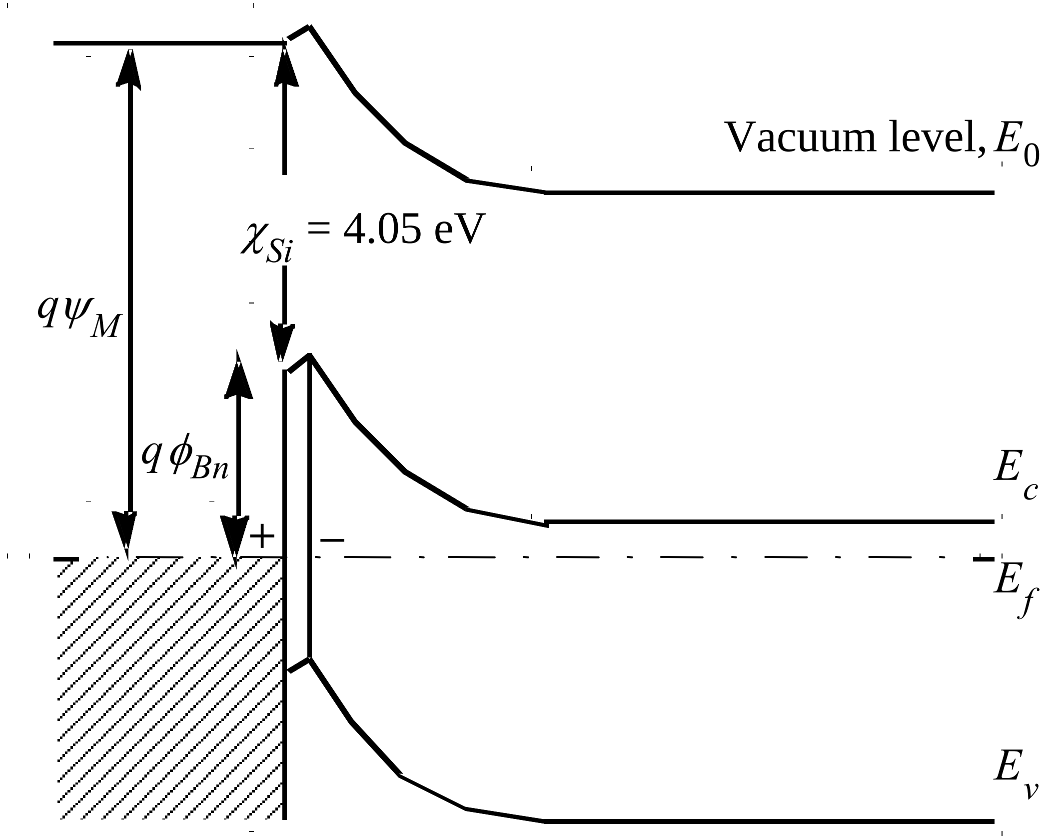
ϕ_{Bn} Increases with Increasing Metal Work Function



Ideally,

$$q\phi_{Bn} = q\psi_M - \chi_{Si}$$

ϕ_{Bn} *is typically 0.4 to 0.9 V*



- A high density of energy states in the bandgap at the metal-semiconductor interface pins E_f to a range of 0.4 eV to 0.9 eV below E_c

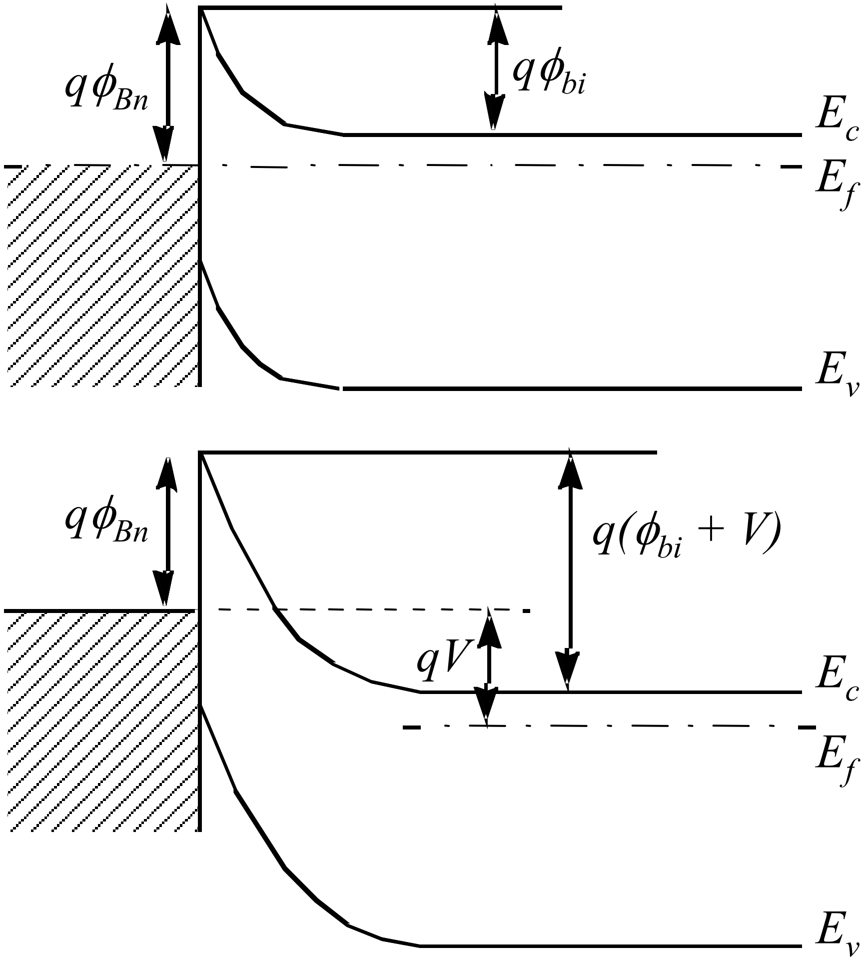
- ***Question***: What is the typical range of ϕ_{Bp}?

Schottky barrier heights of metal silicide on Si

Silicide	$ErSi_{1.7}$	HfSi	$MoSi_2$	$ZrSi_2$	$TiSi_2$	$CoSi_2$	WSi_2	$NiSi_2$	Pd_2Si	PtSi
ϕ_{Bn} (V)	0.28	0.45	0.55	0.55	0.61	0.65	0.67	0.67	0.75	0.87
ϕ_{Bp} (V)			0.55	0.49	0.45	0.45	0.43	0.43	0.35	0.23

Silicide-Si interfaces are more stable than metal-silicon interfaces. After metal is deposited on Si, an annealing step is applied to form a silicide-Si contact. The term ***metal-silicon contact*** includes silicide-Si contacts.

Using CV Data to Determine ϕ_B



$$q\phi_{bi} = q\phi_{Bn} - (E_c - E_f)$$

$$= q\phi_{Bn} - kT\ln\frac{N_c}{N_d}$$

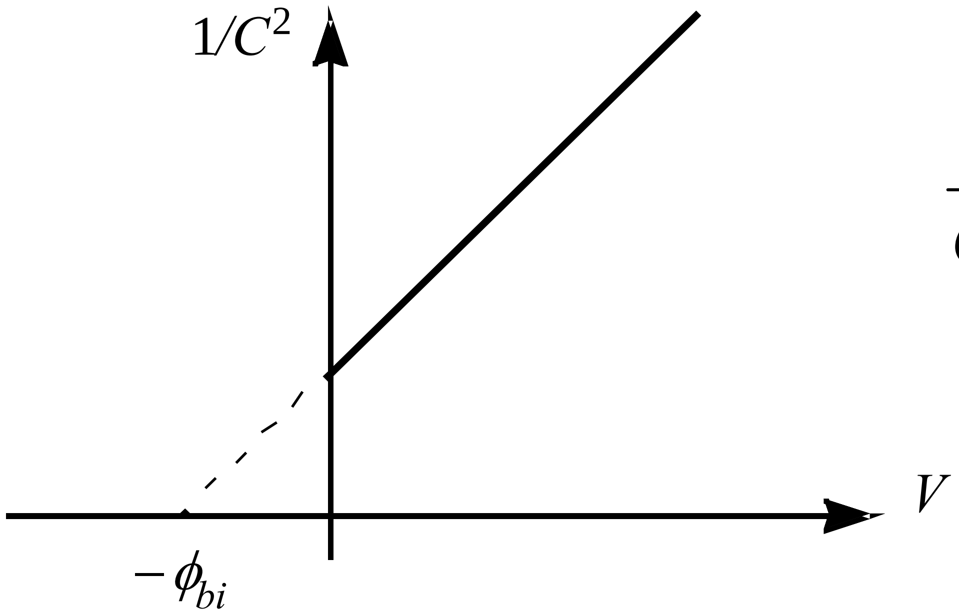
$$W_{dep} = \sqrt{\frac{2\varepsilon_s(\phi_{bi} + V)}{qN_d}}$$

$$C = \frac{\varepsilon_s}{W_{dep}}A$$

Question:

How should we plot the CV data to extract ϕ_{bi}?

Using CV Data to Determine ϕ_B

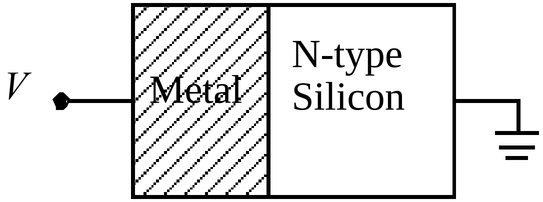


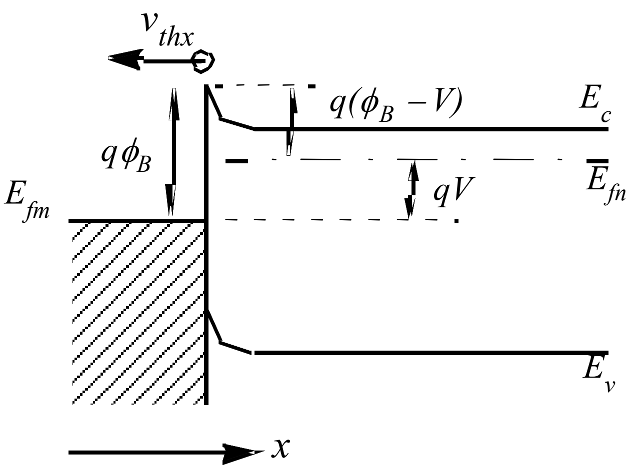
$$\frac{1}{C^2} = \frac{2(\phi_{bi} + V)}{qN_d\varepsilon_s A^2}$$

Once ϕ_{bi} is known, ϕ_B can be determined using

$$q\phi_{bi} = q\phi_{Bn} - (E_c - E_f) = q\phi_{Bn} - kT\ln\frac{N_c}{N_d}$$

9.2 Thermionic Emission Theory





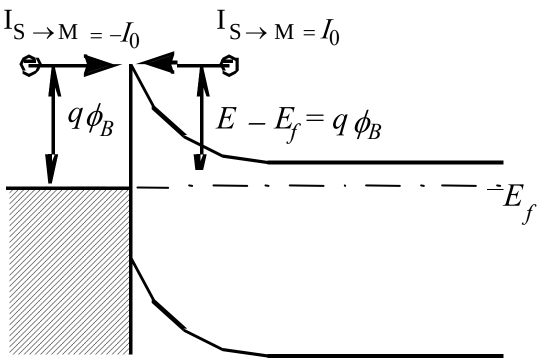
$$n = N_c e^{-q(\phi_B - V)/kT} = 2\left[\frac{2\pi m_n kT}{h^2}\right]^{3/2} e^{-q(\phi_B - V)/kT}$$

$$v_{th} = \sqrt{3kT/m_n} \qquad v_{thx} = -\sqrt{2kT/\pi m_n}$$

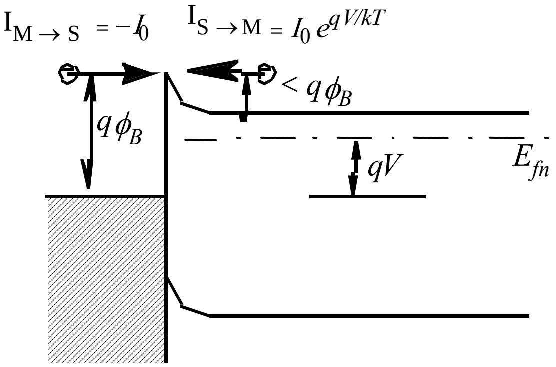
$$J_{S\to M} = -\frac{1}{2} q n v_{thx} = \frac{4\pi q m_n k^2}{h^3} T^2 e^{-q\phi_B/kT} e^{qV/kT}$$

$$= J_0 e^{qV/kT}, \text{where } J_o \approx 100 e^{-q\phi_B/kT} \text{ A/cm}^2$$

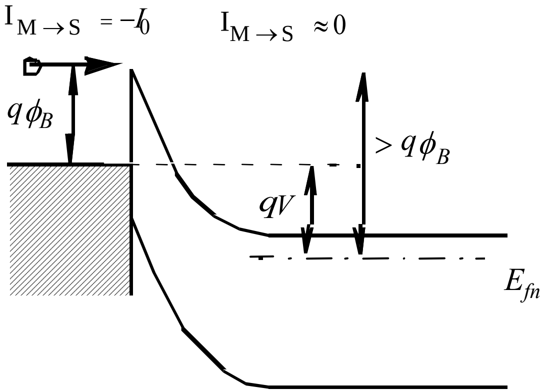
9.3 Schottky Diode



(a) $V = 0$. $I_{S\rightarrow M} = |I_{M\rightarrow S}| = I_0$

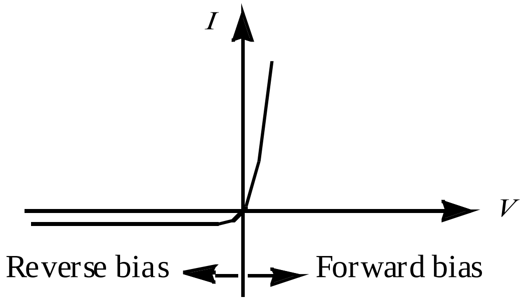


(b) Forward bias. Metal is positive wrt Si. $I_{S\rightarrow M} >> |I_{M\rightarrow S}| = I_0$



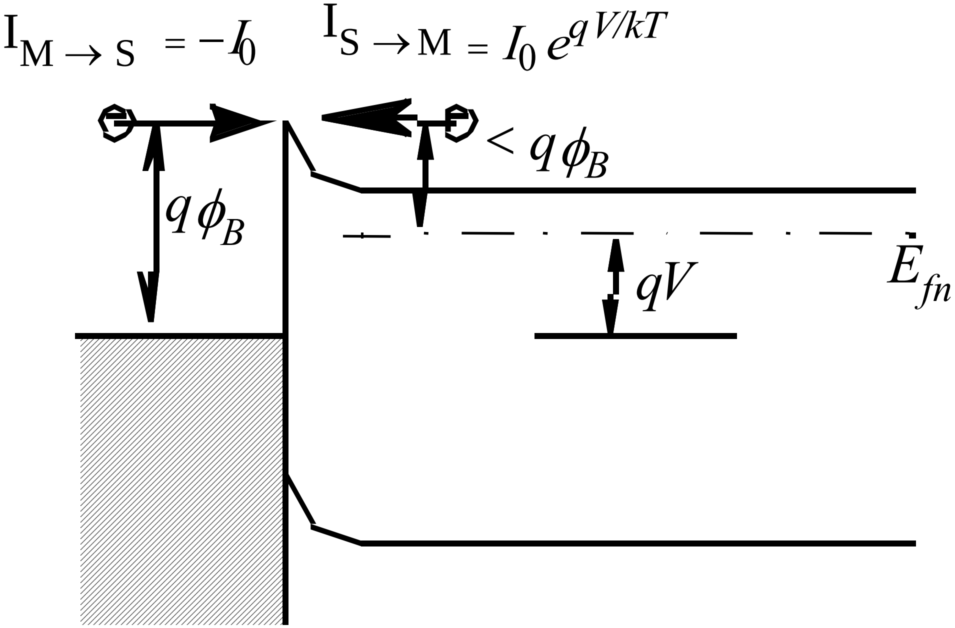
(c) Reverse bias. Metal is negative wrt Si.

$I_{S\rightarrow M} << |I_{M\rightarrow S}| = I_0$



(d) Schottky diode IV.

9.3 Schottky Diode



$$I_0 = AKT^2 e^{-q\phi_B/kT}$$

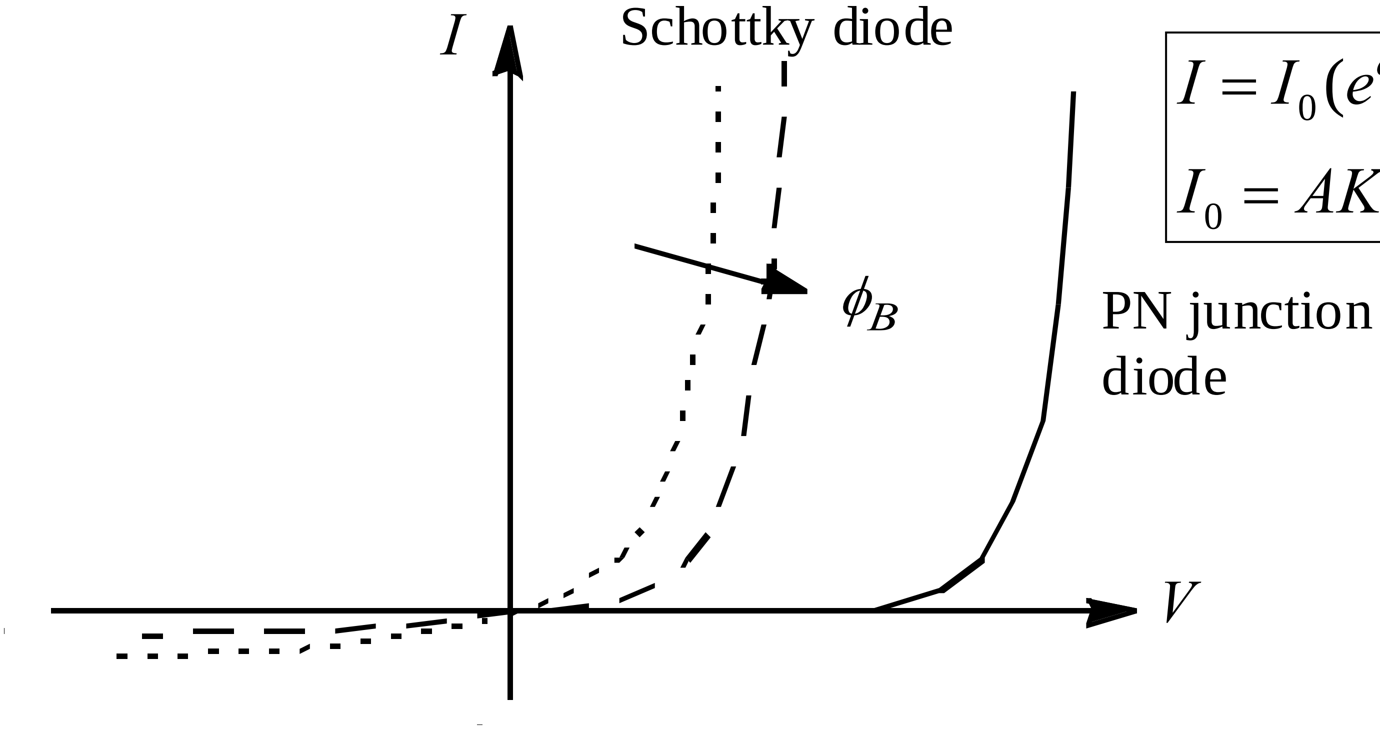
$$K = \frac{4\pi q m_n k^2}{h^3} \approx 100\ \mathrm{A/(cm^2 \cdot K^2)}$$

$$I = I_{S\to M} + I_{M\to S} = I_0 e^{qV/kT} - I_0 = I_0(e^{qV/kT} - 1)$$

9.4 Applications of Schottky Diodes

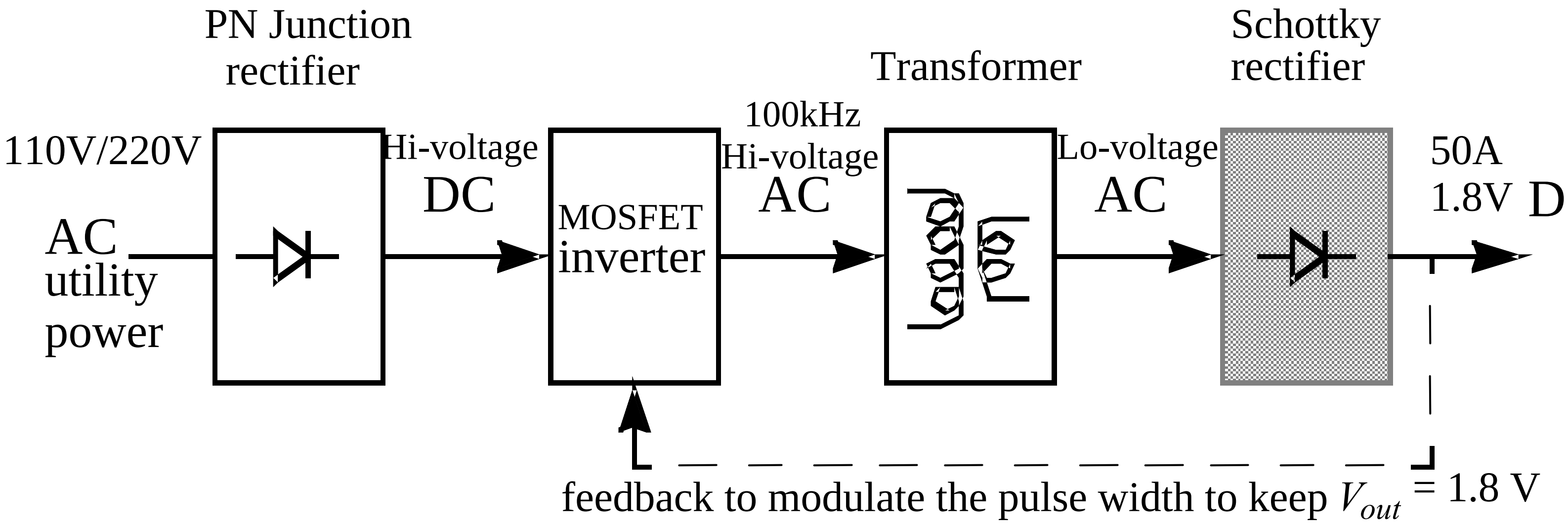
$$I = I_0\left(e^{qV/kT} - 1\right)$$

$$I_0 = AKT^2 e^{-q\phi_B/kT}$$



- I_0 of a Schottky diode is 10^3 to 10^8 times larger than a PN junction diode, depending on ϕ_B. A larger I_0 means a smaller forward drop V.
- A Schottky diode is the preferred rectifier in low voltage, high current applications.

Switching Power Supply



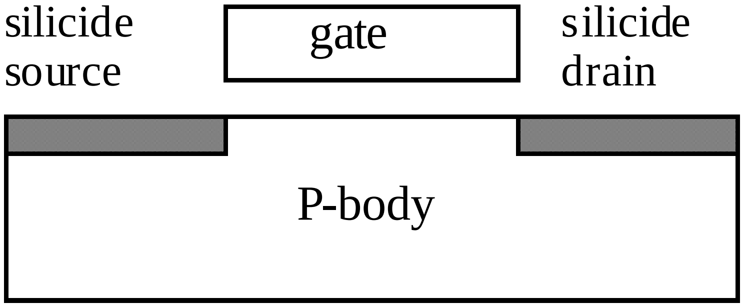
Question*:* What sets the lower limit in a Schottky diode's forward drop?

Synchronous Rectifier: For an even lower forward drop, replace the diode with a wide-W MOSFET which is not bound by the tradeoff between diode V and I_0: $I = I_0 e^{qV/kT}$

9.4 Applications of Schottky Diodes

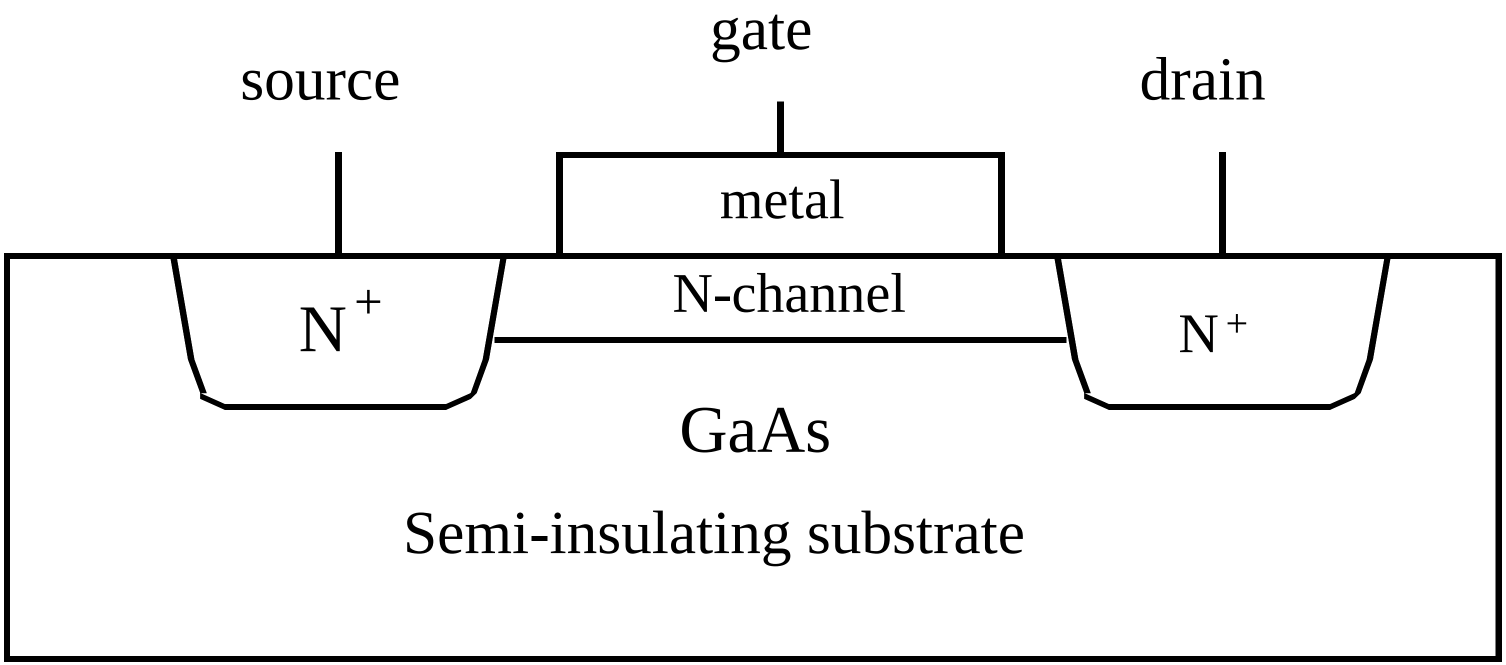
There is no minority carrier injection at the Schottky junction. Thus, the CMOS latch-up problem can be eliminated by replacing the source/drain of the NFET with Schottky junctions.

In addition, the Schottky S/D MOSFET would have shallow junctions and low series resistance. So far, Schottky S/D MOSFETs have lower performance.



No excess carrier storage. What application may benefit from that?

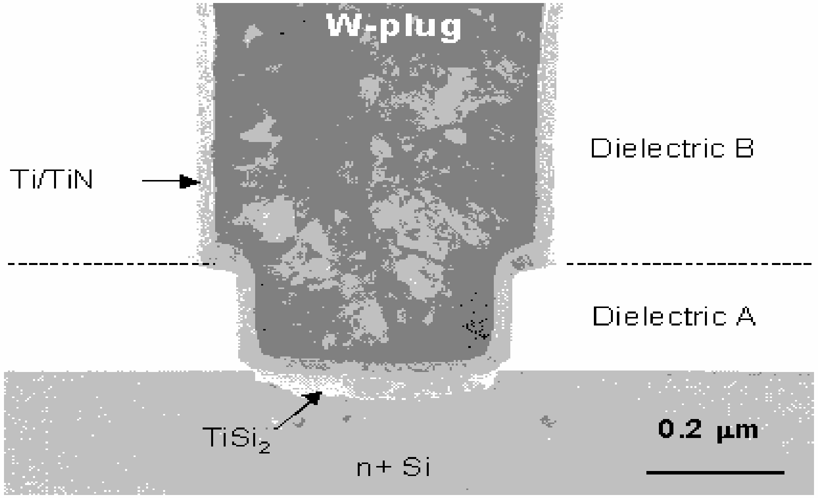
GaAs MESFET

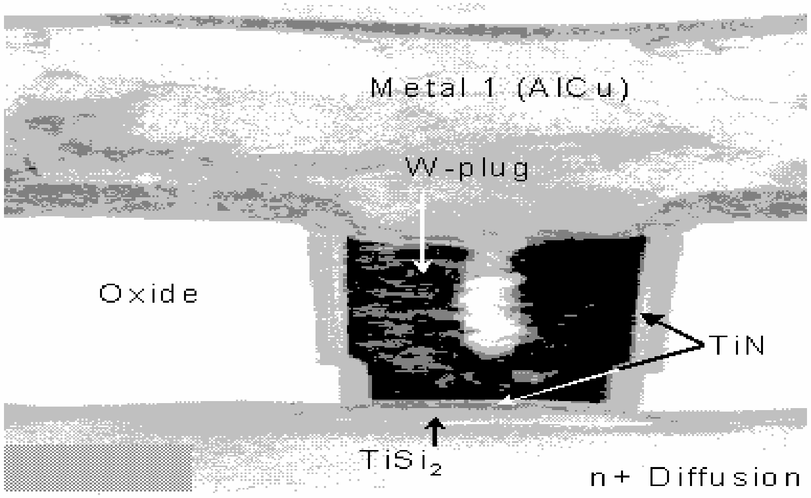


The MESFET has similar IV characteristics as the MOSFET, but does not require a gate oxide.

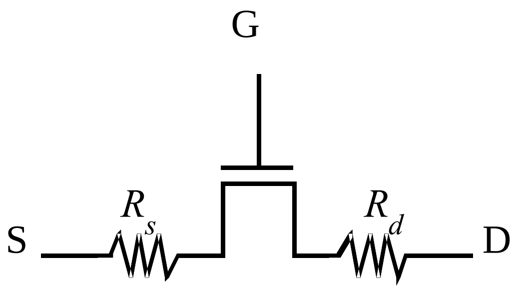
Question: What is the advantage of GaAs over Si?

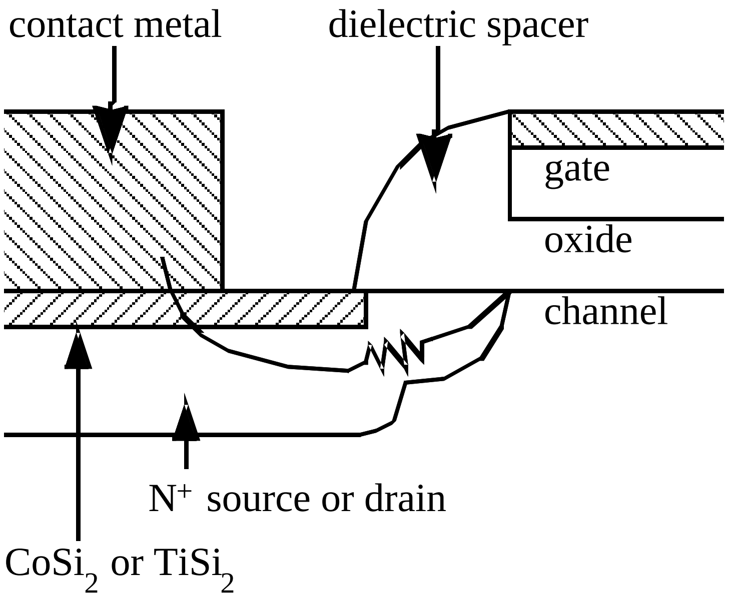
9.5 Ohmic Contacts





SALICIDE (Self-Aligned Silicide) Source/Drain





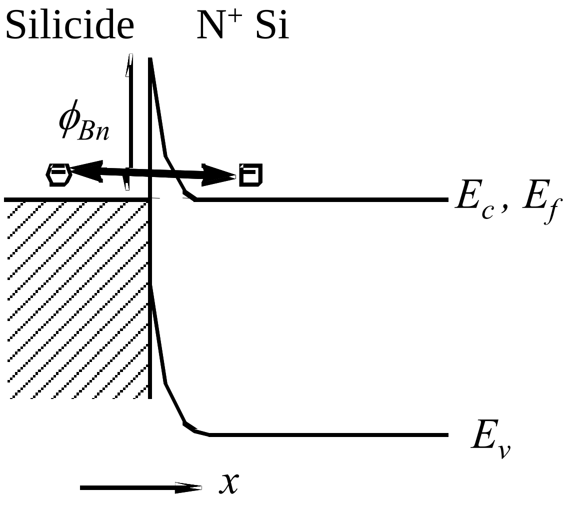
After the spacer is formed, a Ti or Mo film is deposited. Annealing causes the silicide to be formed over the source, drain, and gate. Unreacted metal (over the spacer) is removed by wet etching.

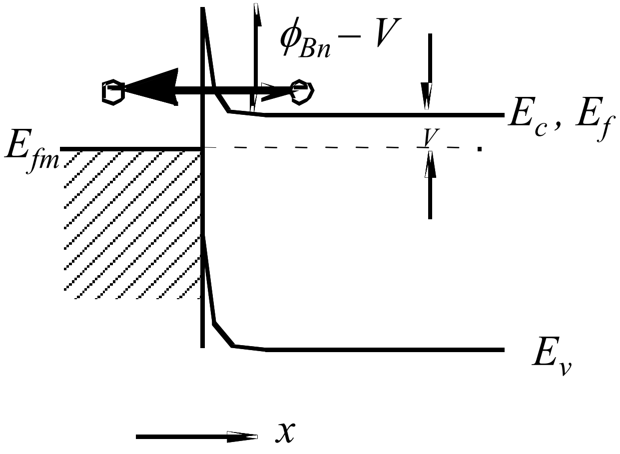
Question:

- What is the purpose of siliciding the source/drain/gate?
- What is self-aligned to what?

9.5 Ohmic Contacts

$$W_{dep} = \sqrt{\frac{2\varepsilon_s \phi_{Bn}}{qN_d}}$$





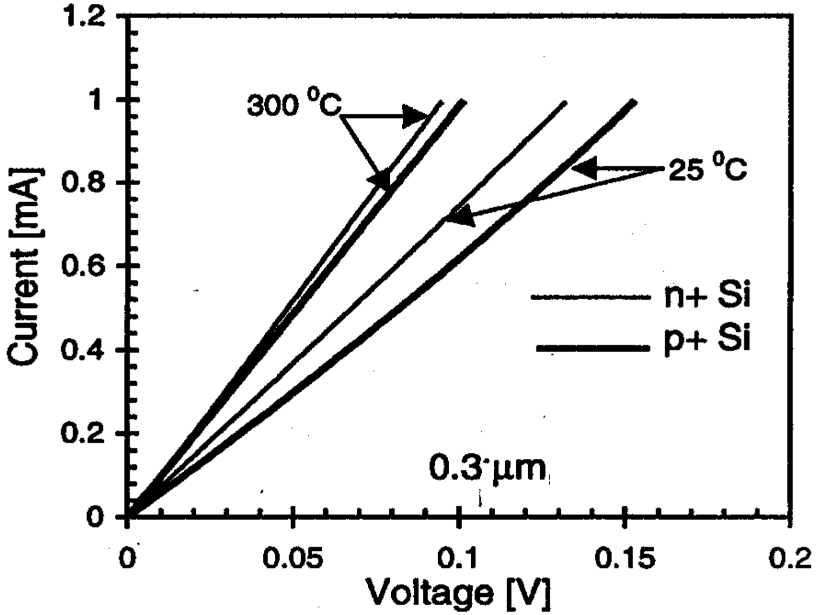
Tunneling probability:

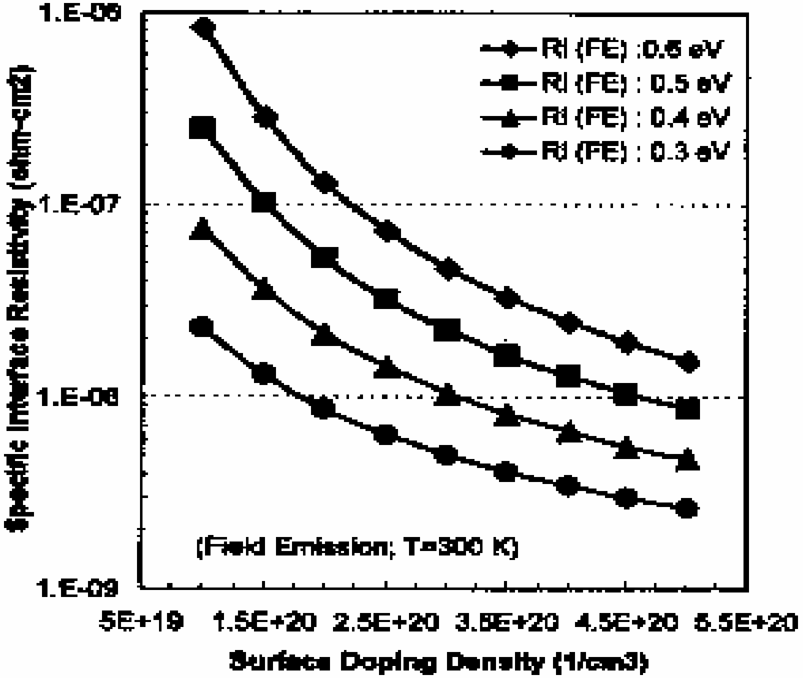
$$P = e^{-H\phi_{Bn}/\sqrt{N_d}}$$

$$H = 4\pi\sqrt{\varepsilon_s m_n}\,/\,h = 5.4\times10^9\sqrt{m_n/m_o}\ \mathrm{cm}^{-3/2}\mathrm{V}^{-1}$$

$$J_{S\rightarrow M} \approx \frac{1}{2}qN_d v_{thx}P = qN_d\sqrt{kT/2\pi m_n}\,e^{-H(\phi_{Bn}-V)/\sqrt{N_d}}$$

9.5 Ohmic Contacts





$$R_c \equiv \left(\frac{dJ_{S \to M}}{dV} \right)^{-1} = \frac{e^{H\phi_{Bn}/\sqrt{N_d}}}{qv_{thx}H\sqrt{N_d}} \propto e^{H\phi_{Bn}/\sqrt{N_d}} \;\; \Omega \cdot \mathrm{cm}^2$$