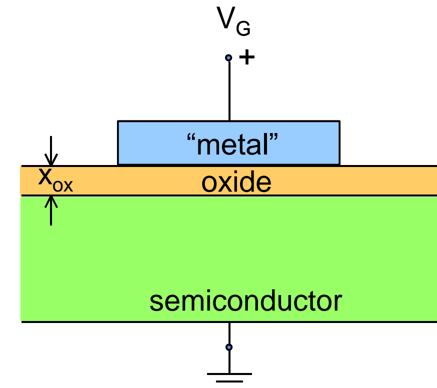
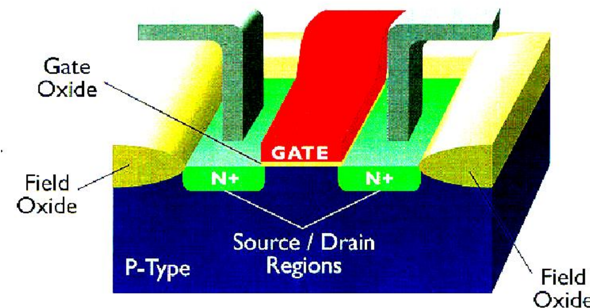
Electrical Characteristics of MOS Devices



- **The MOS Capacitor**
  - Voltage components
  - Accumulation, Depletion, Inversion Modes
  - Effect of channel bias and substrate bias
  - Effect of gate oxide charges
  - Threshold-voltage adjustment by implantation
  - Capacitance vs. voltage characteristics
- **MOS Field-Effect Transistor**
  - I-V characteristics
  - Parameter extraction



1) Reading Assignment

Streetman: Section of Streetman Chap 8 on MOS

2) **Visit the Device Visualization Website**

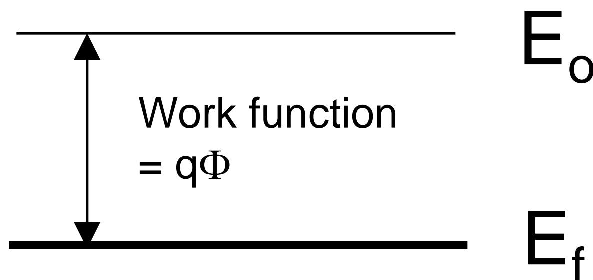
http://jas.eng.buffalo.edu/

and run the *visualization experiments* of

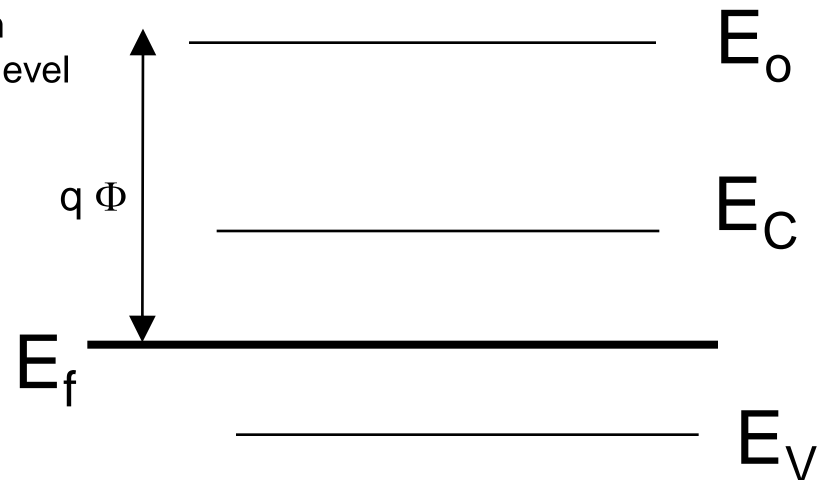
1) Charge carriers and Fermi level,
2) pn junctions
3) MOS capacitors
4) MOSFETs

Work Function of Materials

METAL



SEMICONDUCTOR



$q\Phi_M$ is determined

by the metal material

$q\Phi_S$ is determined

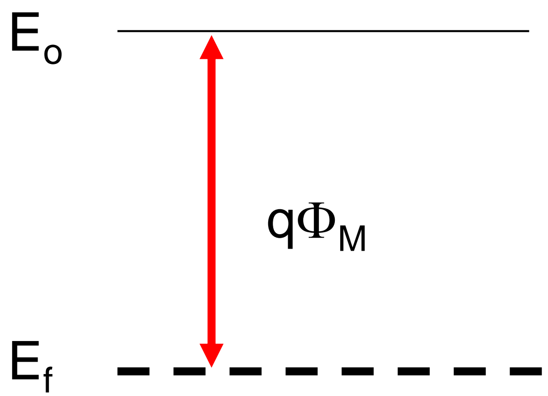
by the semiconductor material,

the dopant type,

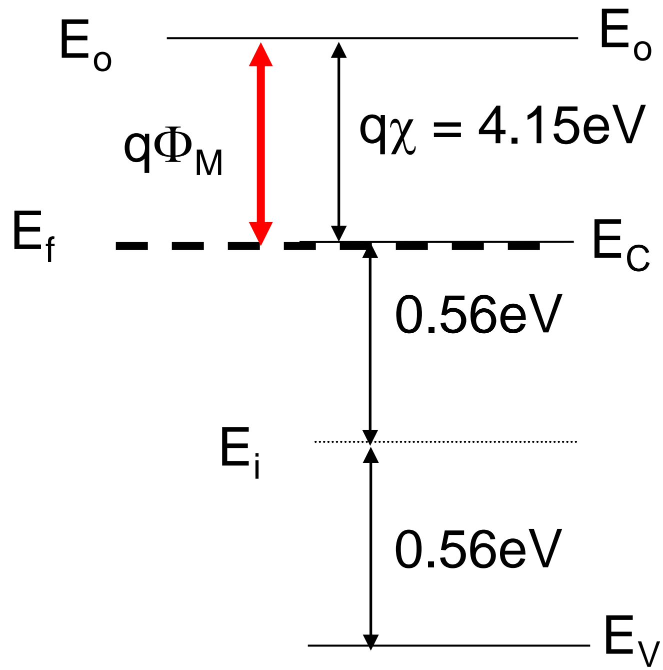
and doping concentration

Work Function ($q\Phi_M$) of MOS Gate Materials

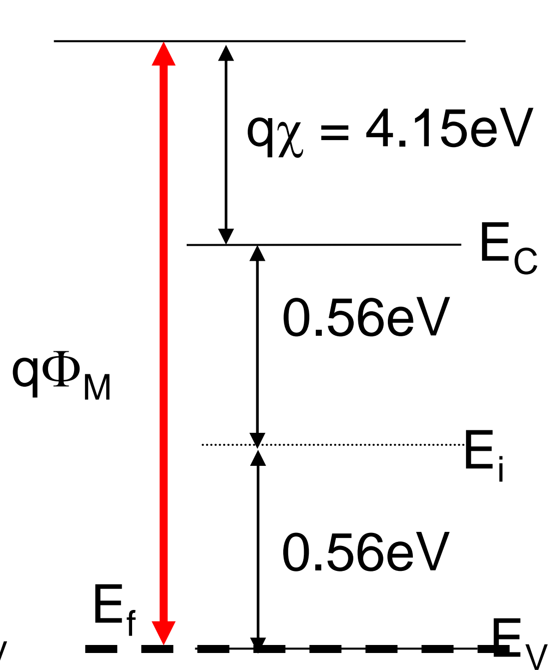
E_o = vacuum energy level **E_f** = Fermi level
E_C = bottom of conduction band **E_V** = top of conduction band
$q\chi$ = 4.15eV (electron affinity)



Examples:
Al = 4.1 eV
$TiSi_2$ = 4.6 eV



n+ poly-Si
(E_f = E_C)

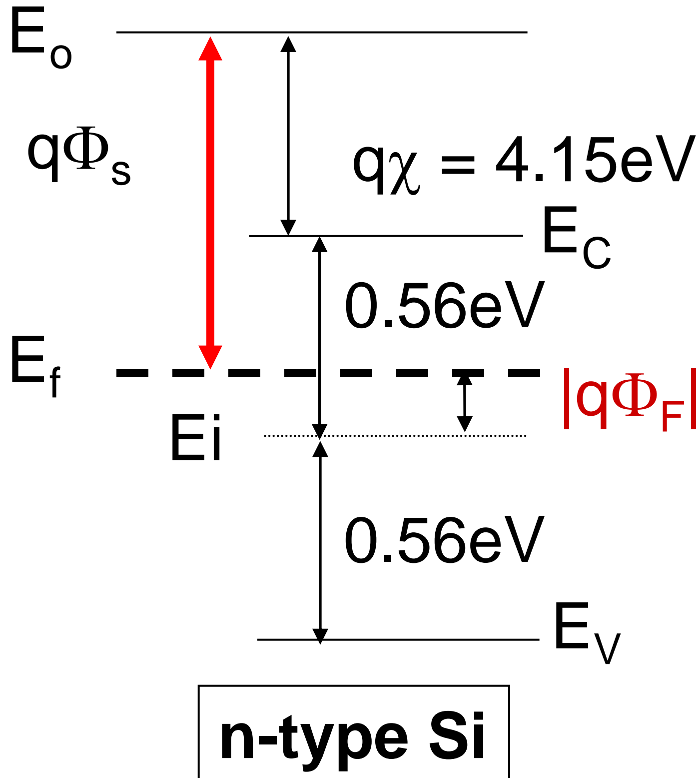


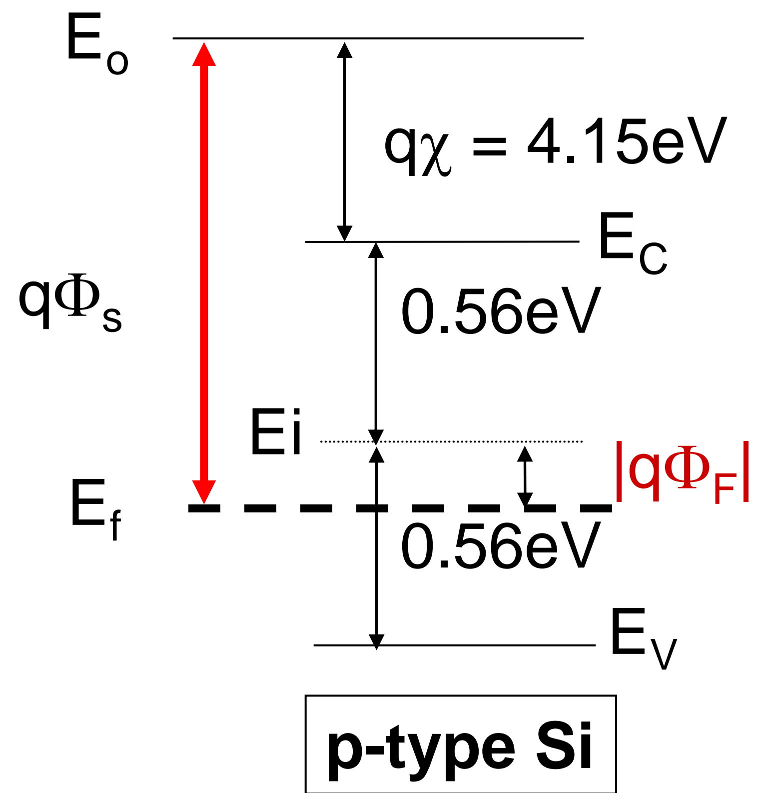
p+ poly-Si
(E_f = E_V)

Work Function of doped Si substrate

* Depends on substrate concentration N_B

$$|\Phi_F| = \frac{kT}{q} \ln\left(\frac{N_B}{n_i}\right)$$

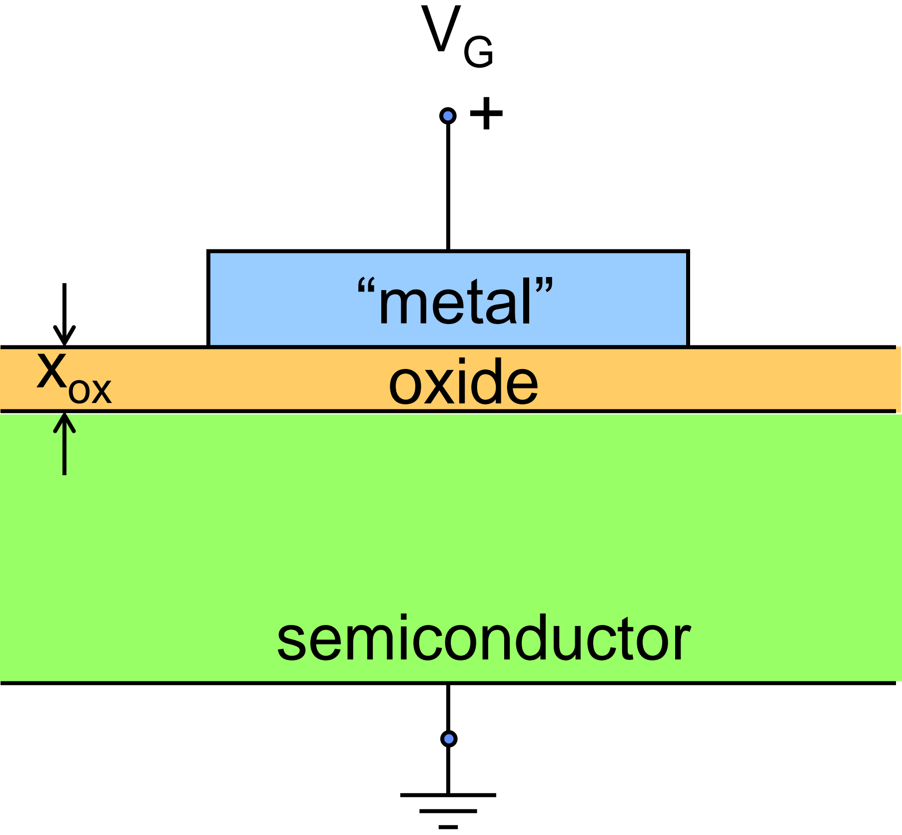


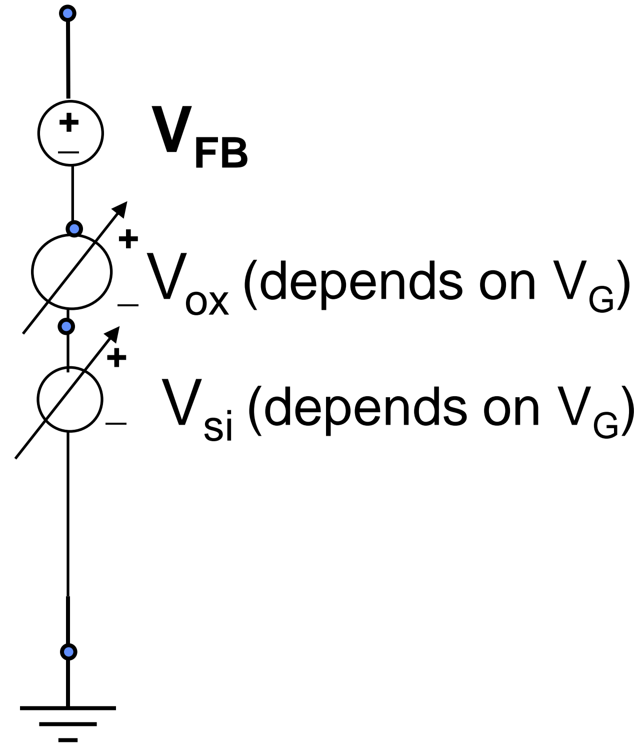


Φ_s (volts) = 4.15 +0.56 - $|\Phi_F|$

Φ_s (volts) = 4.15 +0.56 + $|\Phi_F|$

The MOS Capacitor





$$V_G = V_{FB} + V_{ox} + V_{Si}$$

$$C_{ox} = \frac{\varepsilon_{ox}}{x_{ox}}$$ [in Farads /cm^2]

Oxide capacitance/unit area

Flat Band Voltage

- V_{FB} is the "built-in" voltage of the MOS:

$$V_{FB} \equiv \Phi_M - \Phi_S$$

  - Gate work function Φ_M:

    Al: 4.1 V; n+ poly-Si: 4.15 V; p+ poly-Si: 5.27 V

  - Semiconductor work function Φ_S :

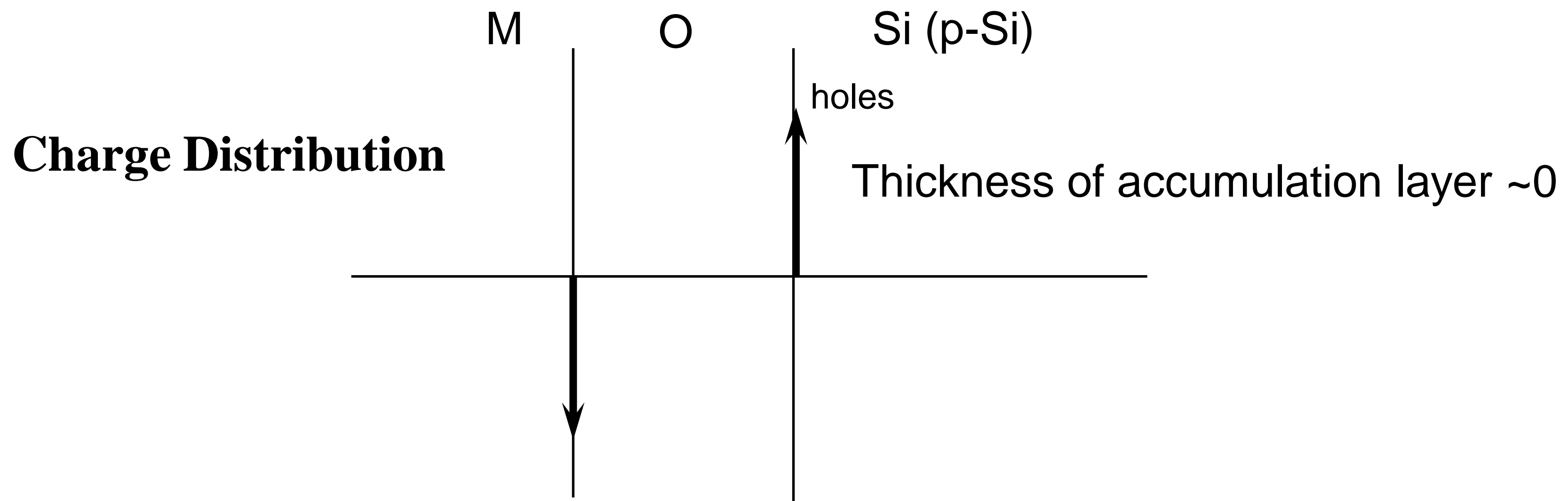
$$\Phi_s \text{(volts)} = 4.15 + 0.56 - |\Phi_F| \text{ for n-Si}$$

$$\Phi_s \text{(volts)} = 4.15 + 0.56 + |\Phi_F| \text{ for p-Si}$$

- V_{ox} = voltage drop across oxide (depends on V_G)
- V_{Si} = voltage drop in the silicon (depends on V_G)

MOS Operation Modes

A) Accumulation: $V_G < V_{FB}$ for p-type substrate



$V_{Si} \approx 0$, so $V_{ox} = V_G - V_{FB}$

Q_{Si}' = charge/unit area in Si

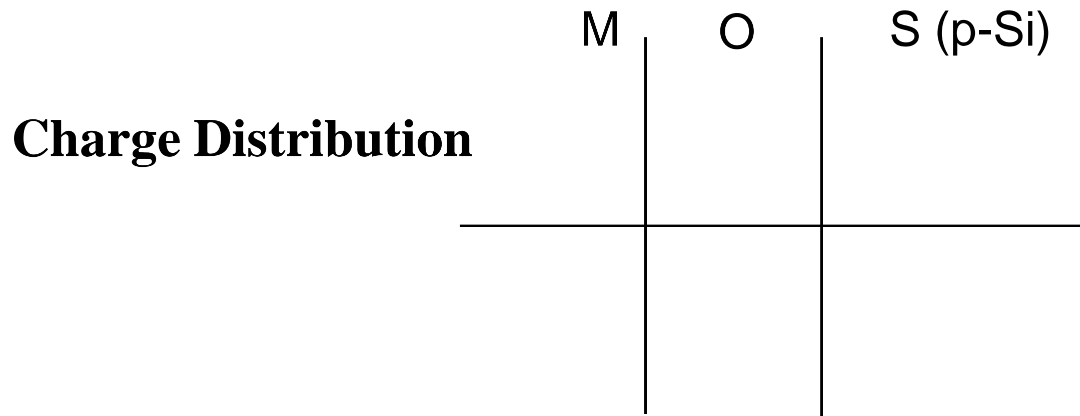
$= C_{ox}(V_G - V_{FB})$

MOS Operation Modes

- **B) Flatband Condition :** $V_G = V_{FB}$

No charge in Si (and hence no charge in metal gate)

- $V_{Si} = V_{ox} = 0$

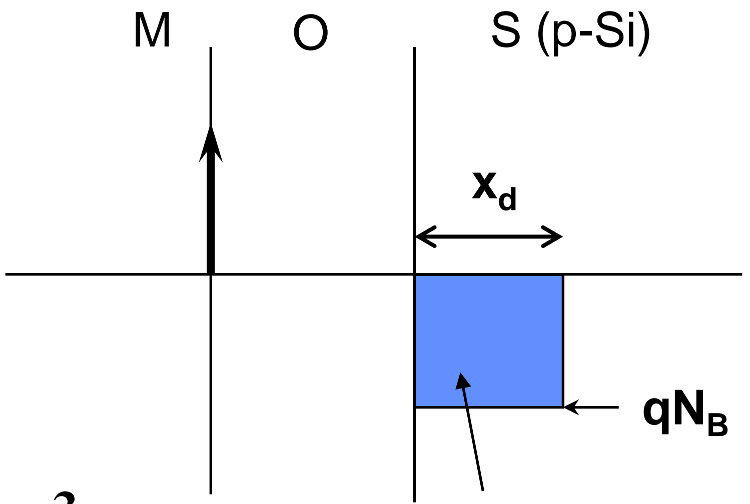


MOS Operation Modes (cont.)

C) Depletion: $V_G > V_{FB}$

Depletion Layer thickness

$$x_d = \sqrt{\frac{2\varepsilon_{Si} V_{Si}}{qN_B}}$$

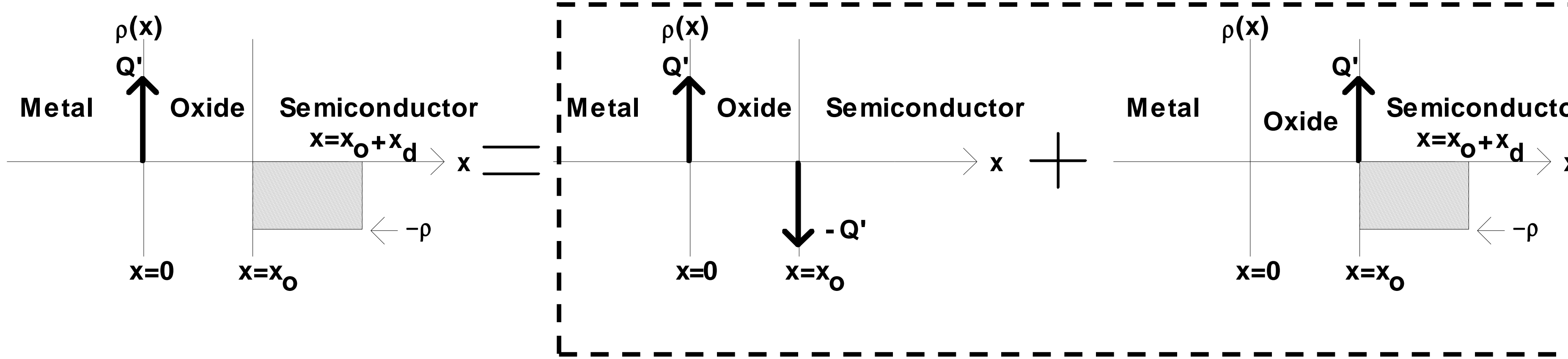


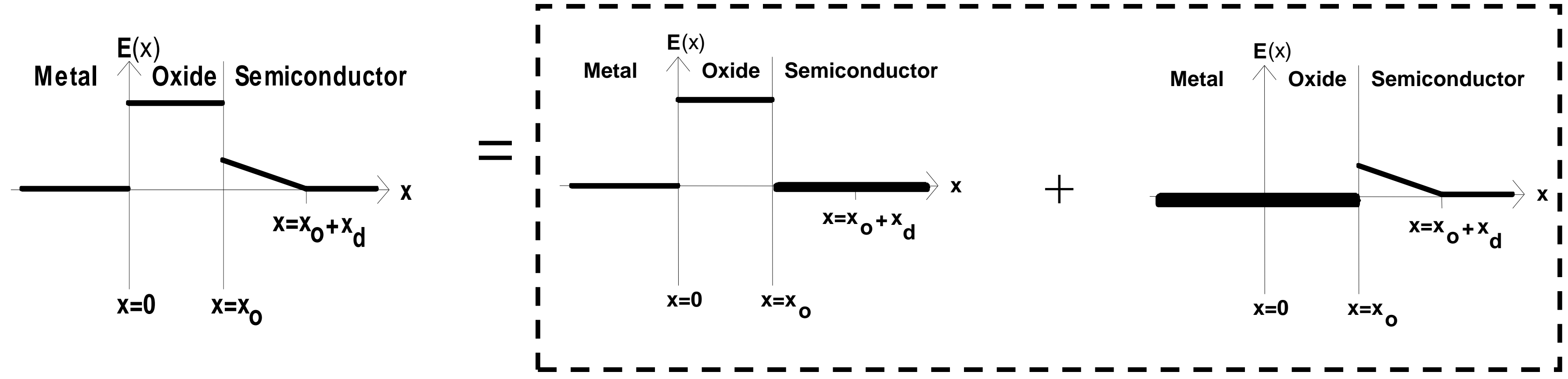
$$V_G = V_{FB} + \underbrace{\frac{qN_B x_d}{C_{ox}}}_{V_{ox}} + \underbrace{\frac{qN_B x_d^{\,2}}{2\varepsilon_s}}_{V_{Si}}$$

Note: $N_B x_d$ is the total charge in Si /unit area

(For given V_G, can solve for x_d)

Depletion Mode :Charge and Electric Field Distributions by Superposition Principle of Electrostatics





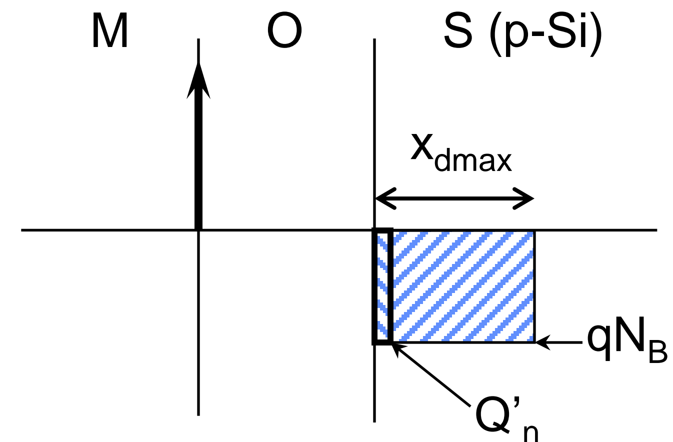
MOS Operation Modes (cont.)

D) Threshold of Inversion: $V_G = V_T$

This is a ***definition*** for onset of strong inversion

$n_{surface} = N_B$ (for p-type substrate)

=> $V_{Si} = 2|\Phi_F|$



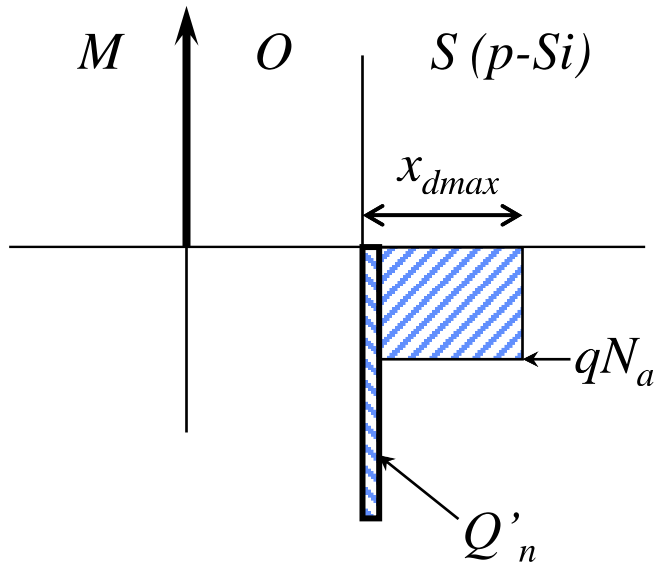
$$V_G = V_T = V_{FB} + \frac{\sqrt{2\varepsilon_s(2|\Phi_F|)qN_B}}{C_{ox}} + 2|\Phi_F|$$

MOS Operation Modes (cont.)

E) Strong Inversion: $V_G > V_T$

$$x_{d\max} = \sqrt{\frac{4\varepsilon_{Si}|\Phi_F|}{qN_B}}$$

x_{dmax} is approximately unchanged when $V_G > V_T$

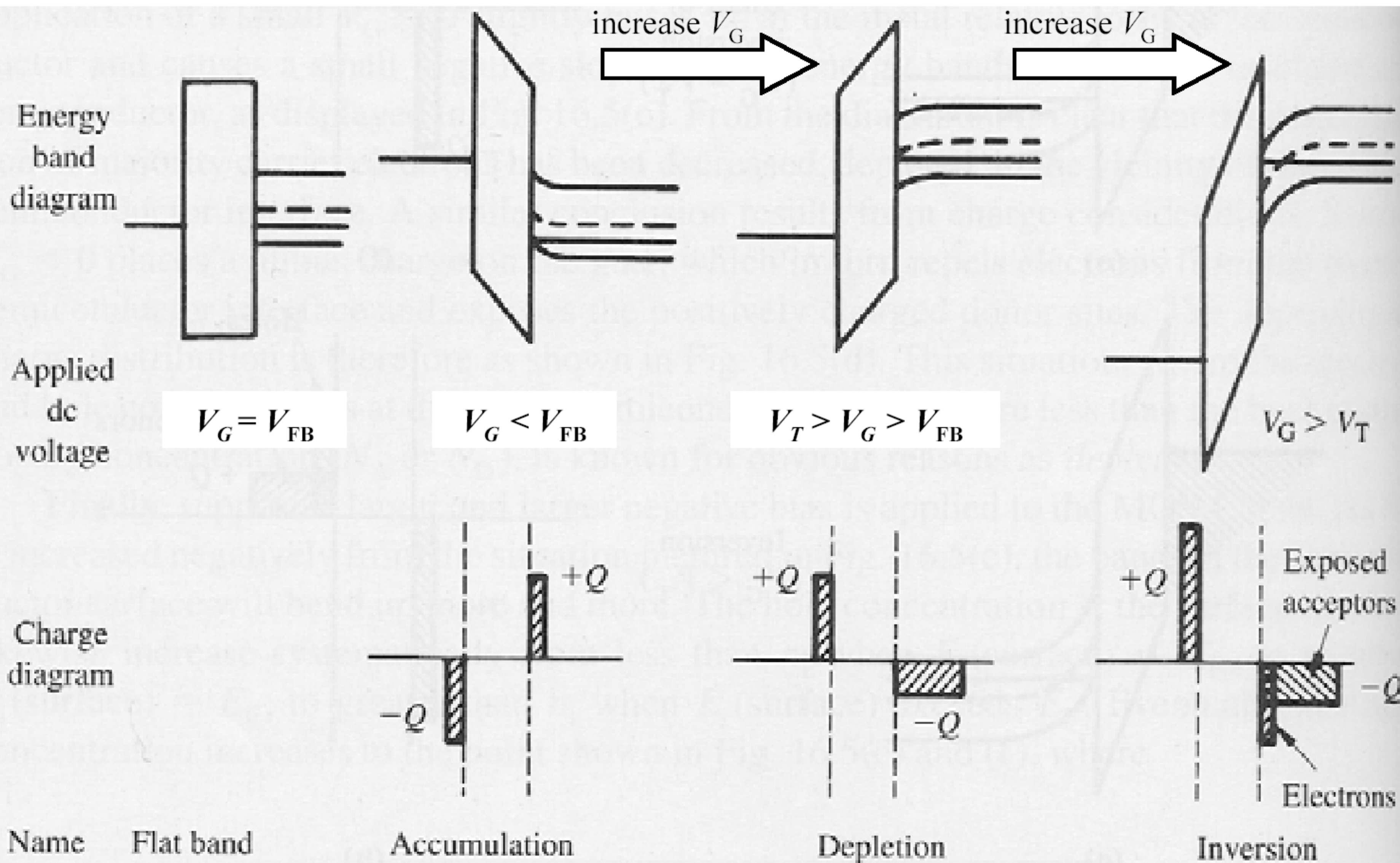


$$V_{ox} = \frac{qN_B x_{d\max} + |Q_n'|}{C_{ox}}$$

$$Q_n' \approx -C_{ox}(V_G - V_T)$$

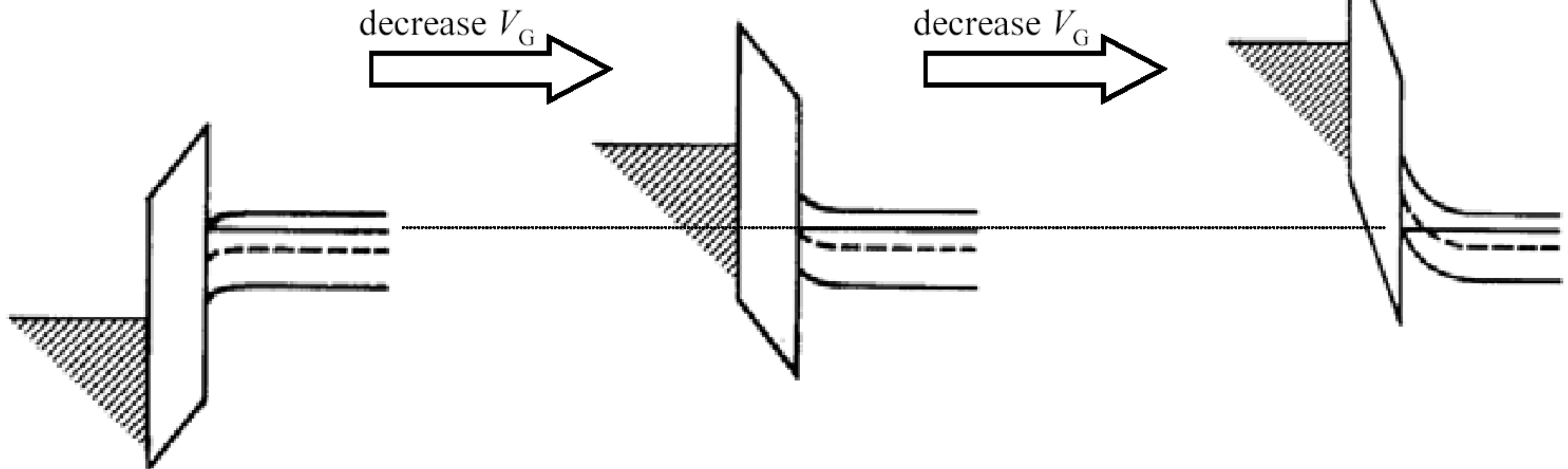
electrons

Biasing Conditions for p-type Si



MOS Band Diagrams (n-type Si)

Decrease V_G (toward more negative values)
-> move the gate energy-bands up, relative to the Si



- Accumulation
  - $V_G > V_{FB}$
  - Electrons accumulate at surface
- Depletion
  - $V_G < V_{FB}$
  - Electrons repelled from surface
- Inversion
  - $V_G < V_T$
  - Surface becomes p-type

Total Charge Density in Si, Q_s

$\mathbf{Q_{acc}} = -C_{ox}(V_G - V_{FB})$

accumulation | depletion | inversion

0, V_{FB}, V_T, V_G

accumulation | depletion | inversion

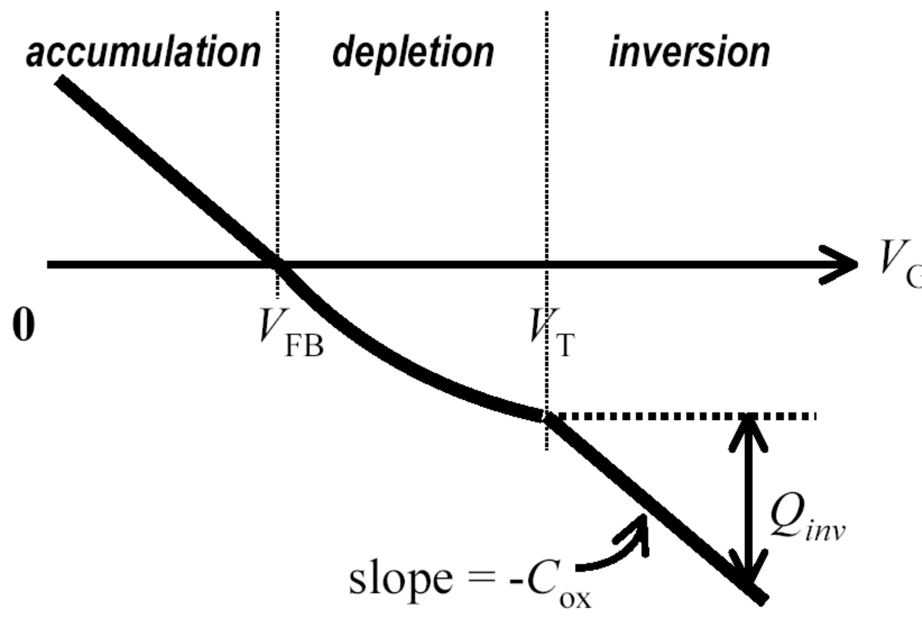
$\mathbf{Q_{dep}} = -qN_A W$

accumulation | depletion | inversion

$\mathbf{Q_{inv}} = -C_{ox}(V_G - V_T)$

p-Si

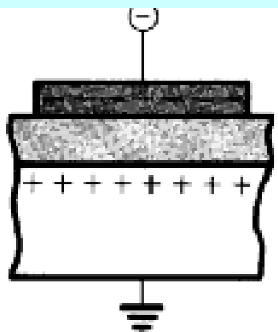
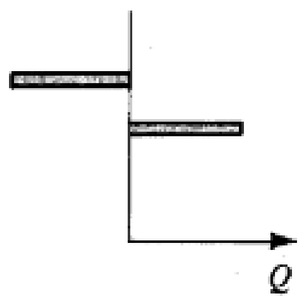
$$Q_s = Q_{acc} + Q_{dep} + Q_{inv}$$

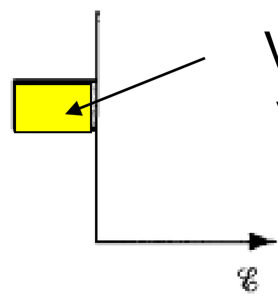


Voltage drop = area under E-field curve

Key:
+ Holes
− Electrons
⊖ Acceptor ions

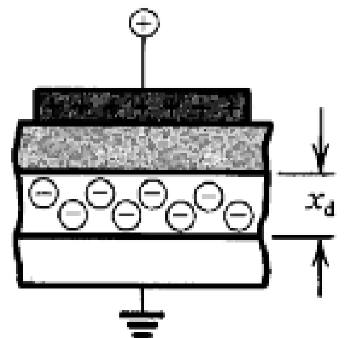
Accumulation

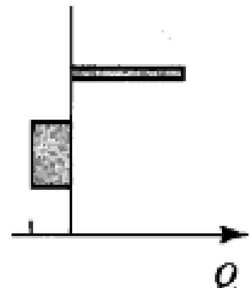



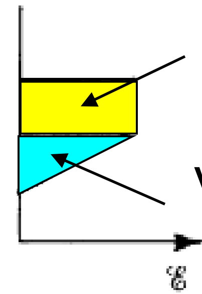


$V_{ox} = Q_a/C_{ox}$
$V_{Si} \sim 0$

Depletion



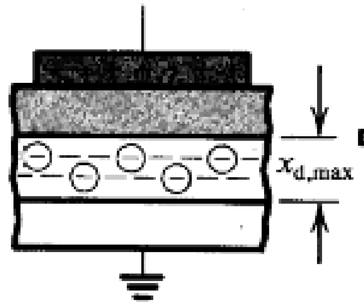


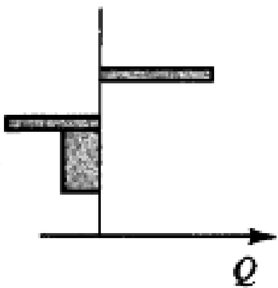


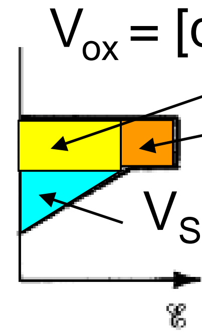
$V_{ox} = qN_a x_d/C_{ox}$

$V_{Si} = qN_a x_d^2/(2\varepsilon_s)$

Inversion







$V_{ox} = [qN_a x_{dmax} + Q_n]/C_{ox}$

$V_{Si} = qN_a x_{dmax}^2/(2\varepsilon_s)$
$= 2|\Phi_F|$

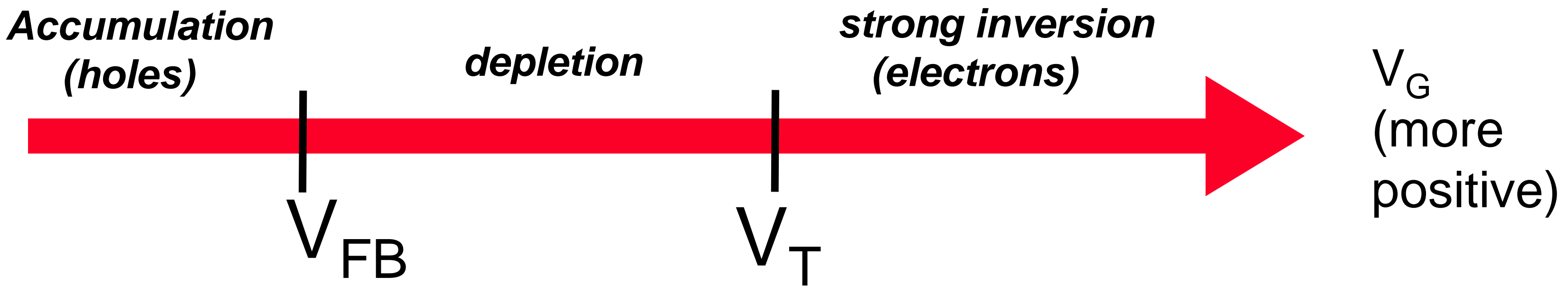
* **For simplicity, dielectric constants assumed to be same for oxide and Si in E-field sketches**

Suggested Exercise

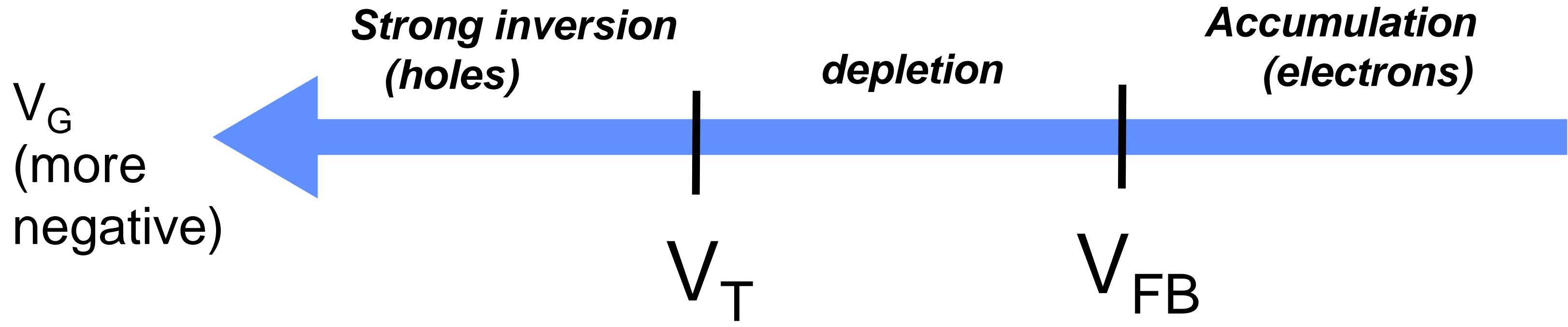
Most derivations for MOS shown in lecture notes are done with p-type substrate (NMOS) as example.

Repeat the derivations yourself for n-type substrate (PMOS) to test your understanding of MOS.

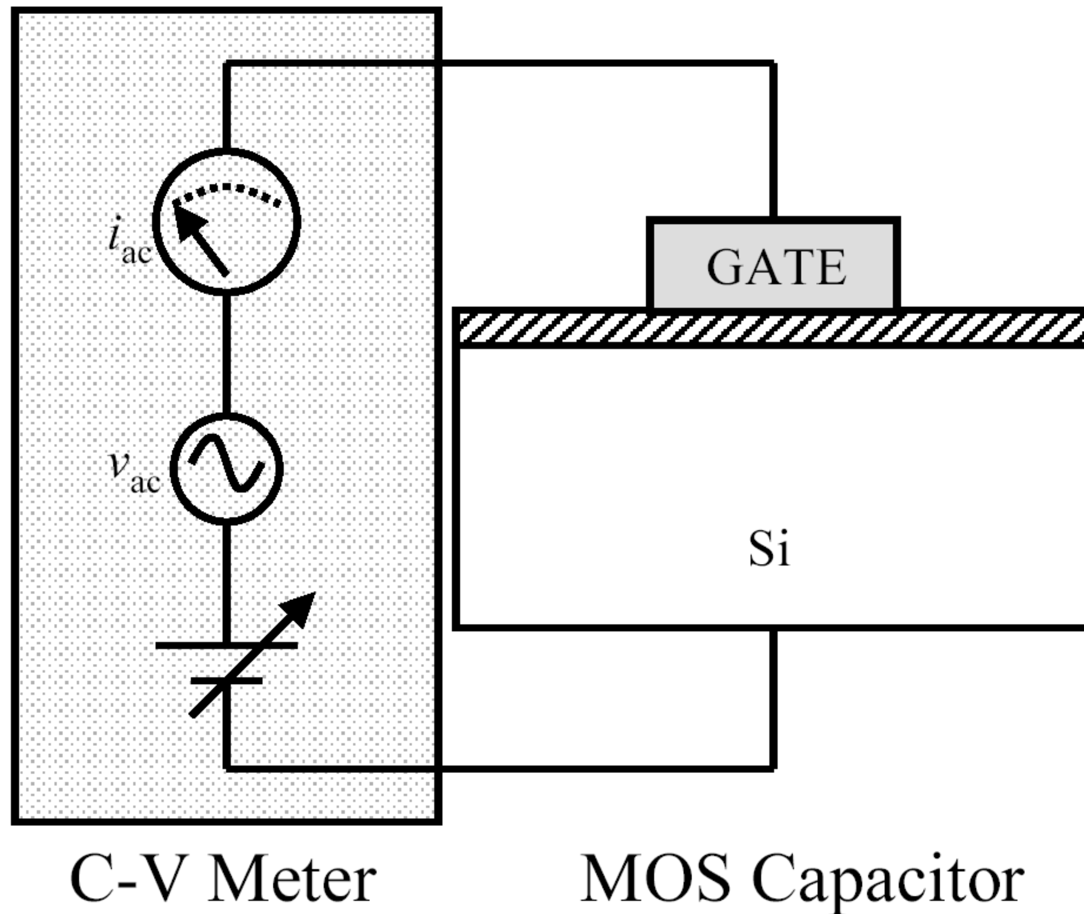
p-Si substrate (NMOS)



n-Si substrate (PMOS)



MOS Capacitance Measurement

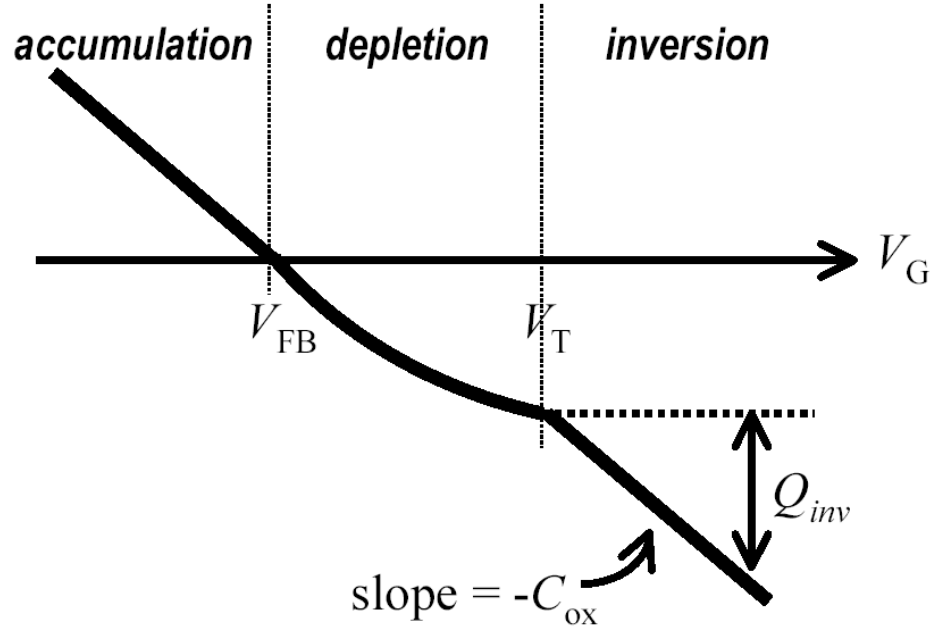


- V_G is scanned slowly
- Capacitive current due to v_{ac} is measured

$$i_{ac} = C\frac{dv_{ac}}{dt}$$

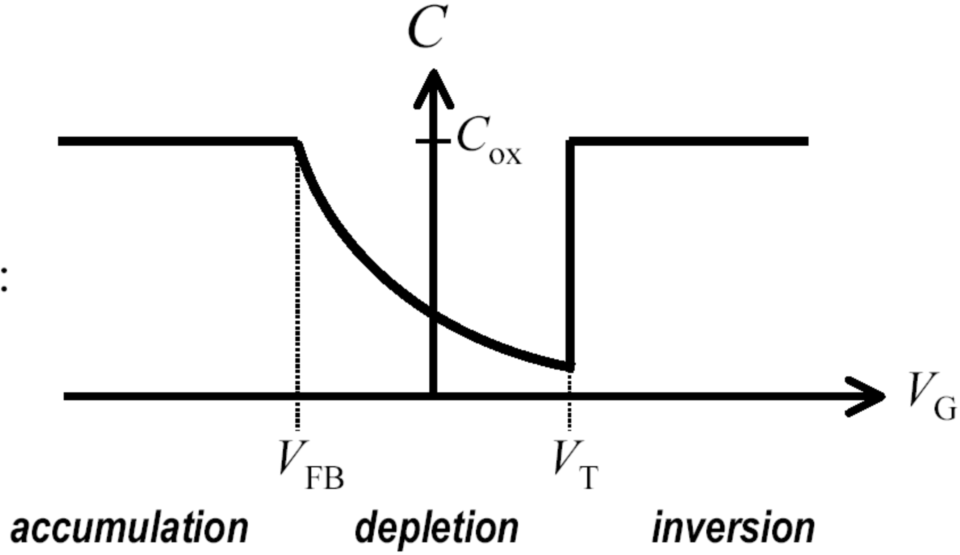
$$C = \left|\frac{dQ_{GATE}}{dV_G}\right| = \left|\frac{dQ_s}{dV_G}\right|$$

MOS *C-V* Characteristics (p-type Si)



$$C = \left| \frac{dQ_s}{dV_G} \right|$$

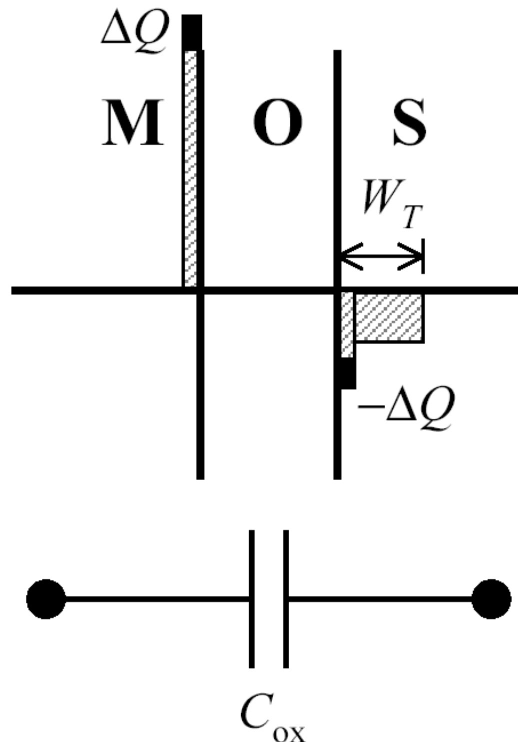
Ideal *C-V* curve:



Capacitance in Inversion (p-type Si)

CASE 1: Inversion-layer charge can be supplied/removed quickly enough to respond to changes in the gate voltage.

→ Incremental charge is effectively added/subtracted at the surface of the substrate.



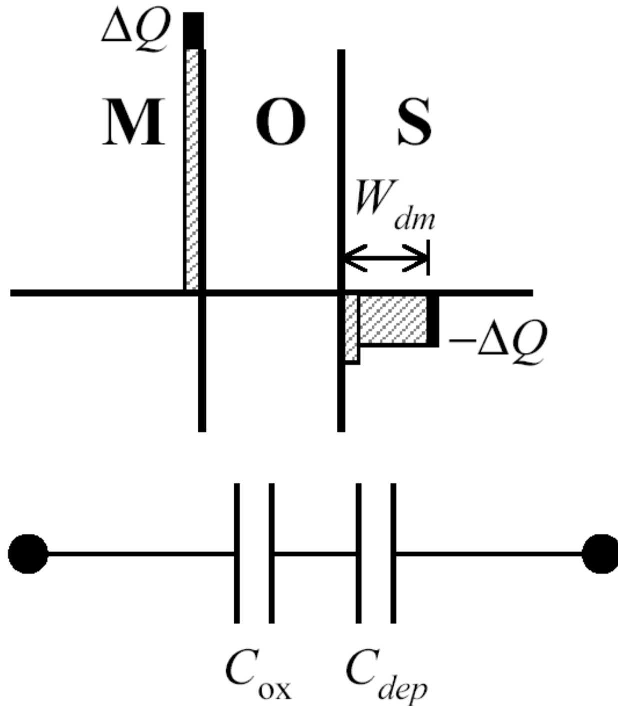
Time required to build inversion-layer charge = $2N_A\tau_o/n_i$, where
τ_o = minority-carrier lifetime at surface

$$C = \left|\frac{dQ_{inv}}{dV_G}\right| = C_{ox}$$

Capacitance in Inversion (p-type Si)

<u>CASE 2</u>: Inversion-layer charge cannot be supplied/removed quickly enough to respond to changes in the gate voltage.

→ Incremental charge is effectively added/subtracted at a depth W_d in the substrate.



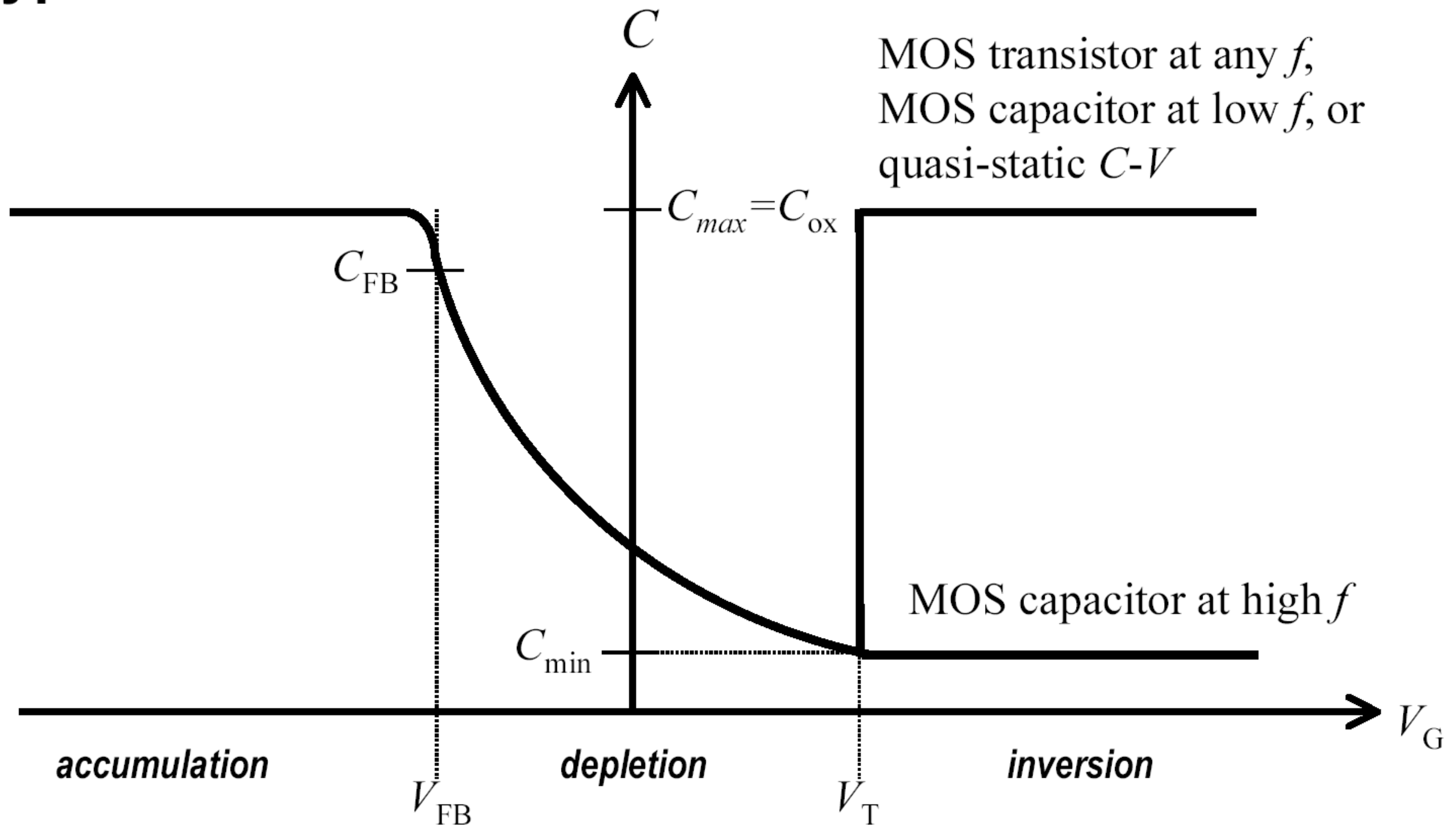
$$\frac{1}{C} = \frac{1}{C_{ox}} + \frac{1}{C_{dep}}$$

$$= \frac{1}{C_{ox}} + \frac{W_{dm}}{\varepsilon_{Si}}$$

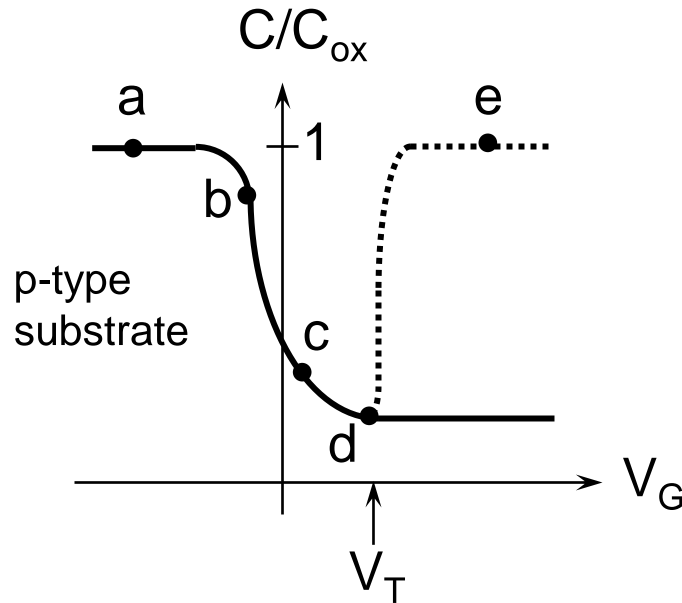
$$= \frac{1}{C_{ox}} + \sqrt{\frac{2(2\psi_B)}{qN_A\varepsilon_{Si}}} \equiv \frac{1}{C_{\min}}$$

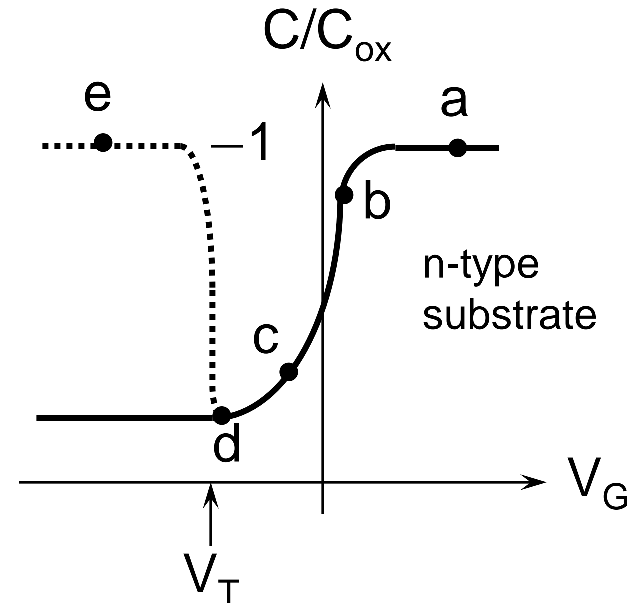
Capacitor *vs.* Transistor *C-V* (or LF *vs.* HF *C-V*)

p-type Si:



C-V Characteristic





a) accumulation: C_{ox}

b) flatband: ~C_{ox} (actually a bit less)

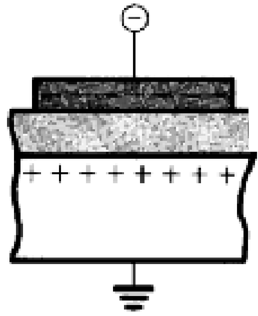
c) depletion: C_{ox} *in series* with the C_{depl}

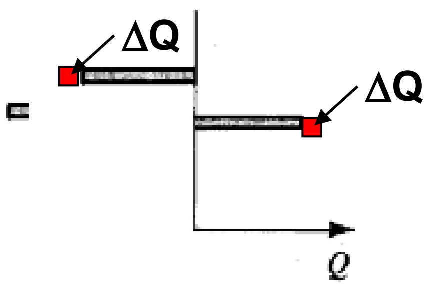
d) threshold: C_{ox} in series with the *minimum* C_{depl}

e) inversion: C_{ox} (with some time delay!)

Small signal charge response ΔQ due to ΔVG

Accumulation

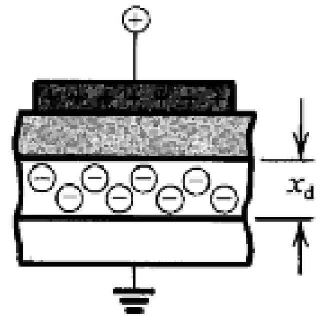


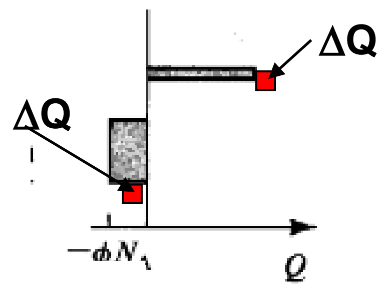


All frequencies

$C = C_{ox}$

Depletion

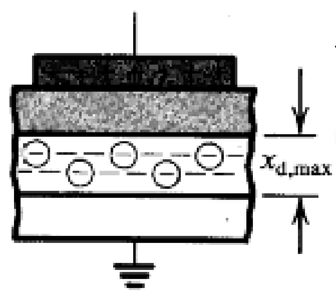


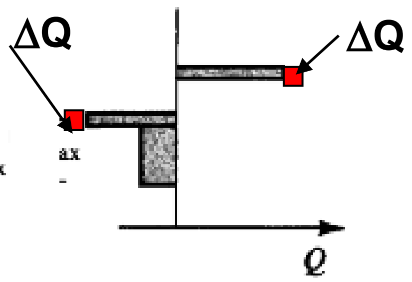


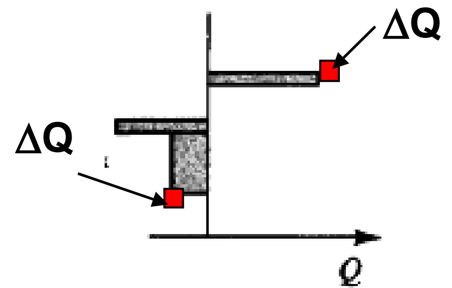
All frequencies

$1/C = 1/C_{ox} + x_d/\varepsilon_s$

Inversion







Key:
+ Holes
– Electrons
⊖ Acceptor ions

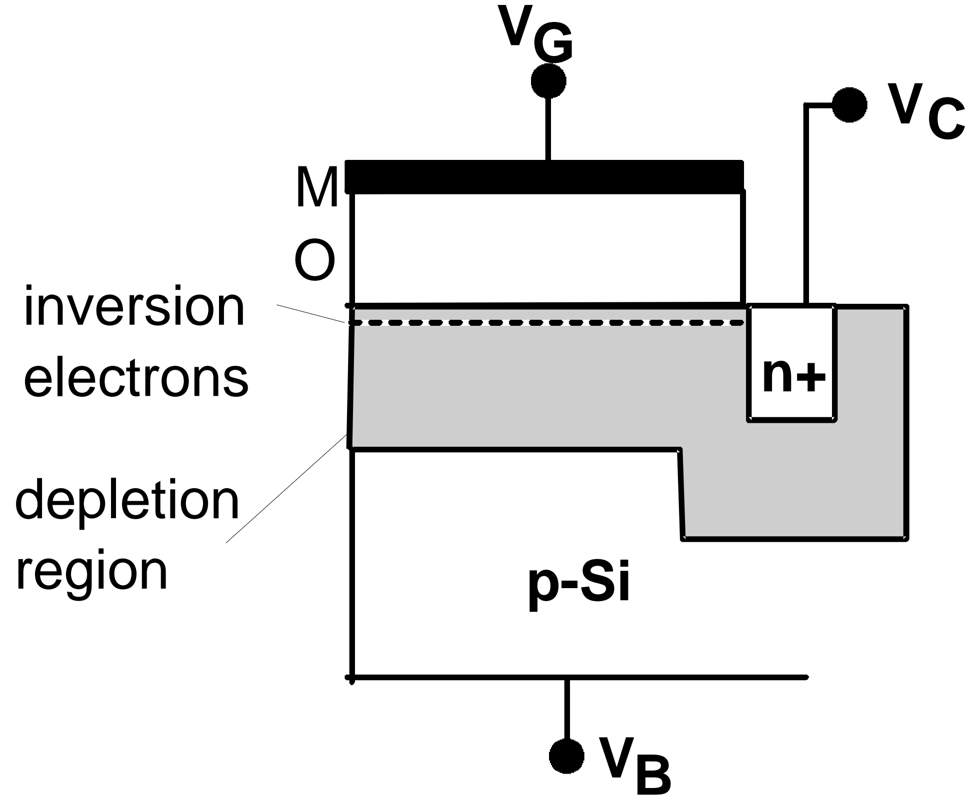
Low frequency

$C = C_{ox}$

High frequency

$1/C = 1/C_{ox} + x_{dmax}/\varepsilon_s$

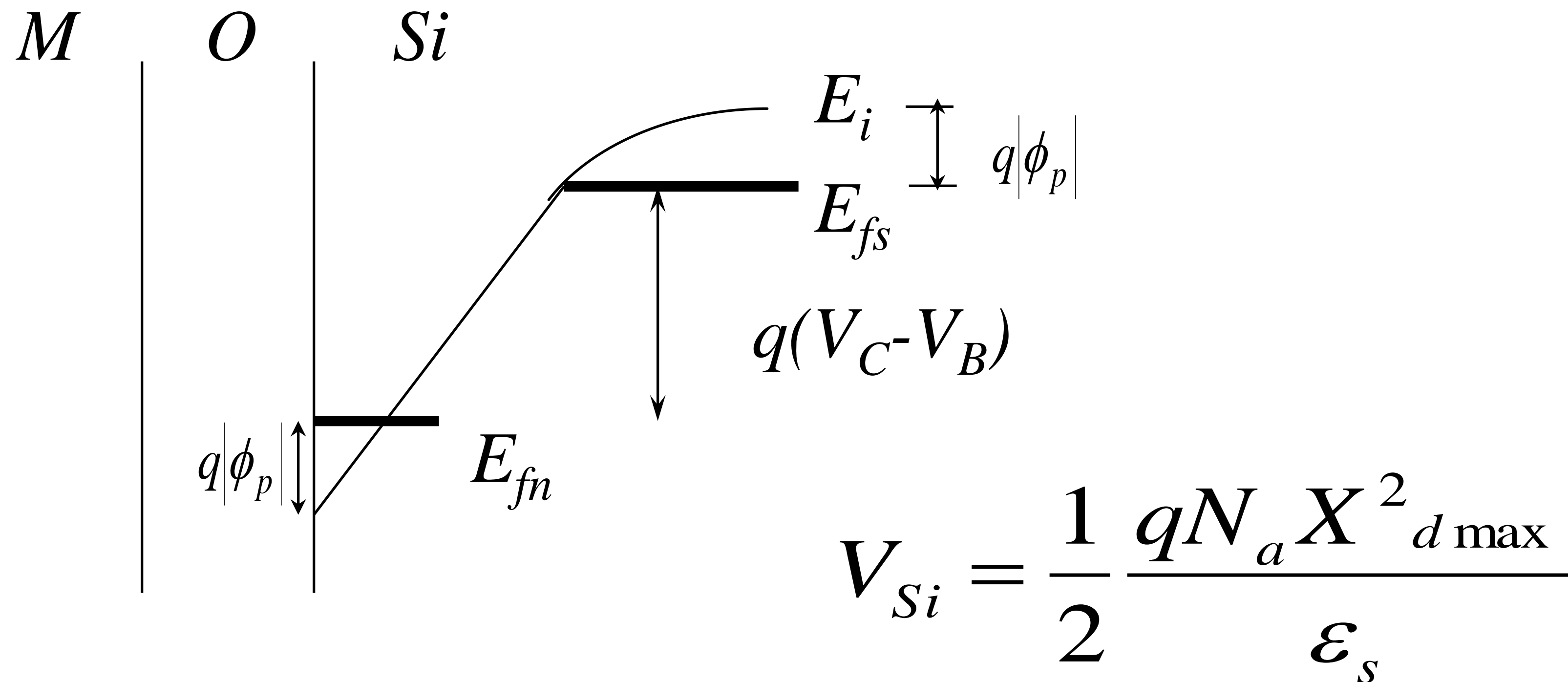
Effect of Substrate Bias V_B and Channel Bias V_C



$$\underbrace{(V_G - V_B)}_{\text{net bias across MOS}} = V_{FB} + V_{ox} + V_{Si}$$

net bias across MOS

At the onset of strong inversion, where V_G is defined as the threshold voltage



$$V_{Si} = \frac{1}{2}\frac{qN_a X^2_{d\max}}{\varepsilon_s}$$

$$V_{Si} = 2|\phi_p| + (V_C - V_B)$$

$$(V_G - V_B) = V_{FB} + \frac{qN_a X_{d\max}}{C_{OX}} + \frac{1}{2}\frac{qN_a X^2_{d\max}}{\varepsilon_s}$$

At threshold: $V_G - V_B = V_{FB} + V_{ox} + V_{Si}$

But $V_{Si} = 2|\Phi_p| + (V_C - V_B)$ =>

x_{dmax} is different from no-bias case

$$x_{d\max} = \sqrt{\frac{2\varepsilon_{Si} V_{Si}}{qN_B}}$$

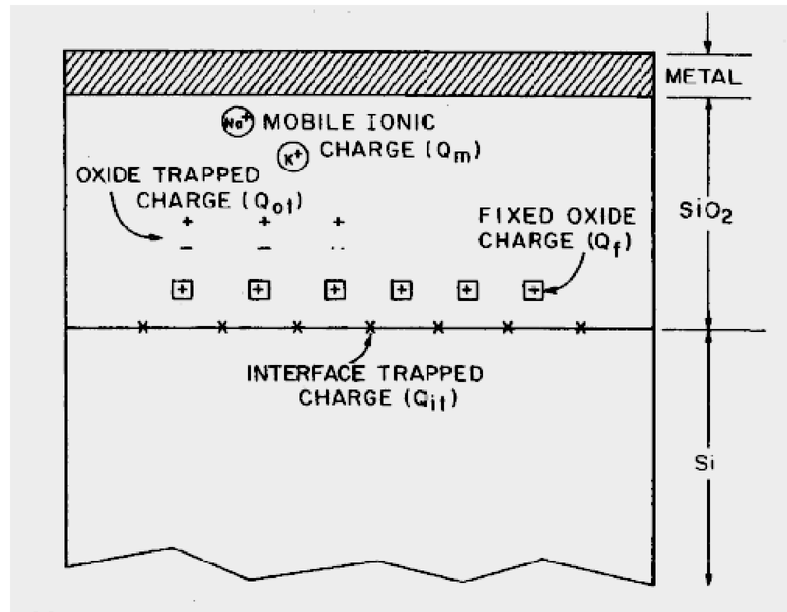
$$V_T - V_B = V_{FB} + \underbrace{\frac{\sqrt{2\varepsilon_s q N_B (2|\phi_F| + V_C - V_B)}}{C_{ox}}}_{V_{ox}} + \underbrace{2|\phi_F| + V_C - V_B}_{V_{Si}}$$

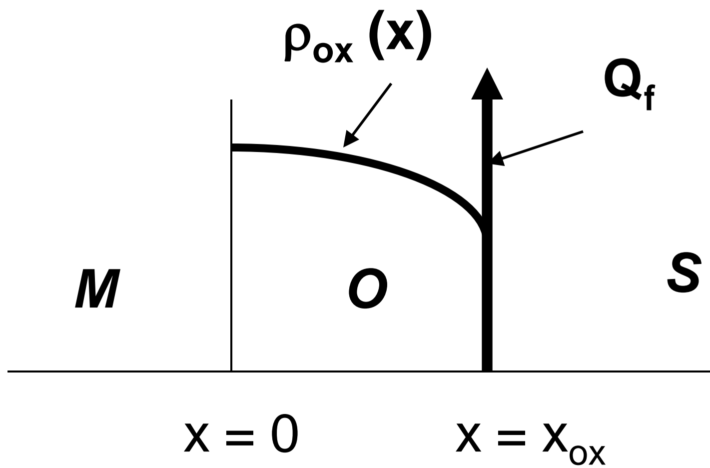
(The V_B terms on both sides are crossed out.)

Flat Band Voltage with Oxide charges

V_{FB} is the Gate voltage required to create no charge in the Si

$$V_{FB} \equiv \Phi_M - \Phi_S - \frac{Q_f}{C_{ox}} - \frac{1}{C_{ox}} \int_0^{x_{ox}} \frac{x \rho_{ox}(x)}{x_{ox}} dx$$

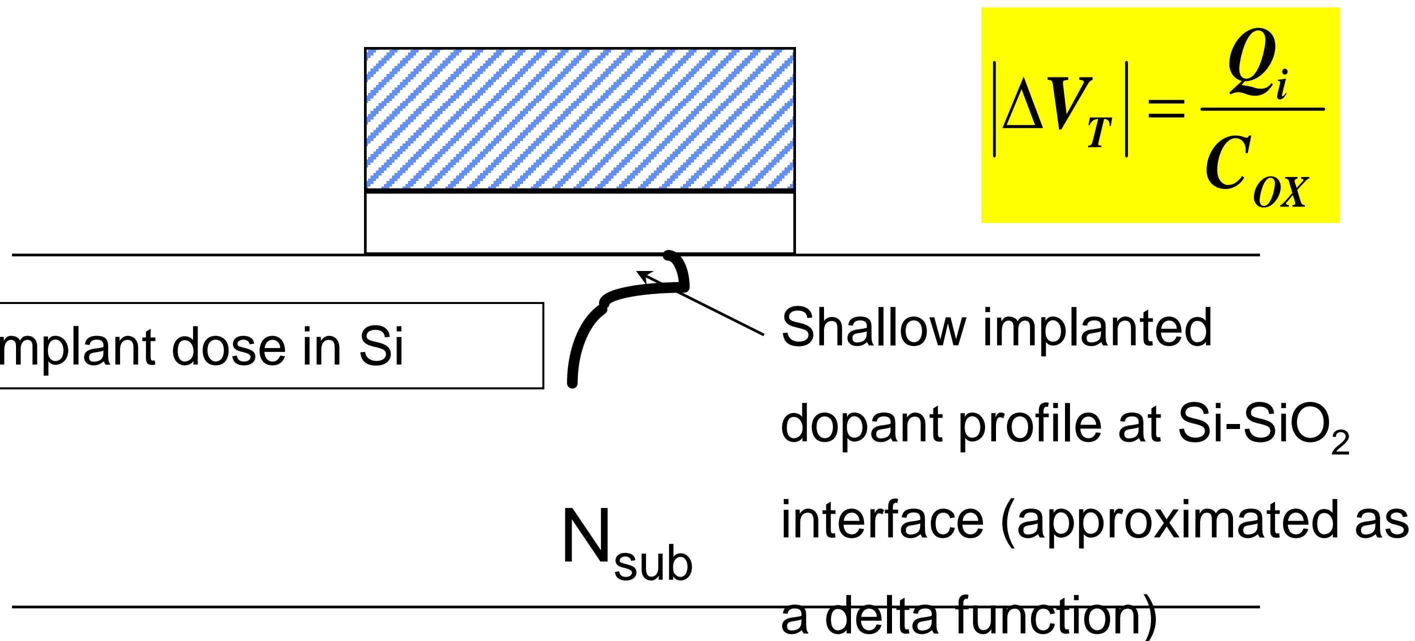




ρ_{ox} (x) due to alkaline contaminants or trapped charge

Q_f due to broken bonds at

V_T Tailoring with Ion Implantation



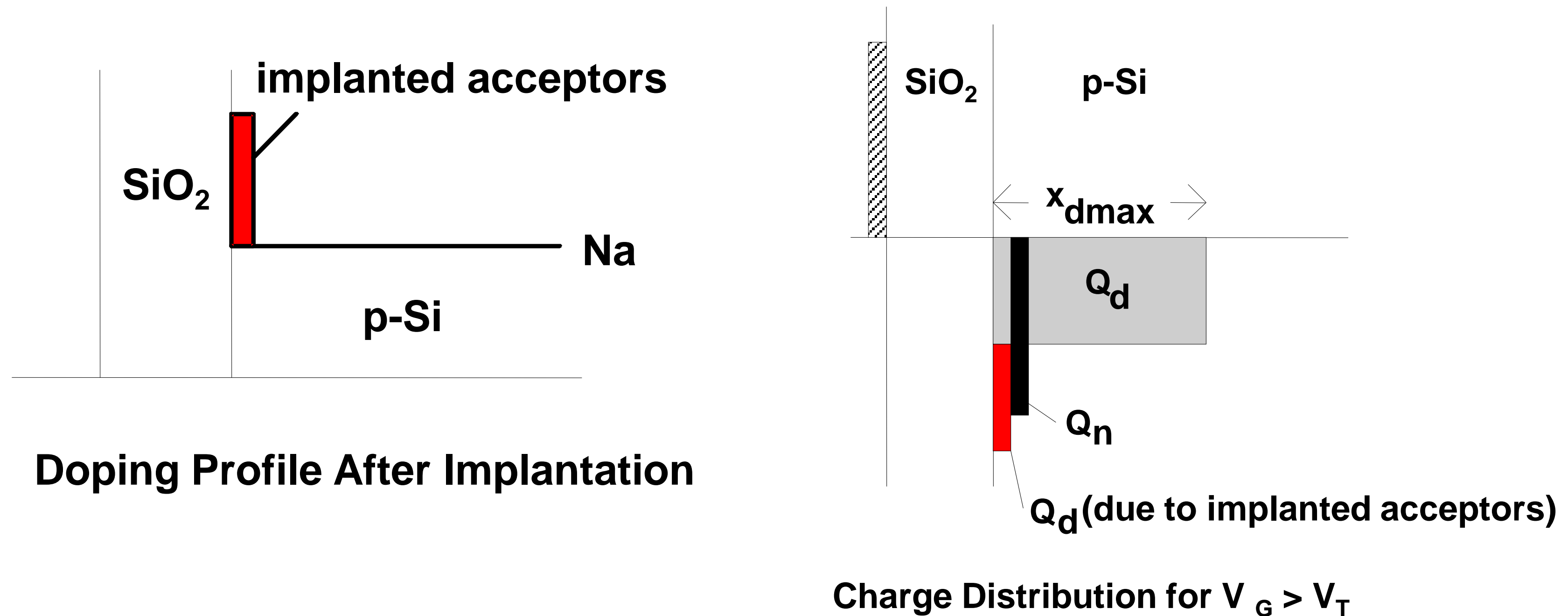
Q_i = q • implant dose in Si

- ***Acceptor*** implant gives positive shift (**+** ΔV_T)
- ***Donor*** implant gives negative shift **-** ΔV_T

Algebraic sign of V_T shift is independent of n or p substrate !

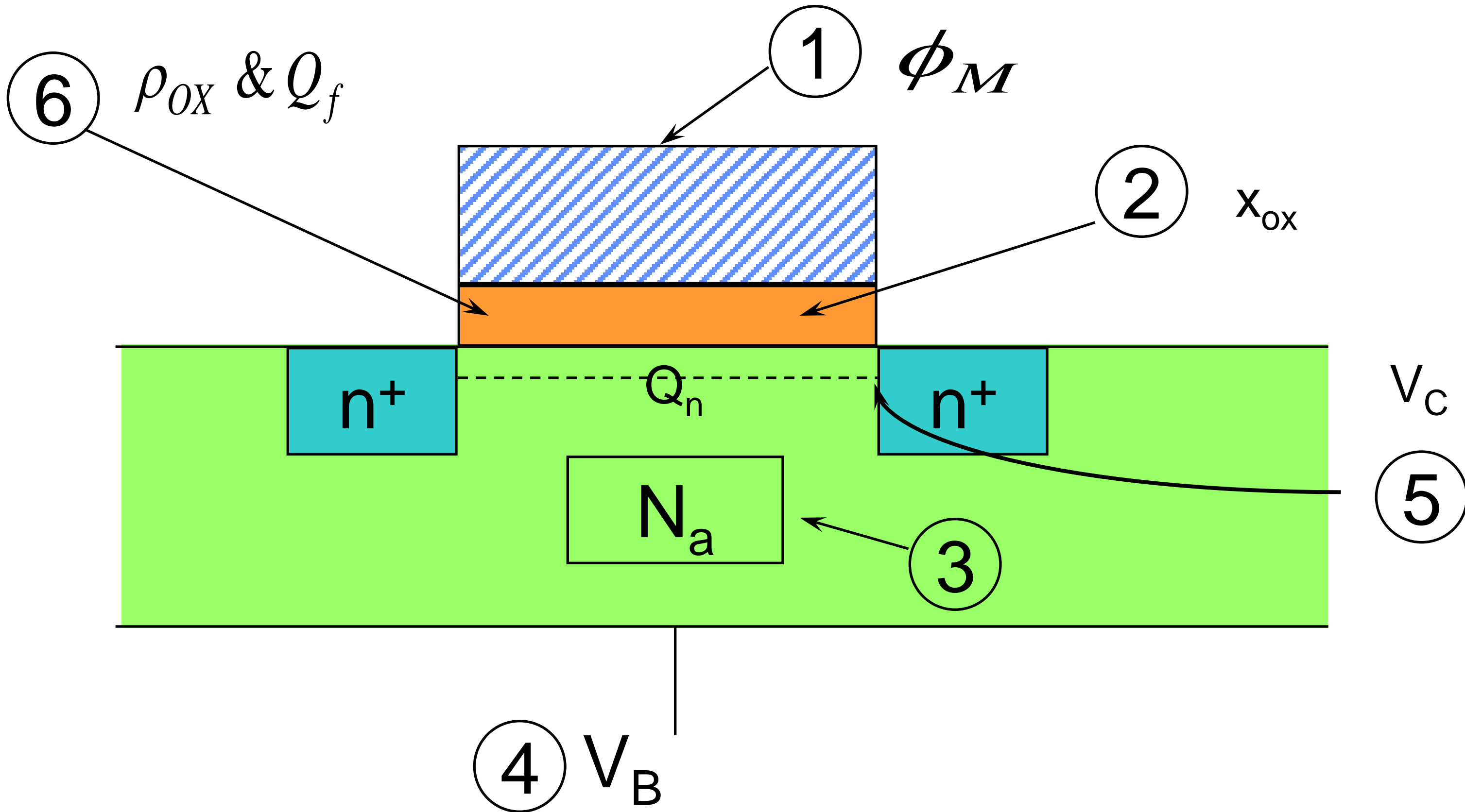
The delta-function approximation of implanted profile

* Valid if thickness of implanted dopants << x_{dmax}

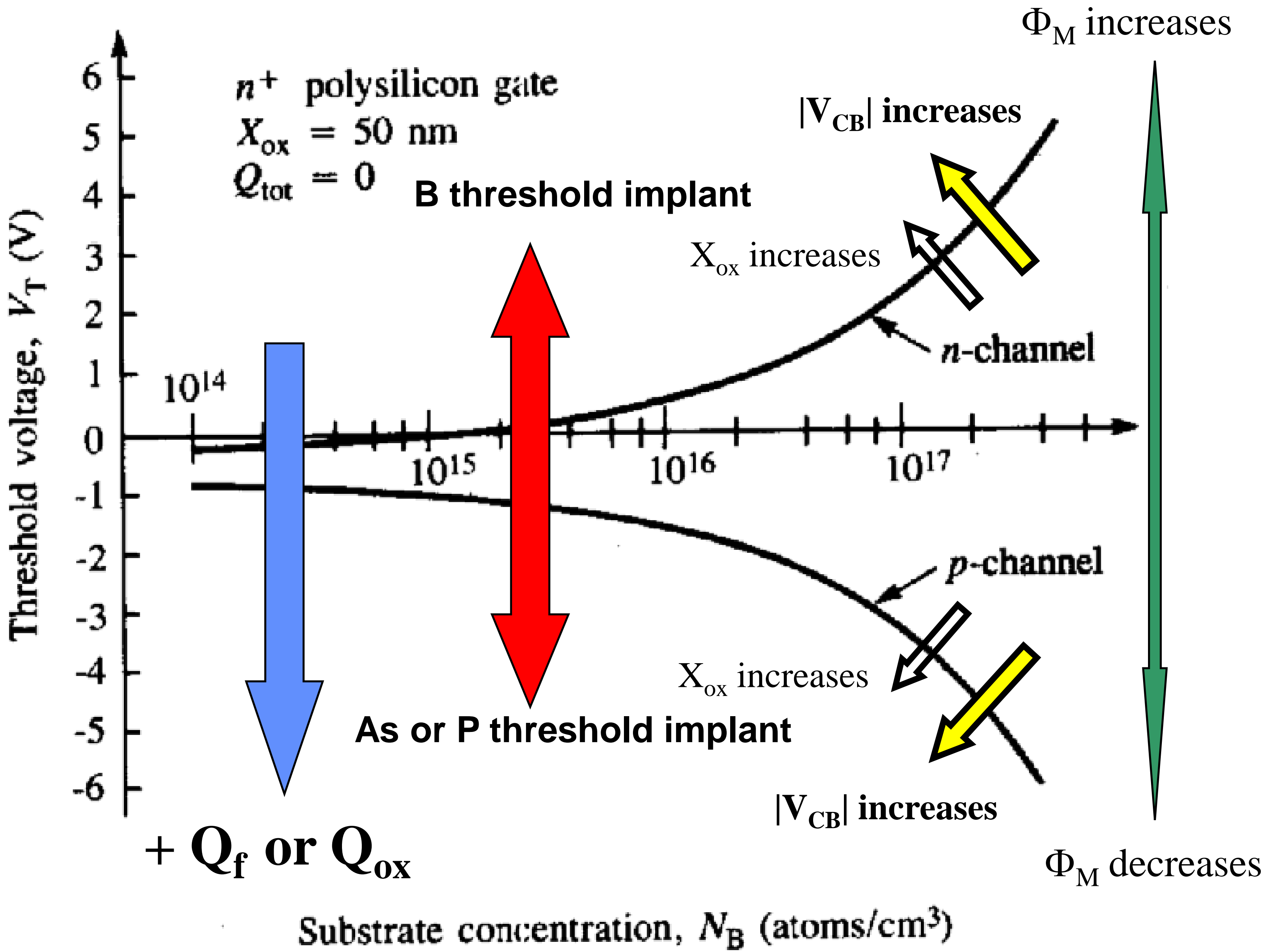


The V_T shift can be viewed as the extra gate voltage nee
deplete the implanted dopants ~ Q_i/C_{ox}

Summary : Parameters Affecting V_T



7 Dopant implant near Si/SiO_2 interface


Φ_M increases
n^+ polysilicon gate
X_{ox} = 50 nm
Q_{tot} = 0
B threshold implant
$|V_{CB}|$ increases
X_{ox} increases
n-channel
p-channel
X_{ox} increases
As or P threshold implant
$|V_{CB}|$ increases
Φ_M decreases
+ Q_f or Q_{ox}
Threshold voltage, V_T (V)
Substrate concentration, N_B (atoms/cm^3)
6
5
4
3
2
1
0
-1
-2
-3
-4
-5
-6
10^{14}
10^{15}
10^{16}
10^{17}

Summary of MOS Threshold Voltage (NMOS, p-substrate)

- Threshold voltage of MOS capacitor:

$$V_T = V_{FB} + \frac{\sqrt{2\varepsilon_s q N_B (2|\phi_F|)}}{C_{ox}} + 2|\phi_F| - \frac{Q_i}{C_{ox}}$$

- Threshold voltage of MOS transistor:

$$V_T = V_{FB} + \frac{\sqrt{2\varepsilon_s q N_B (2|\phi_F| + |V_C - V_B|)}}{C_{ox}} + 2|\phi_F| + V_C - \frac{Q_i}{C_{ox}}$$

Note 1: At the ***onset*** of strong inversion, inversion charge is negligible and is often ignored in the V_T expression

Note 2: V_T of a MOSFET is taken as the V_T value at source (i.e., $V_C = V_S$)

Note 3 : Q_i = (q • implant dose) is the charge due to the ionized donors or acceptors implanted at the Si surface. Q_i is ***negative*** for acceptors and is ***positive*** for donors

Summary of MOS Threshold Voltage (PMOS, n-substrate)

- Threshold voltage of MOS capacitor:

$$V_T = V_{FB} - \frac{\sqrt{2\varepsilon_s q N_B (2|\phi_F|)}}{C_{ox}} - 2|\phi_F| - \frac{Q_i}{C_{ox}}$$

- Threshold voltage of MOS transistor:

$$V_T = V_{FB} - \frac{\sqrt{2\varepsilon_s q N_B (2|\phi_F| + |V_C - V_B|)}}{C_{ox}} - 2|\phi_F| + V_C - \frac{Q_i}{C_{ox}}$$

* Yes, **+** sign for V_C term but V_C (<0) is a negative bias for PMOS because the inversion holes have to be negatively biased with respect to the n-substrate to create a reverse biased pn junction.