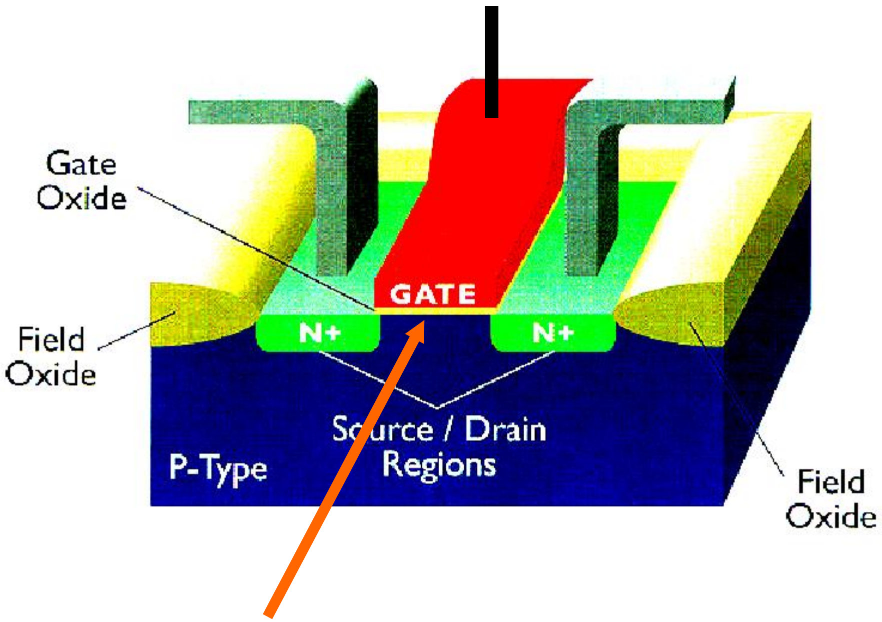
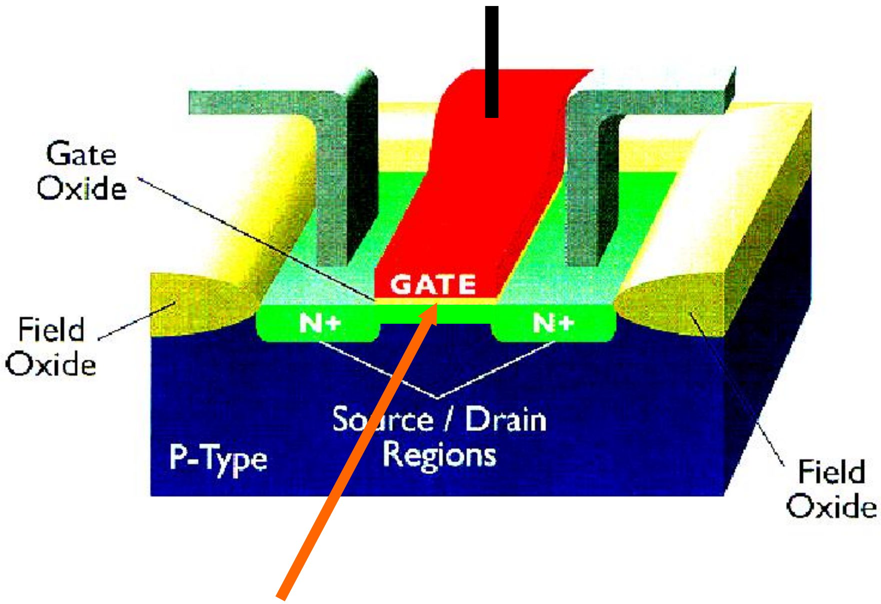
Metal -Oxide-Semiconductor Transistor [n-channel]

$$V_G < V_{threshold}$$



Negligible electron concentration underneath Gate region; Source-Drain is electrically open

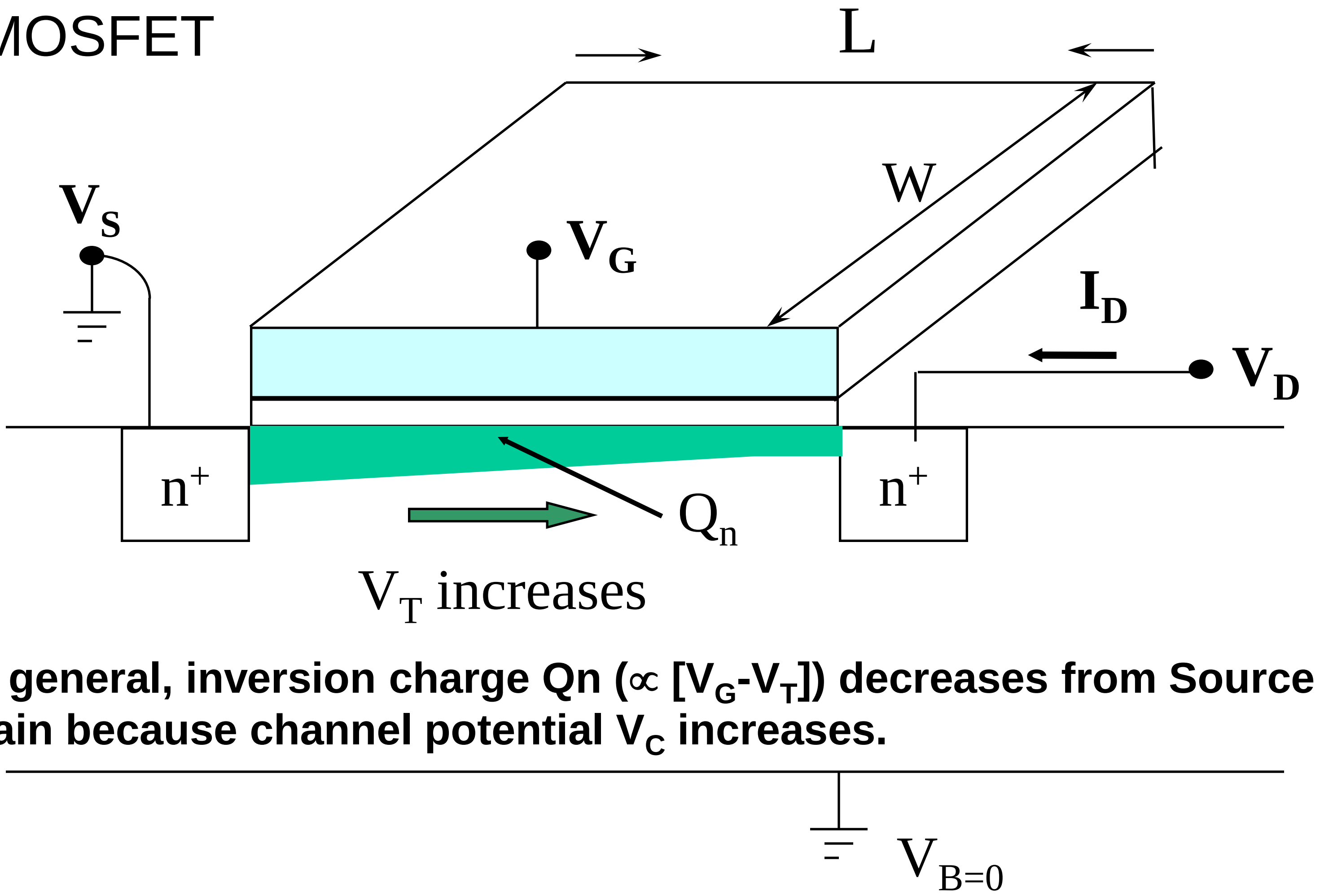
$$V_G > V_{threshold}$$



High electron concentration underneath Gate region; Source-Drain is electrically connected

MOSFET I-V Analysis

N-MOSFET



- **In general, inversion charge Qn (∝ [V_G-V_T]) decreases from Source toward Drain because channel potential V_C increases.**

Approximate Analysis

Inversion layer thickness **Inversion layer concentration**

$$I_D = W\mathbf{t} \bullet (-q\ \ \mathbf{n}\ v_{drift})$$
$$= W \bullet \mathbf{Q_n} \bullet v_{drift}$$

Note: I_D is constant for all positions along channel

Let V_T **defined** to be threshold voltage at Source

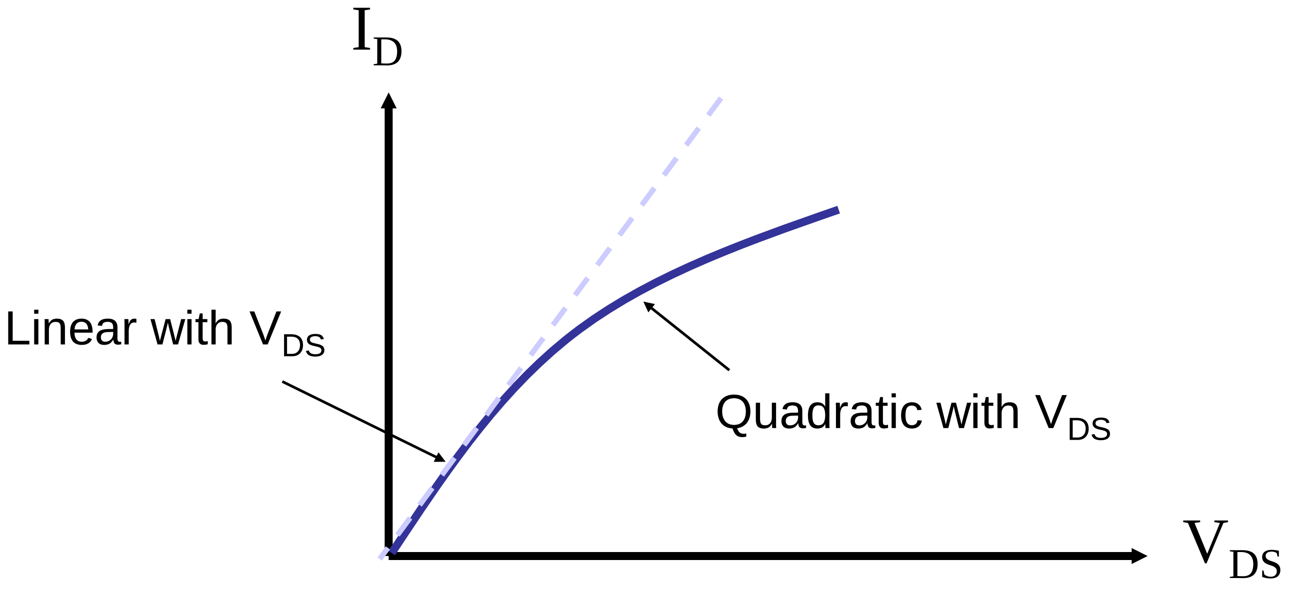
$$\mathbf{V_T(average) \sim V_T + \frac{V_{DS}}{2}}$$

[This is an approximation]

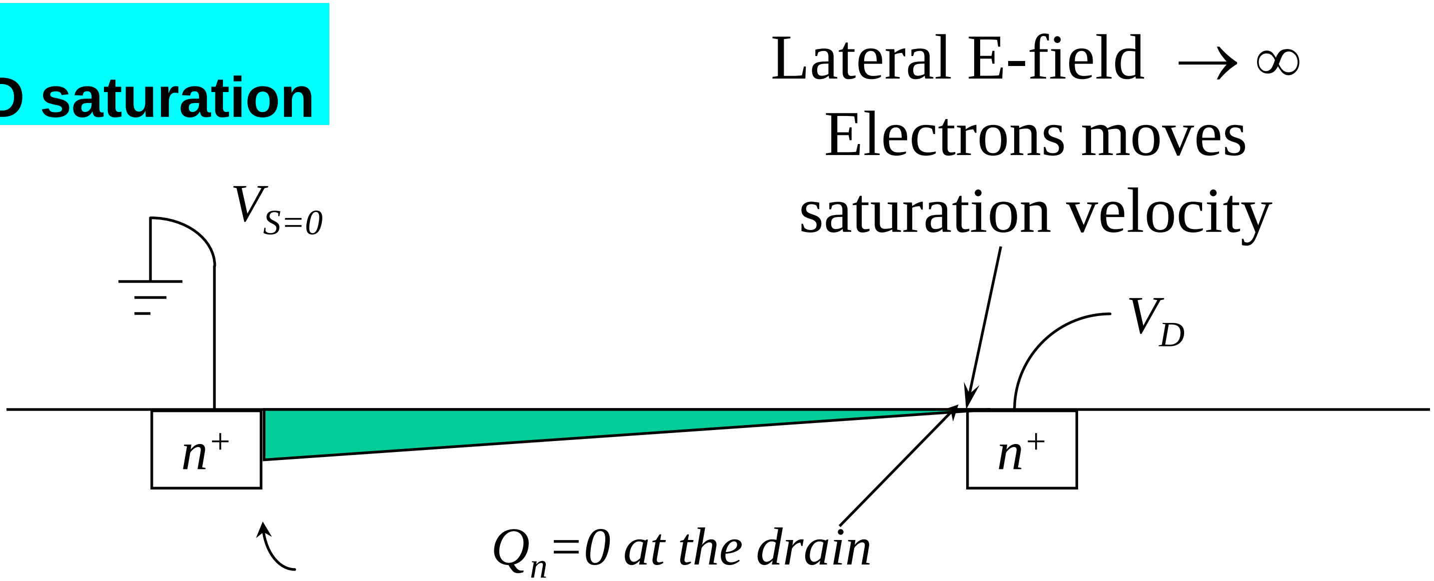
$$\mathbf{Q_n\,(average) = C_{OX}\left(V_G - V_T(average)\right)}$$
$$\mathbf{= C_{OX}\left(V_G - V_T - \frac{V_{DS}}{2}\right)}$$

$$\textbf{With } v_{drift} = -\mu_n E \approx \frac{\mu_n V_{DS}}{L}$$

$$I_D = \mu \frac{W}{L} C_{OX}\left(V_G - V_T - \frac{V_{DS}}{2}\right) V_{DS}$$



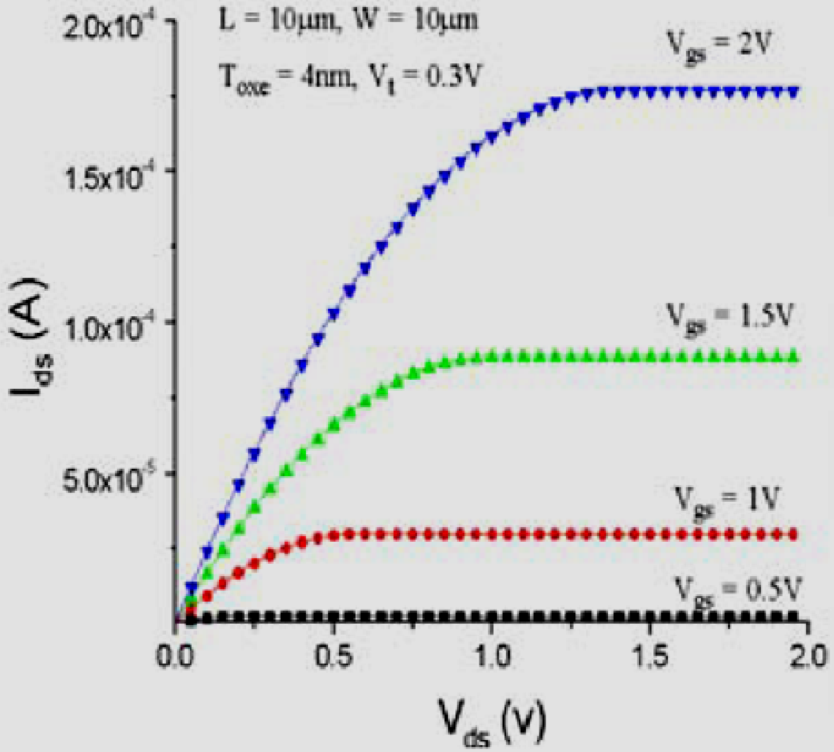
$V_{D\ saturation}$


Lateral E-field → ∞
Electrons moves saturation velocity

V_{Dsat} is *defined* to be the value of V_D with Q_n=0 *at drain.*

From $Q_n = C_{ox}(V_G - V_T - V_D)$, we get $V_{Dsat} = V_G - V_T$

Saturation Current



- saturation region:

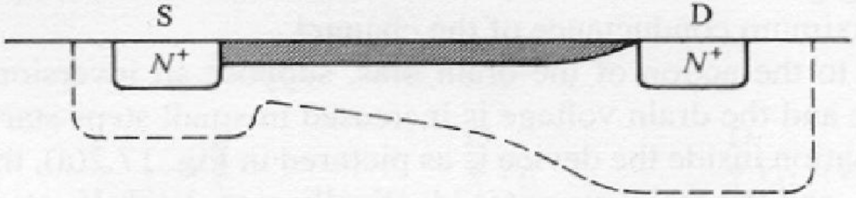
$$V_D \geq \boxed{V_{Dsat} = V_{GS} - V_T}$$

$$\boxed{I_{Dsat} = \frac{W}{2L} C_{oxe} \mu_{eff} (V_{GS} - V_T)^2}$$

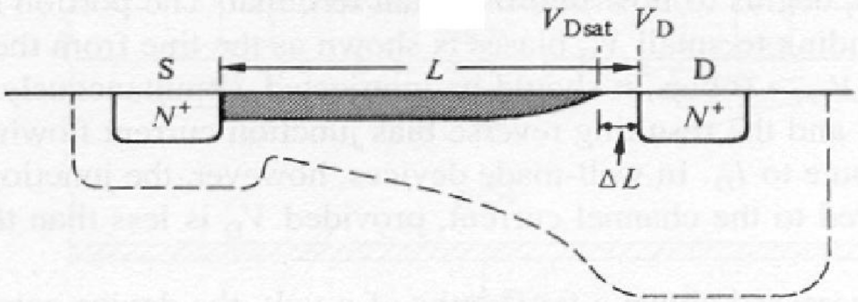
Pinch-Off & Channel-Length Modulation

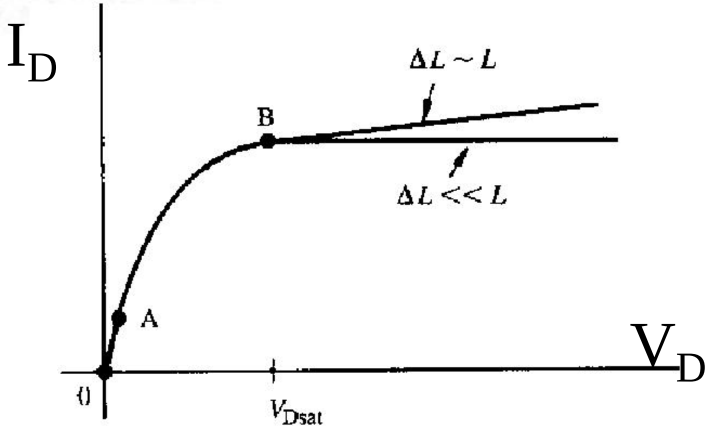
$V_{GS} > V_T$:

$V_{DS} = V_{GS} - V_T$



$V_{DS} > V_{GS} - V_T$





MOSFET I-V Characteristics Summary

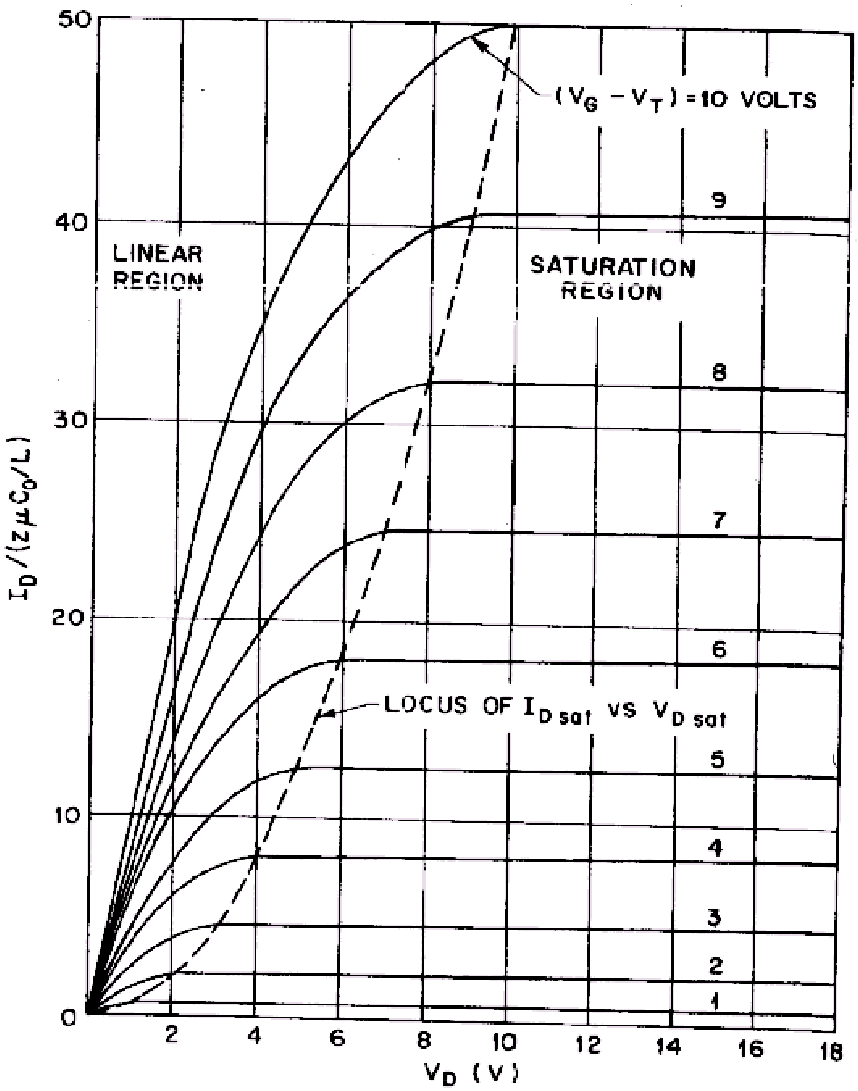
For $V_D < V_{Dsat}$

$$I_D = \frac{\mu_n W}{L} C_{OX}\left(V_G - V_T - \frac{V_{DS}}{2}\right)V_{DS}$$

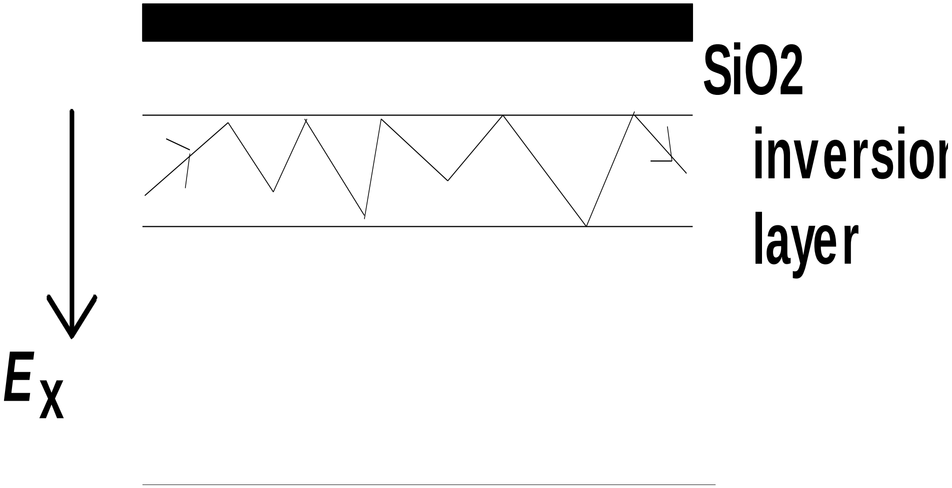
For $V_D > V_{Dsat}$

$$I_D = I_{Dsat} = \frac{\mu_n W}{2L} C_{OX}\left(V_G - V_T\right)^2$$

Note: $V_{Dsat} = V_G - V_T$



Mobility of inversion charge carriers



*Carrier will experience additional scattering at the Si/SiO2 interface

*Channel mobility is lower than bulk mobility

* μ(effective) is extracted from MOSFET I-V characteristics
* Typically ~0.5 of μ(bulk)

I_D vs. V_{DS} Characteristics

The MOSFET I_D-V_{DS} curve consists of two regions:

1) Resistive or “Triode” Region: $0 < V_{DS} < V_{GS} - V_T$

$$I_D = k_n' \frac{W}{L}\left[V_{GS} - V_T - \frac{V_{DS}}{2}\right]V_{DS}$$

where $k_n' = \mu_n C_{ox}$

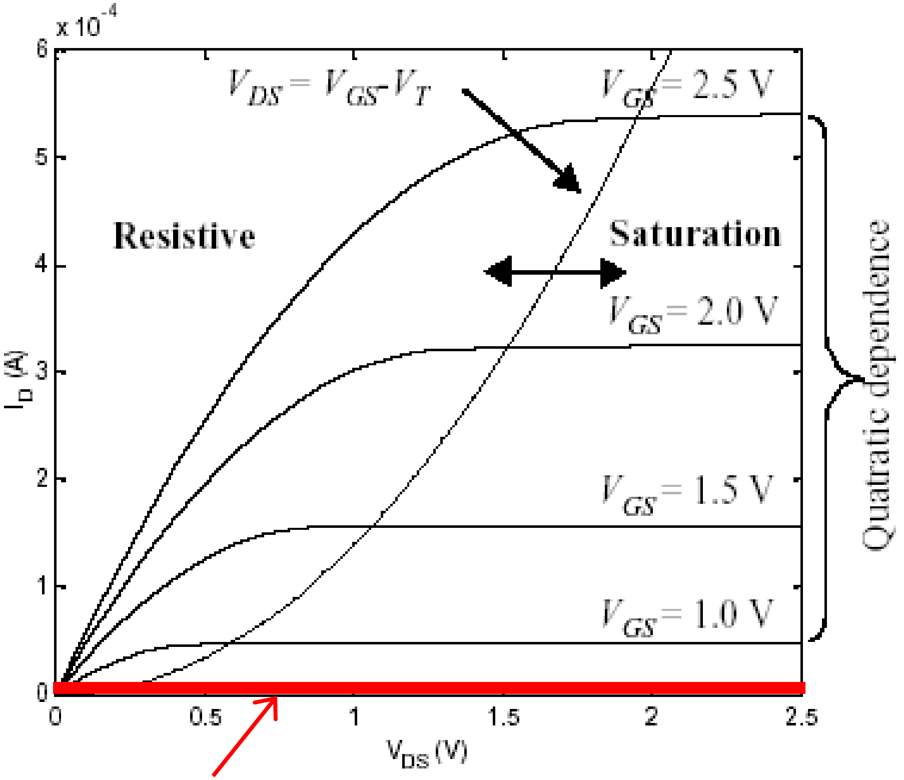
process transconductance parameter

2) Saturation Region:

$V_{DS} > V_{GS} - V_T$

$$I_{DSAT} = \frac{k_n'}{2}\frac{W}{L}\left(V_{GS} - V_T\right)^2$$

where $k_n' = \mu_n C_{ox}$

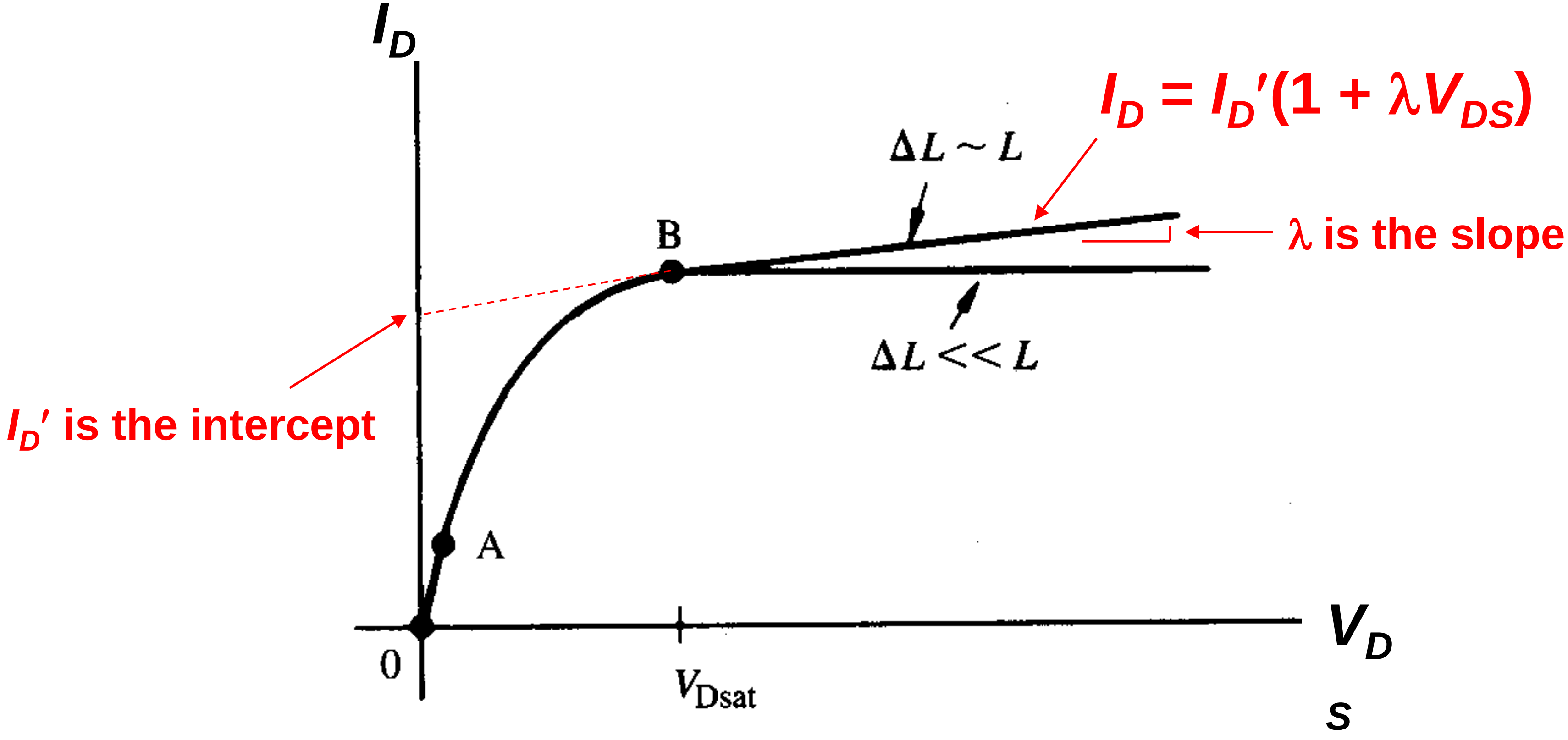


“CUTOFF” region: $V_G < V_T$

Channel-Length Modulation

If *L* is small, the effect of *ΔL* to reduce the inversion-layer “resistor” length is significant

→ I_D increases noticeably with *ΔL* (*i.e.* with V_{DS})



$I_D = I_D'(1 + \lambda V_{DS})$

λ is the slope

I_D' is the intercept

N-Channel MOSFET Summary

V_{DS} and V_{GS} normally positive values

- $V_{GS} < V_t$: cut off mode, $I_{DS}=0$ for any V_{DS}
- $V_{GS} > V_t$: transistor is turned on

1) $V_{DS} < V_{GS}-V_t$: Triode Region

$$\mathbf{i_D = \frac{W}{L} \bullet \frac{KP}{2}\left[2(v_{GS} - V_t)v_{DS} - v_{DS}{}^2\right]}$$

2) $V_{DS} > V_{GS} - V_t$: Saturation Region

$$\mathbf{i_D = \frac{W}{L} \bullet \frac{KP}{2}\left[2(v_{GS} - V_t)^2\right]}$$

Boundary between Triode and Saturation Regions

$$v_{GS} - V_t = v_{DS}$$

P-Channel MOSFET Summary

v_{DS} and v_{GS} normally negative values

- $v_{GS} > V_t$:cut off mode, $I_{DS}=0$ for any V_{DS}
- $v_{GS} < V_t$:transistor is turned on

1) $v_{DS} > V_{GS}-V_t$: Triode Region

$$i_D = \frac{W}{L} \bullet \frac{KP}{2}\left[2(v_{GS} - V_t)v_{DS} - v_{DS}^{\;2}\right]$$

2) $v_{DS} < v_{GS}-V_t$: Saturation Region

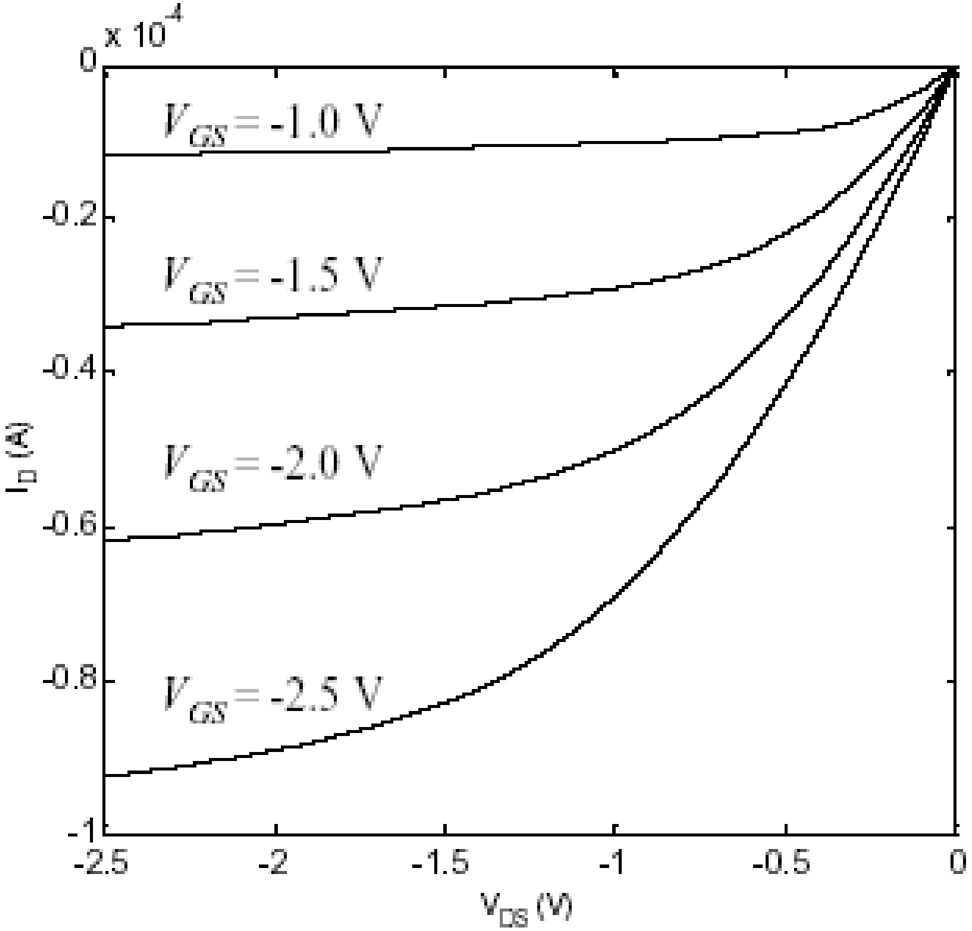
$$i_D = \frac{W}{L} \bullet \frac{KP}{2}\left[2(v_{GS} - V_t)^2\right]$$

Boundary

$$v_{GS} - V_t = v_{DS}$$

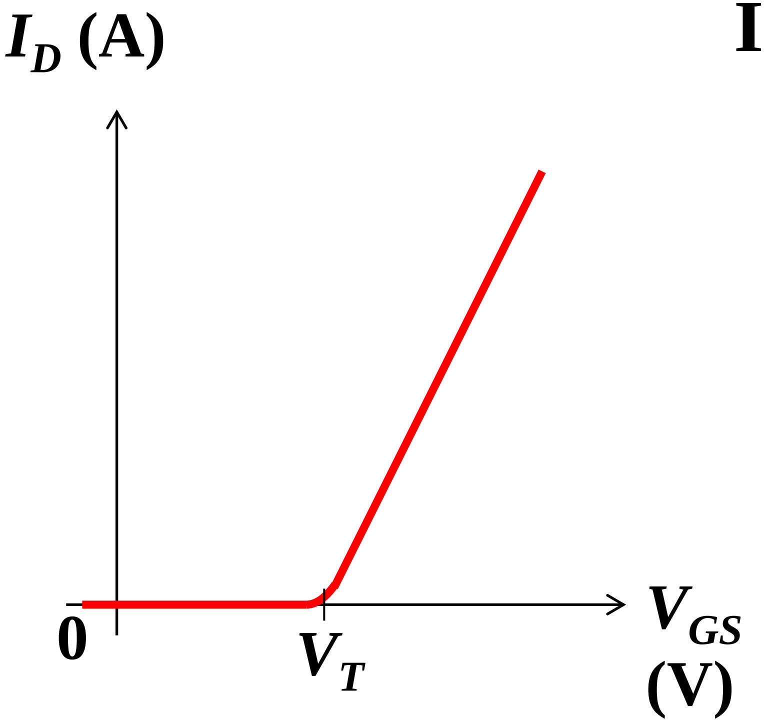
P-Channel MOSFET I_D *vs.* V_{DS}

- As compared to an n-channel MOSFET, the signs of all the voltages and the currents are reversed:



MOSFET V_T Measurement

- V_T can be determined by plotting I_D *vs.* V_{GS}, using a low value of V_{DS} :



$$I_D = K[2(V_{GS} - V_T) - V_{DS}]V_{DS}$$

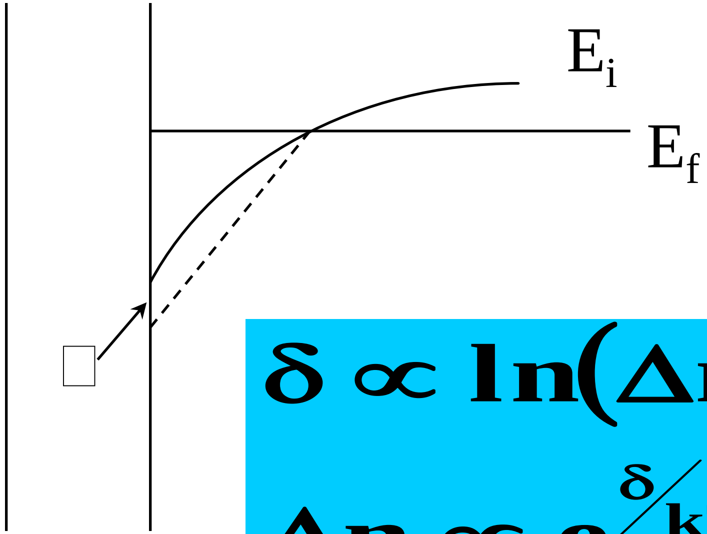
Why x_{dmax} ~ constant beyond onset of strong inversion ?

$$V_G = V_{FB} + V_{OX} + V_{Si}$$

Higher than V_T

Picks up all the changes in V_G

Approximation assumes
V_{Si} does not change much



$$\boldsymbol{\delta \propto \ln(\Delta n)}$$

$$\boldsymbol{\Delta n \propto e^{\delta/kT}}$$

Justification:
If surface electron density changes by □n

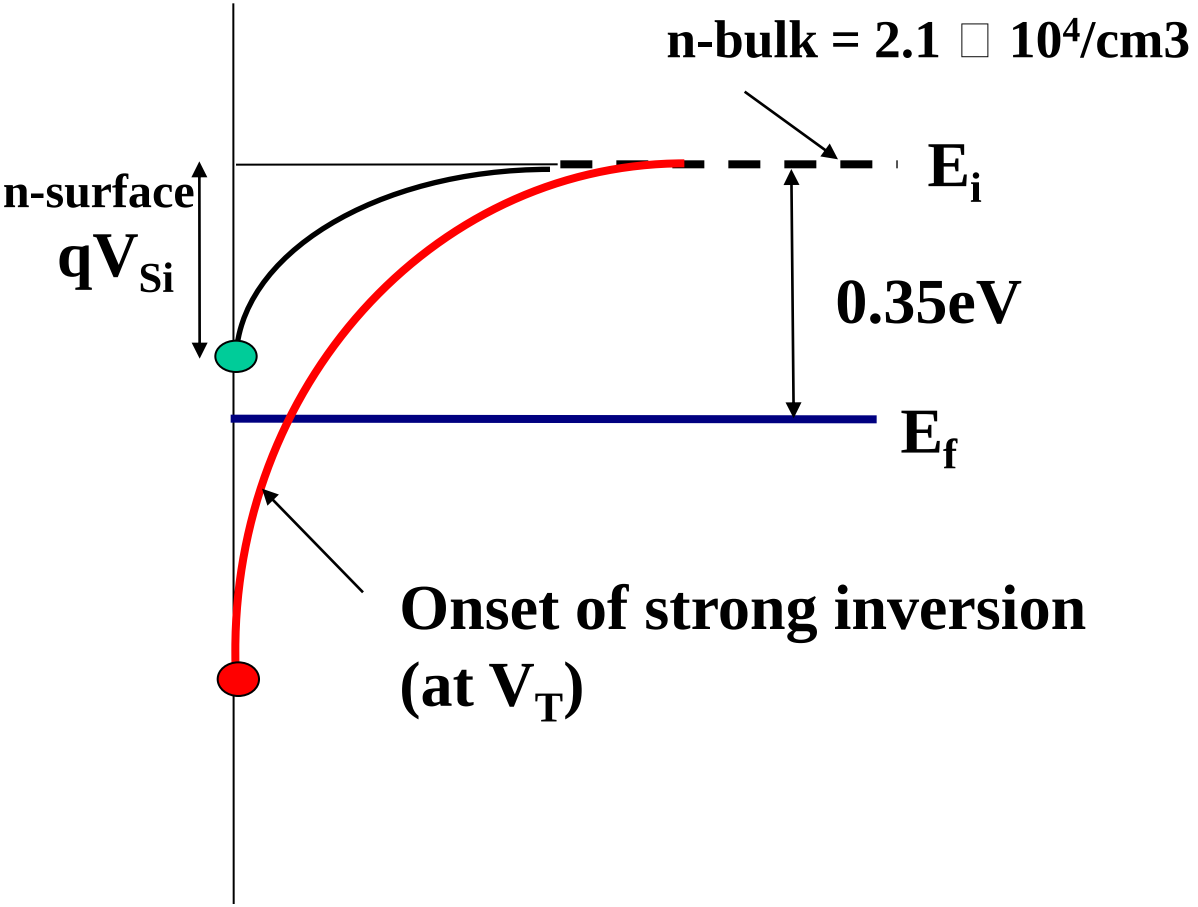
$$\Delta V_{OX} \propto \frac{\Delta n}{C_{OX}}$$

but the change of V_{Si} changes only by kT/q [ln (□n)] – **small**!

n-surface = n-bulk □ $e^{qVSi/kT}$

p-Si

$N_a=10^{16}$/cm3



n-bulk = 2.1 □ 10^4/cm3

E_i

n-surface

qV_{Si}

0.35eV

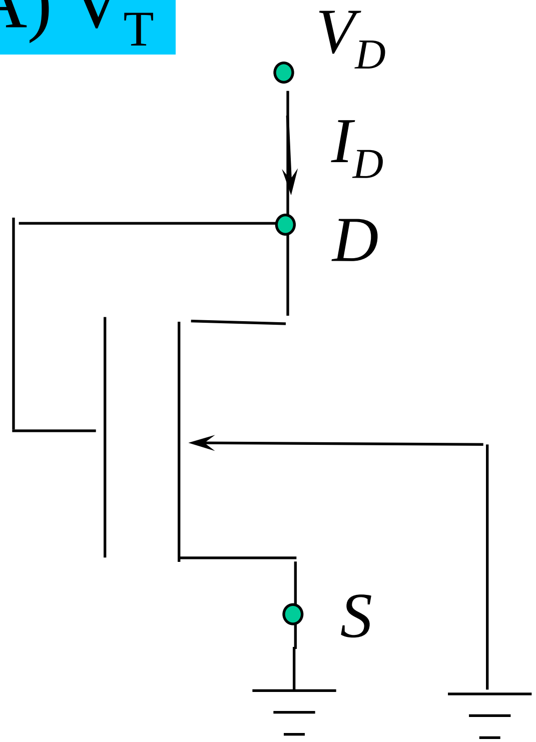
E_f

Onset of strong inversion (at V_T)

VSi	n-surface
0	2.10E+04
0.1	9.84E+05
0.2	4.61E+07
0.3	2.16E+09
0.4	1.01E+11
0.5	4.73E+12
0.6	2.21E+14
0.7	**1.04E+16**
0.8	4.85E+17
0.9	2.27E+19

Parameter Extraction from MOSFET I-V

(A) V_T



$$For\, V_D = V_G > V_T$$

$$V_T^{'}\; at\, drain$$

$$= V_{FB} + V_D + 2\left|\phi_p\right|$$

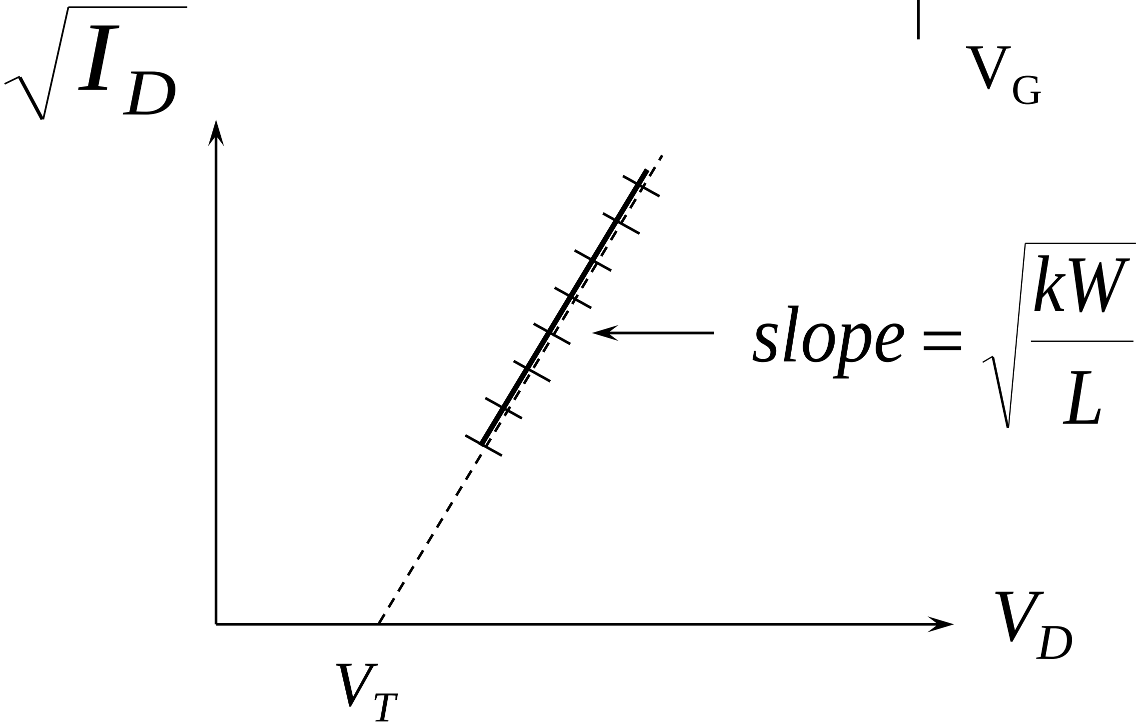
$$+ \frac{1}{C_{OX}}\sqrt{2\varepsilon_s q N_a\left(2\left|\phi_p\right| + V_D\right)}$$

$$\Rightarrow V_G - V'_T < 0$$

$$\Rightarrow Drain\, is\, at\; pinch - off$$

$$\Rightarrow MOSFET\; is\, in\, saturation\, mode.$$

$$\therefore I_D = I_{Dsat} = \overset{\mu_n C_{OX}}{k}\,\frac{W}{L}\left(\underset{V_G}{V_D} - V_T\right)^2$$



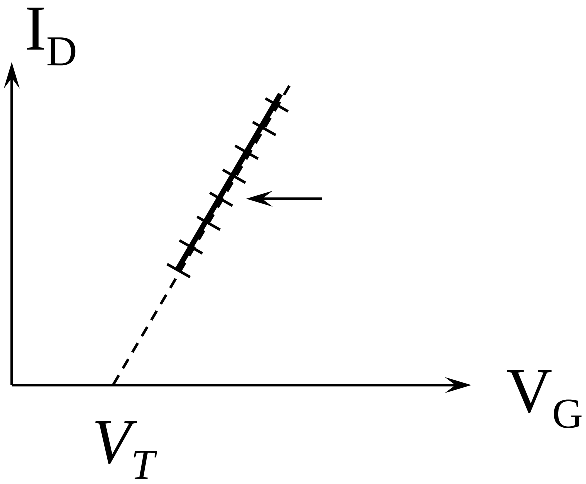
$$slope = \sqrt{\frac{kW}{L}}$$

Alternative way to extract V_T

- Measure I_D versus V_G for a **fixed** ***small*** V_{DS} (say <100mV)

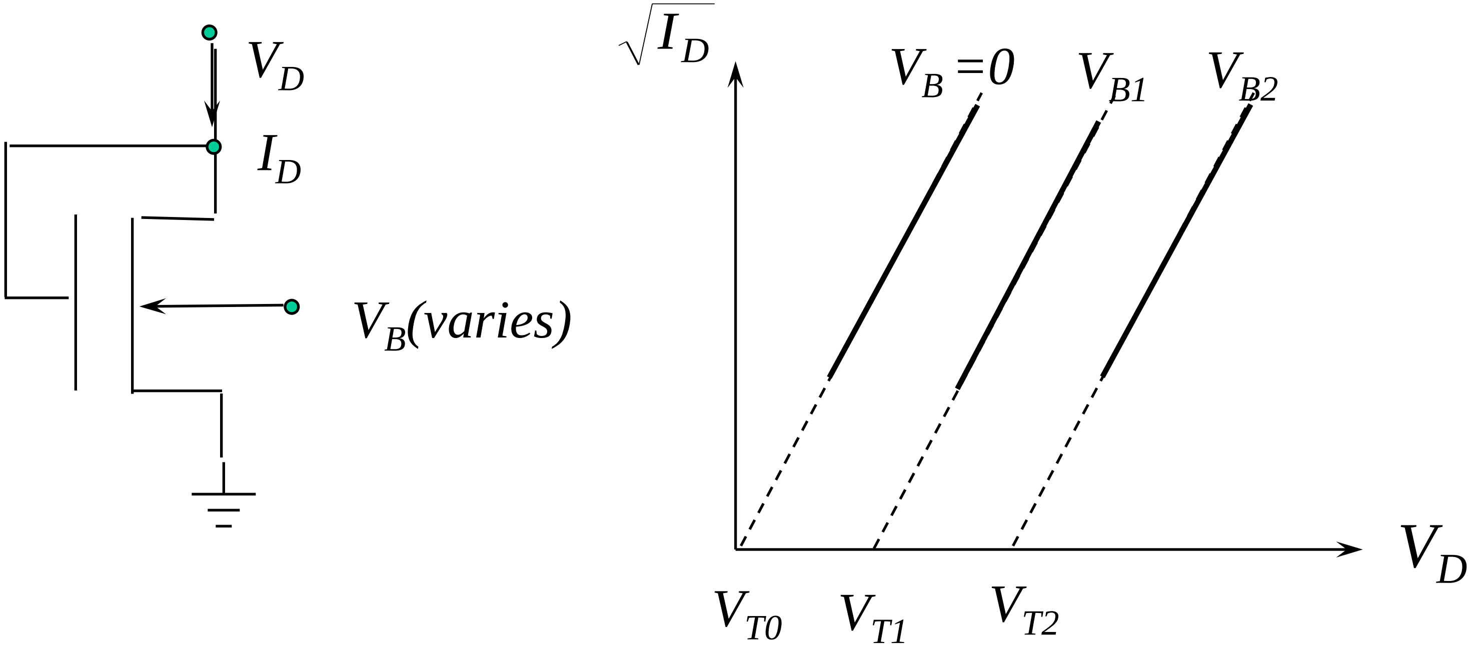
$$I_D = \frac{\mu_n W}{L} C_{OX}\left(V_G - V_T - \cancel{\frac{V_{DS}}{2}}\right)V_{DS}$$

$$\approx \frac{\mu_n W}{L} C_{OX}\left(V_G - V_T\right)V_{DS}$$



The intercept of I_D versus V_G plot on V_G-axis is V_T.

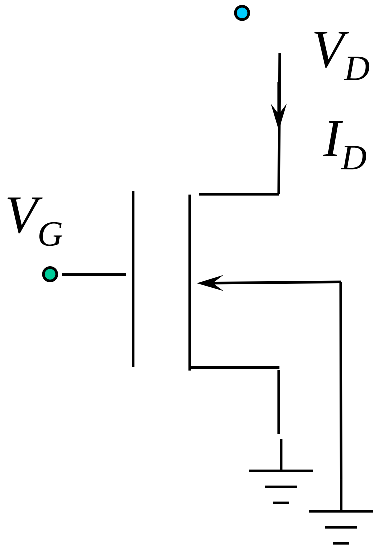
(B) Body Coefficient γ

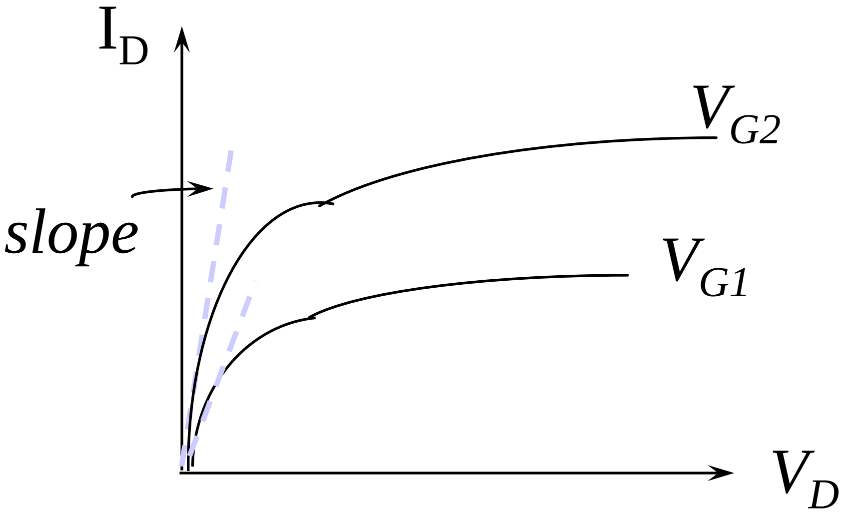


$$\gamma \equiv \left[\frac{V_T\left(with\, V_{SB} \neq 0\right) - V_T\left(with\, V_{SB} = 0\right)}{\sqrt{2\left|\phi_p\right| + \left|V_{SB}\right|} - \sqrt{2\left|\phi_p\right|}} \right]$$

$$= \frac{\sqrt{2\varepsilon_s q N_a}}{C_{OX}}$$

(C) $\mu_n C_{OX} \frac{W}{L}$



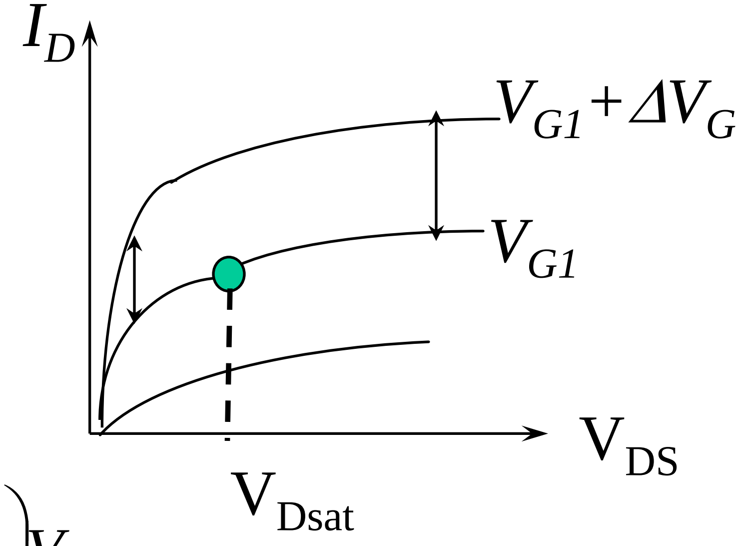


$$I_D = \mu_n \frac{W}{L} C_{OX} \left(V_G - V_T - \frac{V_D}{2} \right) V_D$$

$$\frac{\partial I_D}{\partial V_D} = \mu_n C_{OX} \frac{W}{L} (V_G - V_T) \ \text{for small } V_D$$

(D) Transconductance g_m

$$g_m \equiv \left.\frac{\partial I_D}{\partial V_G}\right|_{fixed\, V_D}$$



(a) For $V_{DS}<V_{Dsat}$

$$I_D = \frac{\mu_n W}{L} C_{OX}\left(V_G - V_T - \frac{V_{DS}}{2}\right)V_{DS}$$

$$\therefore \frac{\partial I_D}{\partial V_G} = \mu_n C_{OX}\frac{W}{L}\cdot V_{DS}$$

[g_m varies with V_{DS}]

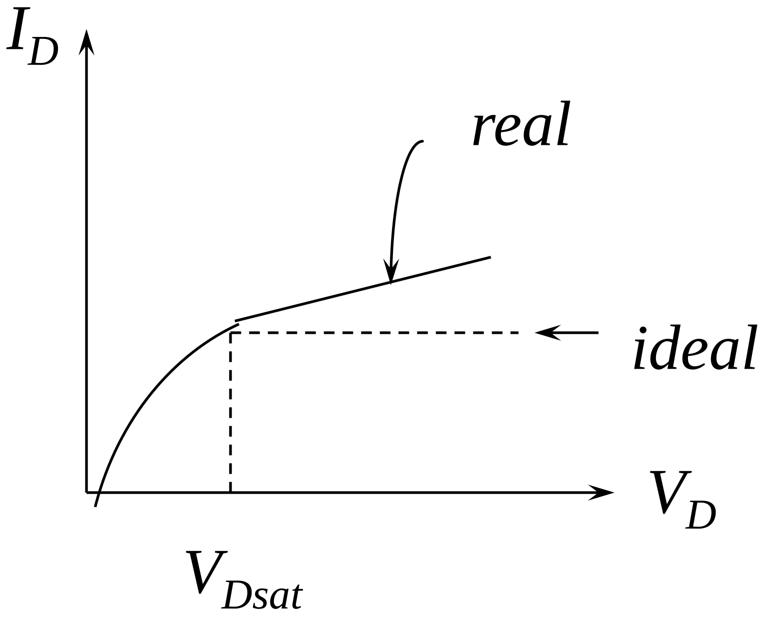
(b) For $V_{DS} > V_{Dsat}$

$$I_D = I_{Dsat} = \frac{\mu_n W}{2L} C_{OX}(V_G - V_T)^2$$

$$\frac{\partial I_D}{\partial V_G} = \frac{\mu_n W}{L} C_{OX}\cdot(V_G - V_T)$$

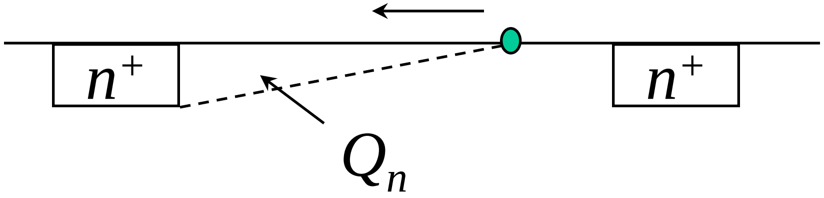
[g_{msat} varies with V_G]

(E) Channel Modulation Parameter λ

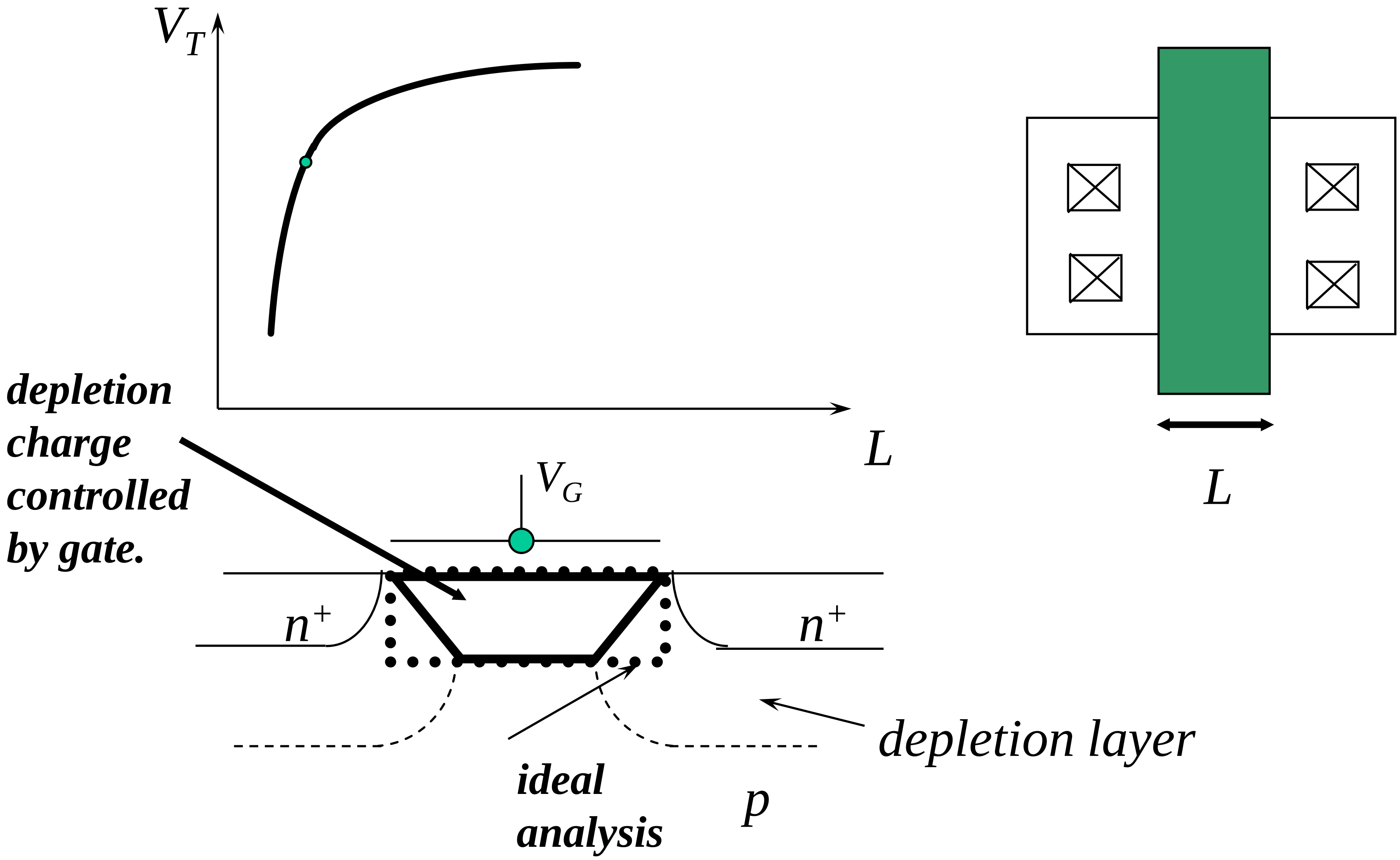


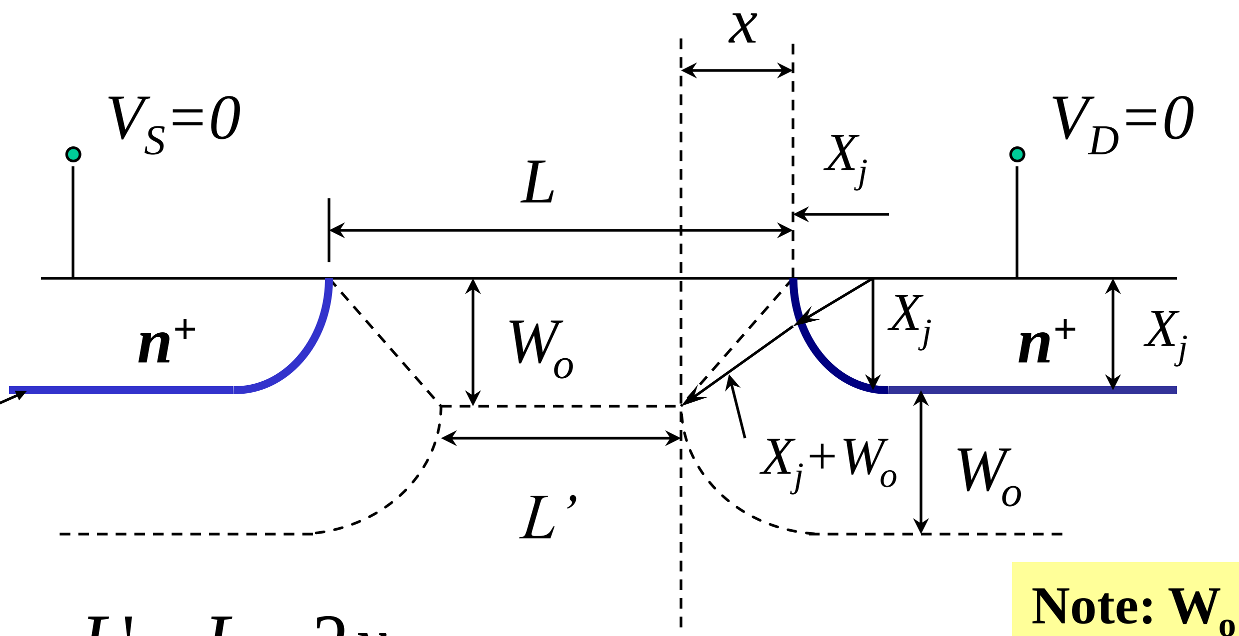
$$I_{Dsat} = \frac{k}{2}\left(V_G - V_T\right)^2\left(1 + \lambda V_{DS}\right)$$

$$Typically\ \lambda \sim 0.1\, to\, 0.01 (volt)^{-1}$$



Short Channel Effect on V_T





Same electric potential because of heavily doped n+

Note: W_o is x_{dmax}

$$L' = L - 2x$$

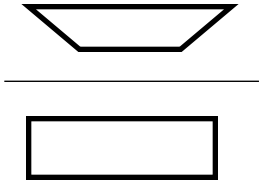
$$= L - 2\left[\sqrt{\left(X_j + W_o\right)^2 - W_o^{\,2}} - X_j\right]$$

$$= L - 2X_j\left[\sqrt{1 + \frac{2W_o}{X_j}} - 1\right]$$

Area of gate charge distribution

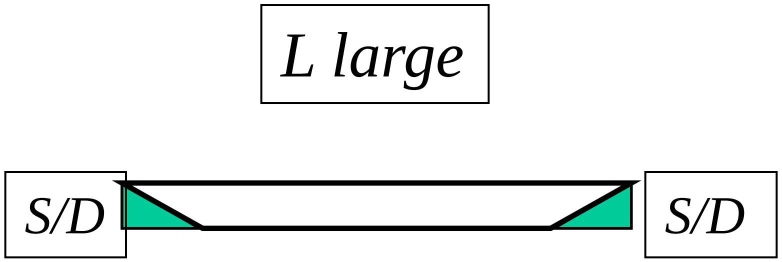
$$= q \cdot N_a \cdot \frac{L + L_1}{2} \cdot W_o \cdot W$$

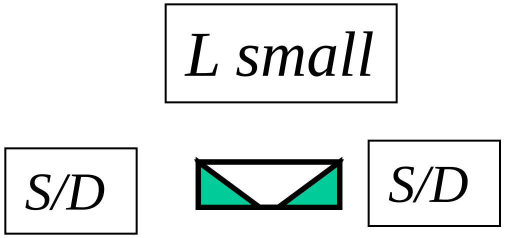
$$\therefore \frac{Q_{actual}}{Q_{ideal}} =$$



$$= 1 - \frac{X_j}{L}\left[\sqrt{1 + \frac{2W_o}{X_j}} - 1\right] \equiv f$$

"Yau Model" for short-channel effect.





To make f $\longrightarrow$ 1

⇨ $X_j \downarrow$

- Implantation at low energy
- Small Dt.
- Minimize channeling and transient enhance diffusion

⇨ $W_o \downarrow$

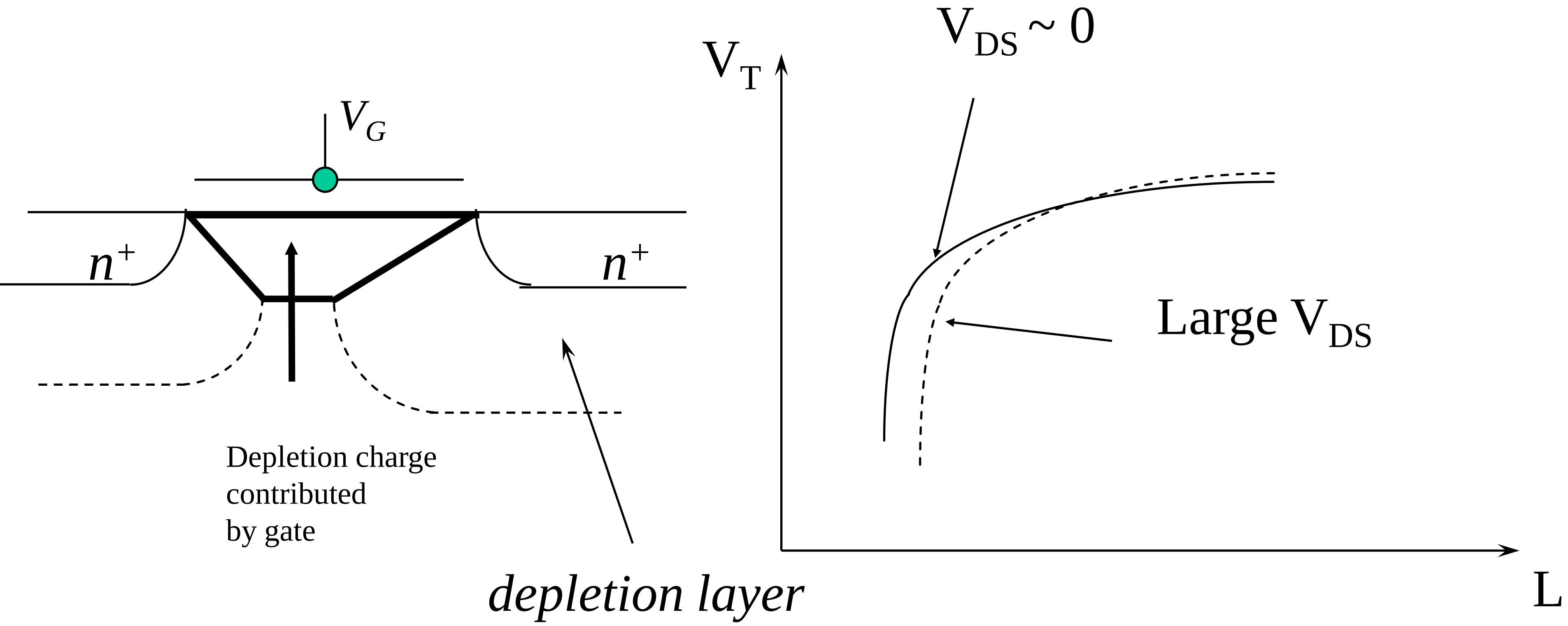
- Increase N_a

Effect of V_{DS} on V_T Lowering

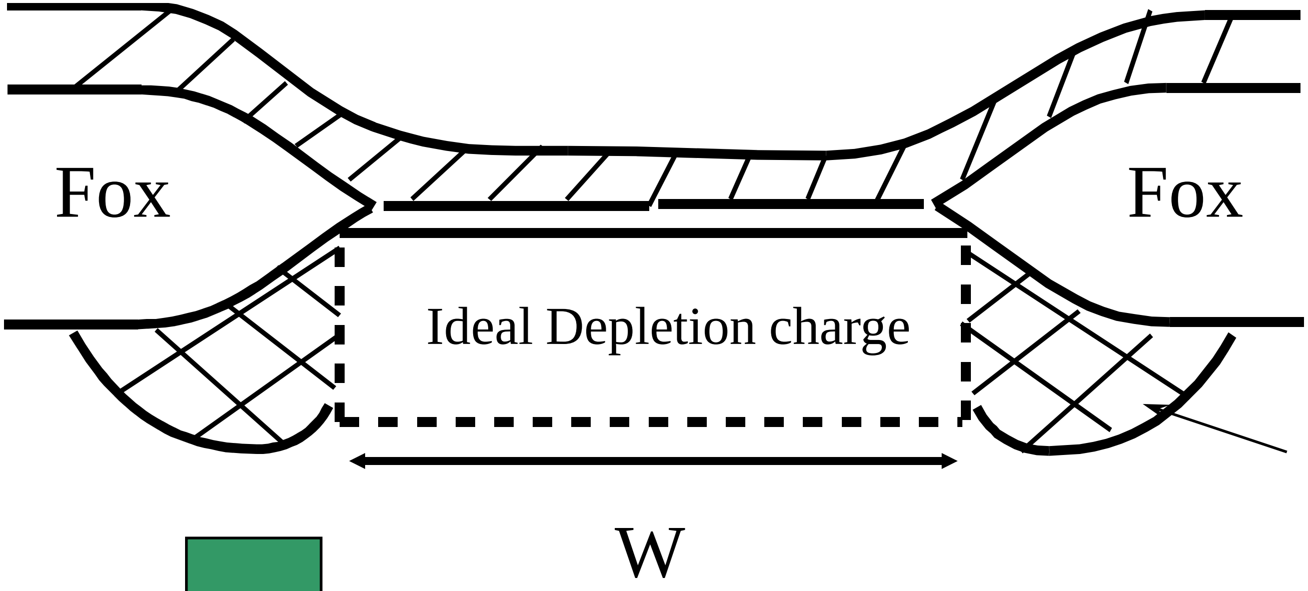
Large V_{DS} ⇒ Larger S/D depletion charge at the drain side

⇒ Smaller depletion region charge contributed by gate

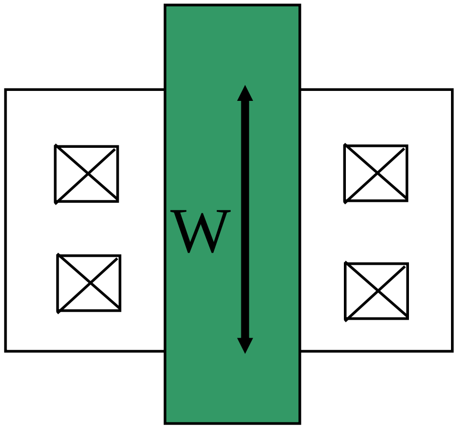
⇒ V_T starts to decrease at larger L



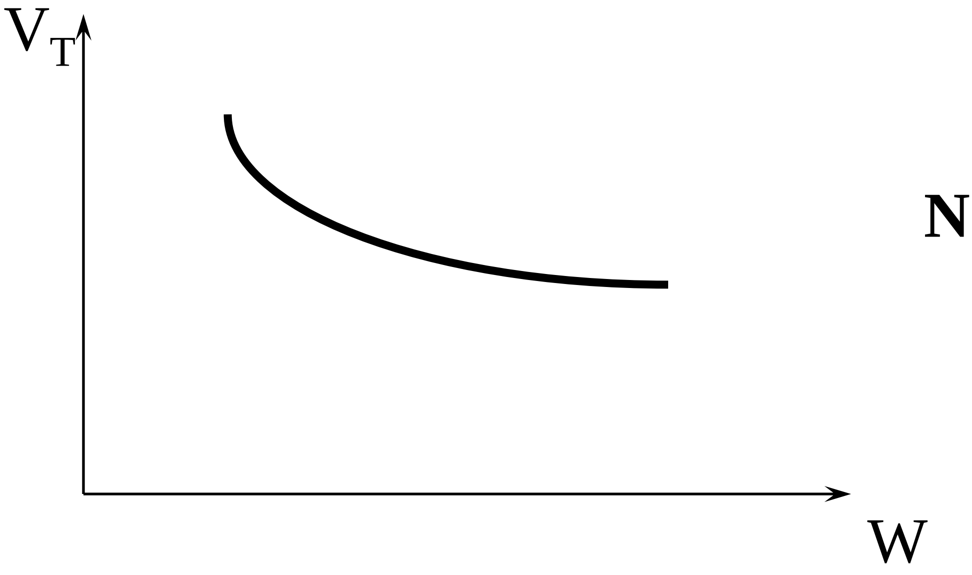
Narrow Width Effect (related to W)



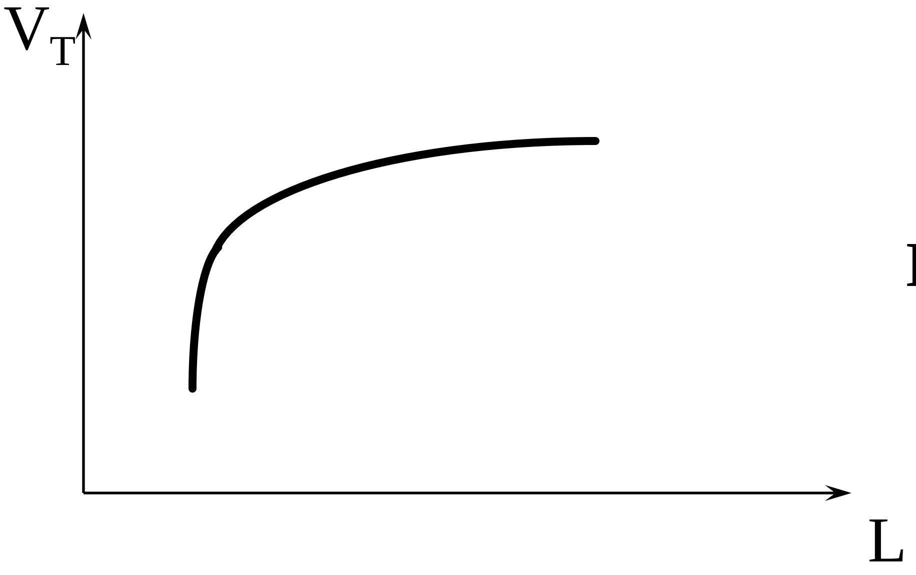
parasitic
charge
which has to
be created
by gate bias



$\therefore V_T$ is larger than ideal analysis.

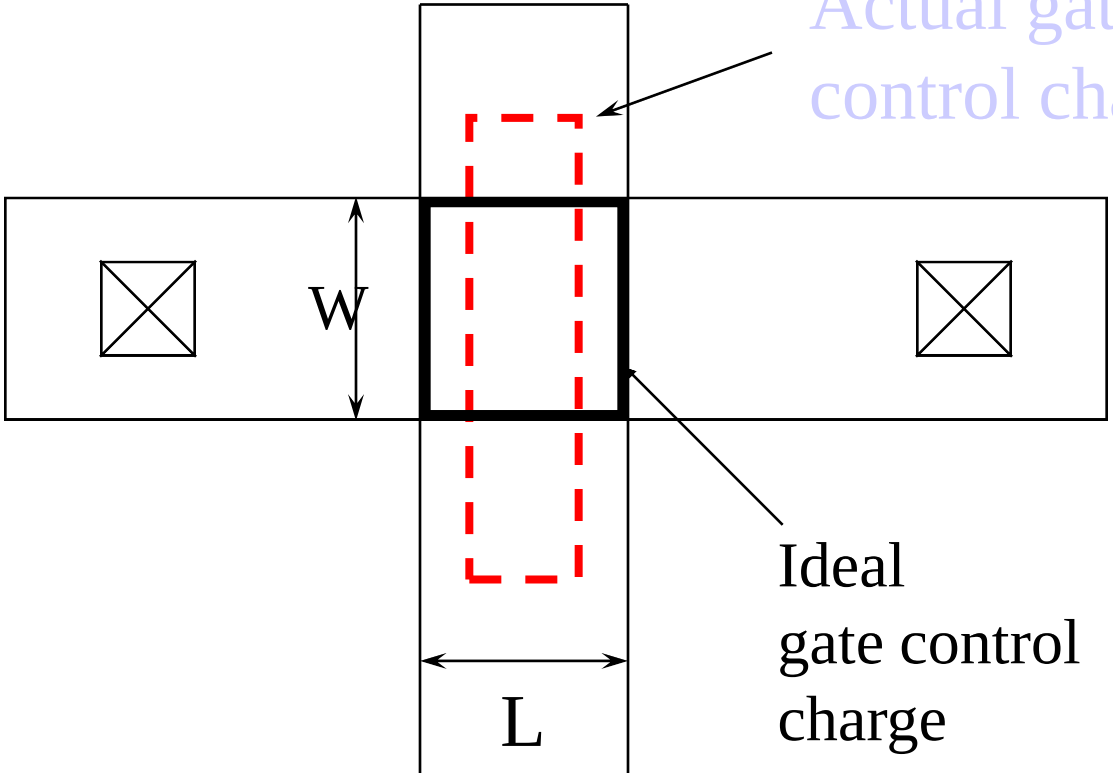


Narrow Width Effect



Narrow Channel Effect

Small Geometry Effects Summary



Actual gate control charge

Ideal
gate control
charge

SUMMARY of MOS Module

- Accumulation, Depletion, and Inversion Modes
- Flat Band Voltage, Threshold Voltage
- Charge Distributions and E-field Distributions
- Voltage drop across Silicon and across oxide
- Channel Bias and Substrate Bias
- Oxide Charge Effects
- Threshold Voltage Tailoring by Implantation
- NMOS and PMOS
- Small Signal Capacitance versus V_G
- MOSFET I-V Characteristics
- V_{Dsat} and I_{Dsat}
- MOSFET Parameters Extraction
- Short Channel and Narrow Channel Effects (qualitative)