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Conference Paper *in* Power Semiconductor Devices and ICs, 1990. ISPSD '90. Proceedings of the 2nd International Symposium on · June 2007

DOI: 10.1109/ISPSD.2007.4294960 · Source: IEEE Xplore

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THE INFLUENCE OF NBL LAYOUT AND LOCOS SPACE ON COMPONENT ESD AND SYSTEM LEVEL ESD FOR HV-LDMOS

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ABSTRACT

This paper investigates the influence of the N-type buried layer (NBL) layout and LOCOS space on the ESD performance and trigger voltage of the lateral DMOS (LDMOS) device. Without adequate LOCOS spacing, LDMOS is vulnerable to ESD damage. If the LOCOS space is sufficiently wide, adding NBL structure can further improve LDMOS ESD performance significantly. This is because NBL can switch the current passage from the surface channel region to the bulk NBL during an ESD zapping, thus, avoiding localized highly damaging ESD current flow in the channel region.

INTRODUCTION

For higher than 30V IC applications, LDMOS with and without NBL structure, as shown in Fig. 1a and 1b, respectively, are one of the most commonly used IC structures for display drivers, power managements and automotive electronics. For display driver ICs, the ESD qualification requires both system level (IEC) [1] and component ESD (HBM and MM) tests. The common failure mechanisms of component ESD tests are oxide break down, junction damage and interconnect burn out. For system level ESD, its major failure mechanisms is in a different way, the latch-up and snapback due to turn-on of the parasitic npn bipolar transistor in LDMOS are dominant mechanisms. For most LDMOS, its snapback voltage is much lower than Vcc. Once the parasitic npn bipolar transistor in a LDMOS has triggered on, it cannot stay extended at the snapback region before causing system level ESD failure. Thus, the trigger voltage of LDMOS cannot be too low since avoiding the undesired npn bipolar turn-on during IEC strike is a necessity, even designed with low on resistance. Although a NBL-isolated LDMOS has better ESD performance for component ESD tests, its system level ESD immunity is, however, worse than non-NBL LDMOS due to the lower trigger voltage. In this paper, a new LDMOS structure with localized-NBL placed only underneath the HVNW of the drain area (Fig. 1c and Fig. 2c) is proposed with compromise on resistance and balanced optimum protection between system level and component ESD performances.

EXPERIMENT

For the analysis of the influence of the NBL layout and LOCOS space on both the system and component level ESD performance and failure mechanism of LDMOS, three different structures, as shown in figure 1 and 2, were fabricated. ESD device parameters analyzed include the trigger voltage, HBM, MM and It2. These three structures are non-NBL LDMOS (Fig. 1a and Fig. 2a), full NBL-isolated LDMOS (Fig. 1b and Fig. 2b), and a new LDMOS structure with localized-NBL (Fig. 1c and Fig. 2c). All LDMOS are designed with 50um wide multi-finger structure. A 0.6um HV 40V/5V CMOS process is used for fabrication. The operation voltages for the drain and gate are 40V and 5V, respectively.

The HBM and MM ESD tests for component ESD evaluation are performed on an ESD simulator that meets both MIL-STD 833C and EIAJ ED-4701 specifications. The direct contact mode and air discharge tests for system level ESD are evaluated using an ESD simulator that meets IEC 61000-4-2 [1] specification.

A 100nsec transmission line pulse (TLP) I [2] is used for high current characterization, including correlation between device trigger voltage (Vt1) and the system level ESD, as well as between device ESD performance and It2. It2 is the maximum device current detected before catastrophic ESD damage. In order to simulate a system level ESD event, the rise time of the TLP is set at 200psec for generating higher displacement current. The failure criterion for HBM, MM, and TLP tests is defined as when the drain leakage current exceeding 1nA under a 45V drain biased after ESD zapping.

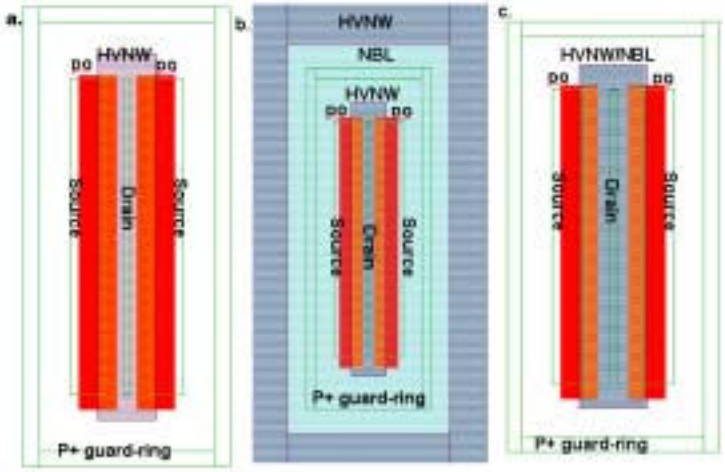

Fig.1 Top views for: (a) a non-NBL LDMOS, (b) Full NBL-isolated LDMOS and, (c) the new LDMOS structure with isolated-BL placed underneath the drain HVNW areas.

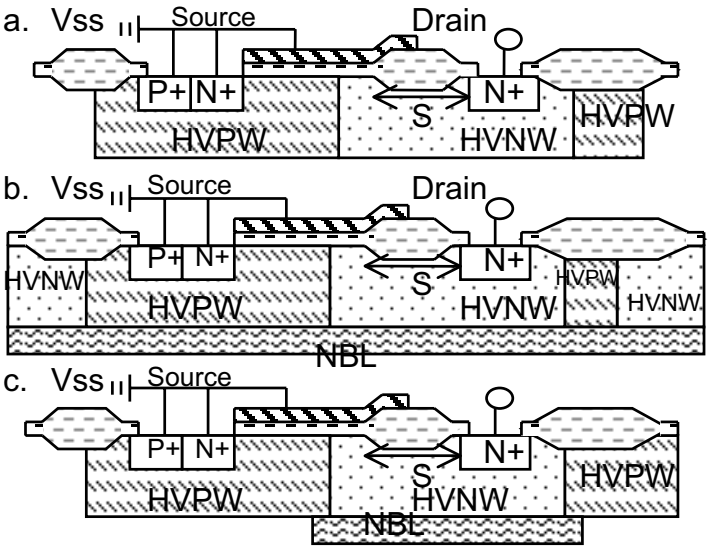

Fig.2 Cross section views for: (a) a non-NBL LDMOS, (b) Full NBL-isolated LDMOS and, (c) the new LDMOS structure with isolated-BL placed underneath the drain HVNW areas.

RESULTS AND DISCUSSION

A. Leakage Characteristics

The gradually increased leakage after ESD zapping beyond the snapback region is one of the main concerns for HV device (Fig. 3). Earlier study [3] has attributed the leakage increase to FOX charge trapping. However, it has not provided electrical data to further elaborate the mechanism of the leakage increase after snapback.

Based on the leakage current characteristics, the high current IV characteristics of the LDMOS under TLP stress can be separated into five distinctive regions: (1) initial stage, (2) pre-snapback stage, (3) snap-back stage, (4) soft breakdown and, (5) hard breakdown, as demonstrated in Fig. 3. To identify root cause and mechanism of the leakage increase after snapback, the leakage of the four terminals (gate, drain, source and bulk) of the LDMOS are measured using DC parameter analyzer HP 4156. As shown in Fig. 4, the measured data indicates that TLP stress does not lead to leakage currents increase at the source and gate even after hard breakdown. However, the drain and bulk current has increased slightly after soft breakdown region and more significantly after hard-breakdown. The complete I_D-V_G curve of the LDMOS is shown in Fig. 5. One may note that drain current has increased with the gate bias for devices after soft-breakdown. This is the well-known "gate induced drain leakage current (GIDL)" effect. The GIDL for ESD protection device increases after ESD zapping has been discussed earlier [4]. During ESD zapping, hot carriers are generated and accelerated in the high field drain junction. Some of the hot carriers can penetrate through gate oxide, resulting in increased interface-state defects in the drain to gate overlaps region. Subsequently, these defects enhance the band-to-defect tunneling assisted current [5], resulting in GIDL increases in the LDMOS after ESD zapping. It implies that the TLP does not lead to the gate oxide damage due to short stress time (~100nsec). This is true even for the thin oxide of 5V operation and the trigger voltage higher than 45V. Nevertheless, it creates a significant amount of interface-states at the overlaps region between gate oxide and drains and resulted in enhanced GIDL current.

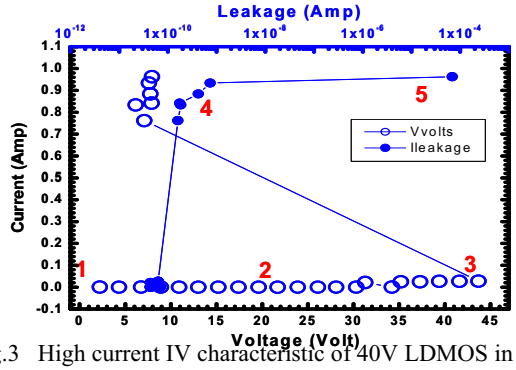

Fig.3 High current IV characteristic of 40V LDMOS in 5 distinctive regions as indicated in Fig. 3

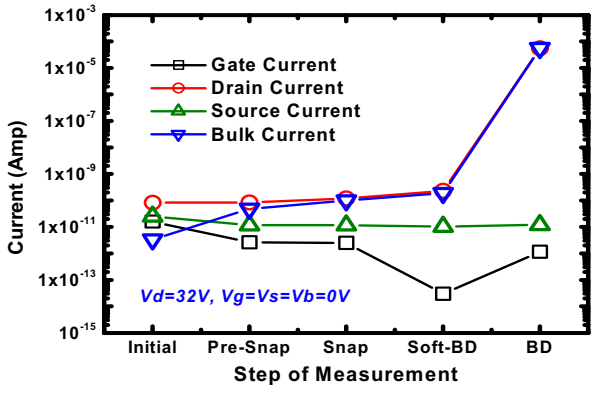

Fig.4 Four terminals DC currents of the LDMOS.

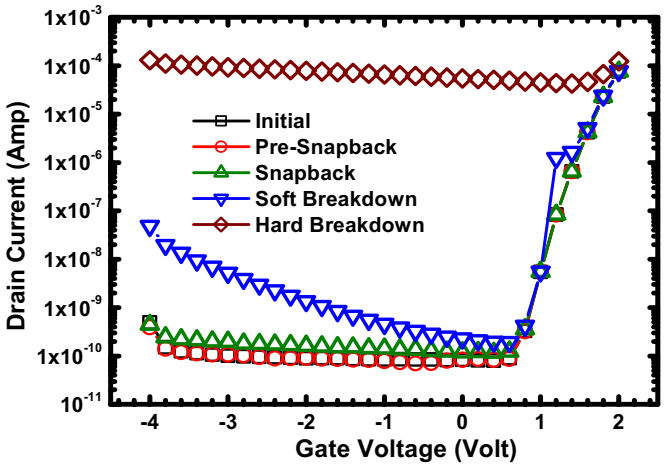

Fig.5 Gate induced drain leakage (GIDL) current was found after soft breakdown region.

B. Effects of LOCOS Space and NBL

High current IV characteristics have been analyzed using both 3 and 5um LOCOS space for all three LDMOS structures, as shown in Fig. 1. With 3um LOSOS space, the leakage currents of all three structures will increase with voltage after the snapback region (Fig. 6). This phenomenon is caused by enhanced GIDL current as a result of hot carriers penetration through gate oxide as discussed earlier. Unlike a non-NBL device, the leakage currents after snapback for LDMOS, either with localized-NBL or full NBL-isolation, has all remained at the same level comparing to before the snapback region. This is true until the stress level is higher than the device It2 when the LOCOS space has been widen to 5um (Fig 7).

To further understand the influence of NBL layout and LOCUS space on LDMOS, TCAD simulations have been performed to assess its current pass. Fig. 8 shows the simulated current distribution contours of a non-NBL LDMOS. Note that the voltage contours of LDMOS are almost the same for 3um and 5um spacing, with most of the crowded current flow confined near the channel region and under the LOCOS edge of the drain side. Because the discharge current is very close to the gate oxide, it is impossible to avoid hot carriers penetration into gate oxide if the device is operated in the snapback region. Thus, a significant amount of interface-state can be generated to cause of GIDL current to increase after zapping. Moreover, because of the current is crowded near the channel region, it leads to local heating from high power dissipated (I×V). One may also clearly notice that the It2 (2.6A) of the non-NBL device is clearly lower than that of the Full NBL-isolated (6.53A) and localized-NBL (5A) as shown in Fig. 7. Fig. 9 shows the simulated current distribution contours of the LDMOS (S=5um) with full NBL-isolated and localized-NBL, respectively. It is noted that most currents flow from drain down to the NBL underneath and then into the source. Practically no current flows through the channel region near the surface. Because the region where hot carriers being generated is far away from the channel, the possibility of hot carriers penetrating into its gate oxide is far less comparing to a non-NBL LDMOS (Fig. 8). Without hot carriers penetrating into gate oxide, there is no high interface-state generation in the overlaps region between the gate oxide and the drain. Thus, the leakage current increase caused by the band-to-defect assisted tunneling current effect is negligible. It is consistent with the high current measured result shown in Fig. 7 that leakage current has remained at a constant level until the stress current is higher than the device It2. Comparing Fig. 8 to Fig. 9, the current density for the device with NBL is much smaller than the non-NBL device since no current crowding at any given region. This can prevent local heating generation in a small region, which can

induce catastrophic damage to the device during ESD zapping, and result in improving in and higher failure threshold.

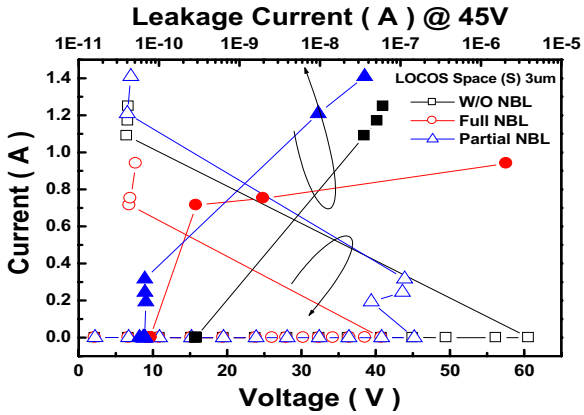

Fig.6 For the three devices in Fig. 1 with S=3um, the leakage current all increases after the snapback region.

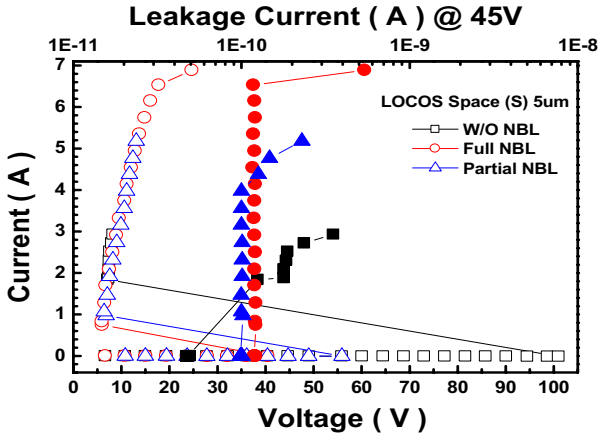

Fig.7 For the three devices with S=5um, the leakage currents of the device with NBL remains at a constant after the snapback region.

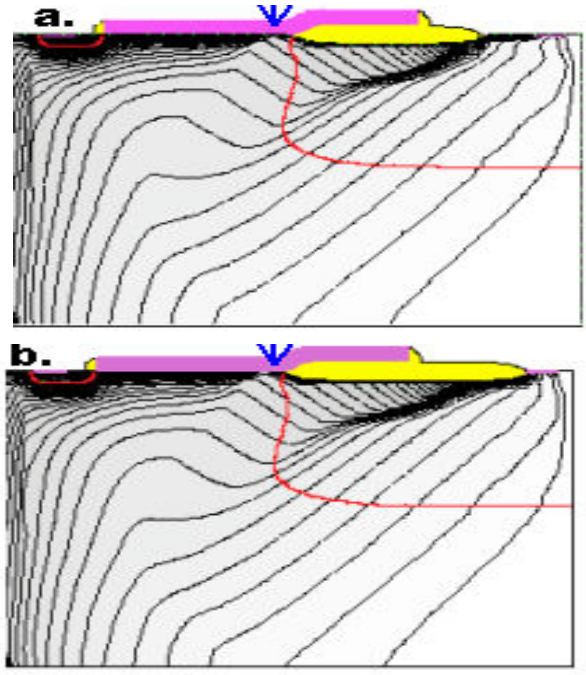

Fig.8 Current flow contours of Non-NBL LDMOS for (a). S=3um and (b) S=5um. Current are crowded in LOCOS edge and channel.

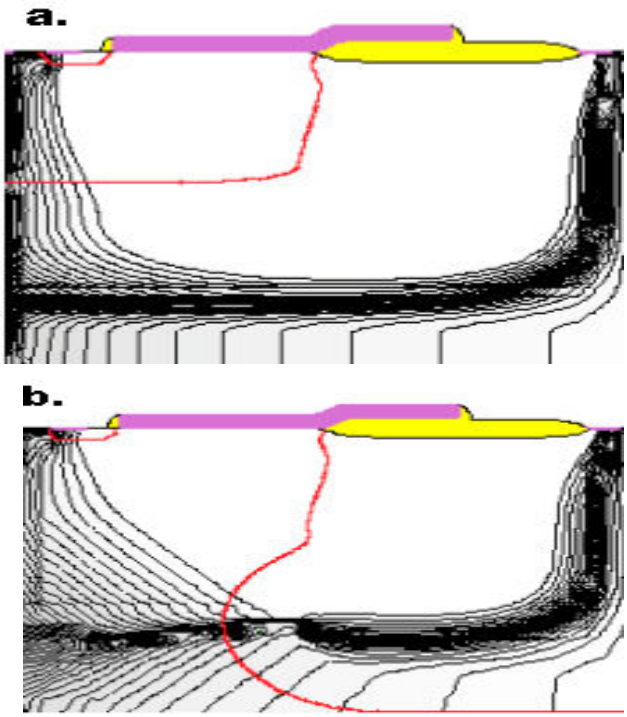

Fig. 9 Current flow contours of LDMOS (S=5um) for (a). Full NBL-isolation, and (b) local NBL. Current flows are directed into NBL from the drain and far away from the LOCOS edge and channel.

C. Effects of LOCOS Space and NBL on Component ESD

Table 1, 2 and 3 summarize the test results of Vt1, It2, HBM and MM failure thresholds of the 3 LDMOS structures. For non-NBL LDMOS shown in table 1, with wider LOCOS space the device Vt1 has increased significantly, along with improved ESD failure threshold to pass 2KV HBM and 200V MM. For LDMOS with localized NBL, its Vt1 has, however, reduced, comparing to Non-NBL, and It2 has increased to more than 2A if the LOCOS space is equal to 4um or wider. Its ESD failure threshold has also improved to 4.5KV and 450V for HBM and MM, respectively. For the LDMOS with full NBL isolation shown in table 3, the increase in LOCOS space has improved both the It2 and ESD failure threshold of the device significantly. It should be noted that the Vt1 cannot increase with the LOCOS space and is only 40V, which is too close to the device normal operation voltage for this technology.

Table 1: Vt1, It2 and ESD results of non-NBL LDMOS

S	Vt1	It2	HBM	MM
3um	60.6V	1.2A	1.0KV	0V
4um	81.6V	1.5A	2.0KV	200V
5um	101V	2.6A	2.0KV	200V

Table 2: Vt1, It2 and ESD results of LDMOS with localized NBL

S	Vt1	It2	HBM	MM
3um	43.9V	1.2A	1.0KV	100V
4um	44.7V	2.1A	4.5KV	450V
5um	55.9V	5.0A	6KV	>800V

Table 3: Vt1, It2 and ESD results of LDMOS with full NBL isolation

S	Vt1	It2	HBM	MM
3um	40.8V	0.8A	1.0KV	100V
4um	40.5V	2.09A	5.0KV	500V
5um	40.5V	6.53A	>8KV	>800V

In summary, our analysis indicates various NBL layout and wider LOCOS space can have significant impacts on Vt1, It2 and ESD performances of LDMOS.

For non-NBL LDMOS, the increase in the LOCOS space can increase the device trigger voltage (Vt1) significantly since the trigger voltage is proportional to drain series resistance [6]. From the simulation result of Fig. 8, the increase in the LOCOS space to 5um cannot change the current distribution. The current is still crowed at the channel region. Although it can improve the device ESD performance to an acceptable level, the device ESD performance is still limited at HBM 2KV and MM200.

Compared the Vt1 results in Table 1-3, adding the NBL to LDMOS will decrease the device Vt1 significantly. This is because adding NBL can increase the device junction capacitance and PW effective resistance since the HVPW is isolated by the NBL and HVNW (Fig. 2b). The increase in the device junction capacitance will increase its displacement current (CdV/dt) during ESD zapping. The well-known criterion to turn on a parasitic npn bipolar is the well potential needs to be higher than 0.7V ($I_{PW} \times R_{PW}$) to forward bias the pn diode between the PW and N+ source. Although the increase in the LOCOS space can increase the drain resistance, it also increases the device junction capacitance. The two effects cancel out each other. So, the Vt1 of the three devices in Table 2 are all clamped at 40.5V. Different from the LDMOS with full NBL, the increase in the LOCOS space for the LDMOS with localized NBL still can increase the device Vt1 since the NBL of the three devices in Table 2 are designed with same area. Thus, the three devices have same displacement current during ESD zapping, but have different drain series resistance, which resulted in different Vt1.

From Table 2-3, the device with smaller LOCOS space (S=3um) still cannot pass HBM 2KV and MM 200V specification. It implies that only adding the NBL still cannot improve the device ESD performance to an acceptable level even it has a NBL since the current cannot be pushed to flow more deeply down through the NBL if the drain series resistance, corresponding to LOCOS space, is not wide enough.

For the non-NBL LDMOS, we can find the damage site (black region) is from drain contact region to HVNW to P-substrate junction and current filaments can be found after ESD zapping, since the current is crowded in the channel region. For the LDMOS with NBL, all the regions between drain and source were damaged by ESD as shown in Fig. 10b. This is consistent with the simulation result that the current flows from the drain through the NBL to source (Fig. 9a). From this result, it implies that the device with NBL has large discharge region compared with the Non-NBL device with its current is crowded at the channel region. So, the device ESD performance can be improved significantly with both NBL and wide LOCOS space.

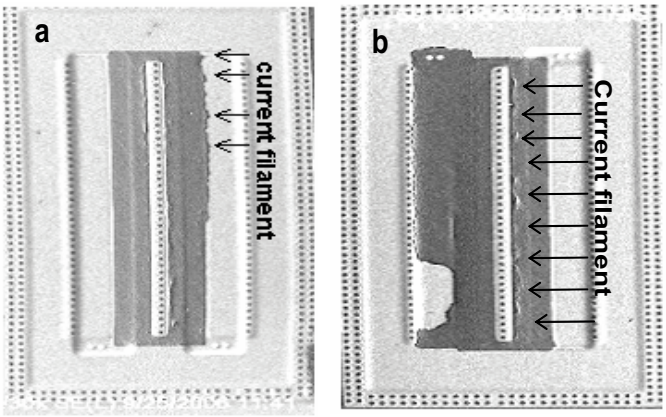

Fig.10 FA results of LDMOS (a) non-NBL, (b) with full NBL isolation. Localized filaments at device without NBL can be observed, but uniform filaments can be observed for device with NBL.

D. System level ESD

Although LDMOS with NBL structure has good component ESD performance, it does not mean its system level ESD can enjoy the same performance. In this experiment, two LDMOS devices with full NBL and partial/localized NBL are designed to evaluate the system level ESD sensitivity of the circuits with two different power domains (VCOM/VEE and VCOM/VSS) in one chip. Fig. 11 shows the FA result of the chip after 8KV direct contact mode ESD-gun zapping. The LDMOS with full NBL-isolation structure was damaged and induced system level ESD failure. However, no damage occurred at the LDMOS with partial or localized NBL. It implies that LDNMOS with partial or localized NBL is a better structure to optimize and balance between the component level and the system level ESD performance.

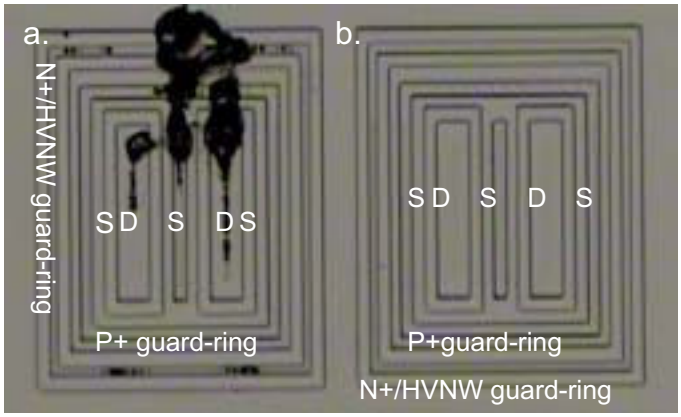

Fig. 11 Top views of: (a) LDMOS ESD device with full NBL structures between VCOM and VEE and (b) LDMOS ESD device with partial or localized NBL between VCOM and VSS. Serious damage on LDMOS with NBL can be observed after ESD gun zapping.

CONCLUSIONS

Our various LDMOS structures and experiment data have demonstrated that without adequate LOCOS spacing, LDMOS is vulnerable to ESD damage. If the LOCOS space is sufficiently wide, adding NBL structure can further improve LDMOS ESD performance significantly. This is because NBL can switch the current passage from the surface channel region to the bulk NBL during an ESD zapping, thus, avoiding localized highly damaging ESD current flow in the channel region.

In our study, the Vt1, It2 and ESD failure threshold of LDMOS with partial or localized NBL, full NBL-isolation and, and non-NBL structures have been thoroughly characterized. The ESD protection mechanisms of the NBL structure are attributed to the increase of both the effective P-well resistance and the junction capacitance that enhances capacitance displacement current and, as a result, a lower parasitic npn bipolar transistor trigger voltage is achieved. Although NBL can significantly improve the component ESD performance of a LDMOS, it also can, at the same time, degrade its system level ESD performance. To optimize between component and system ESD performance for a HV LDMOS, a partial or localized NBL placed underneath the drain HVNW areas is highly recommended.

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