Design Solutions in Foundry Environment

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Design Solutions in Foundry Environment

1. Introduction
2. Custom design flows overview
3. Foundry design access
4. Foundry design solutions:
   - Standard cells
   - IO
   - Technology files and PDK
   - Memory
   - IP initiatives
5. New world of custom IC products
6. Summary

Introduction

Access to foundry leading edge processes has become a common practice for fabless companies and IDMs looking to leverage their capacity.

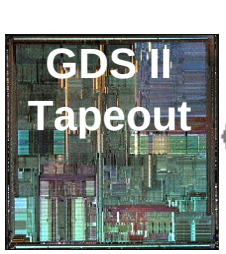
Foundries do not offer a process solution alone, but the complete product, consisting of:

1. **Process with multiple variants.**
2. **Design access.**
3. **Turn key services (i.e. test, assembly, drop ship, etc.)**

The use of design solutions through foundries is increasing:

- **25% of 0.25 um tapeouts at the leading foundry use provided libraries.**
- **60% of 0.18 um tapeouts at the leading foundry use provided libraries.**
- **85% of 0.13 um tapeouts at the leading foundry use provided libraries.**

Foundry Design Access Model



Customer

Physical Implementation
(Backend Design)

Functional Implementation
(Frontend Design)

Product Conceptualization
(Architecture Design)

Partner

Mask Tooling

Foundry

Foundry Process Specs
- DR
- ET/EP
- SPICE Model
- IA Model

Design Kits & Verification Tools Support
- PDK
- LVS
- DRC
- RC Extraction

Partner

STD Libraries
- Std Cell
- I/O Pads
- Memory Compiler

Analog IPs
- Non-differentiable IPs : PLL, ADC, DAC, USB, etc
- VCX Program

Verified in Silicon

Foundry Technology

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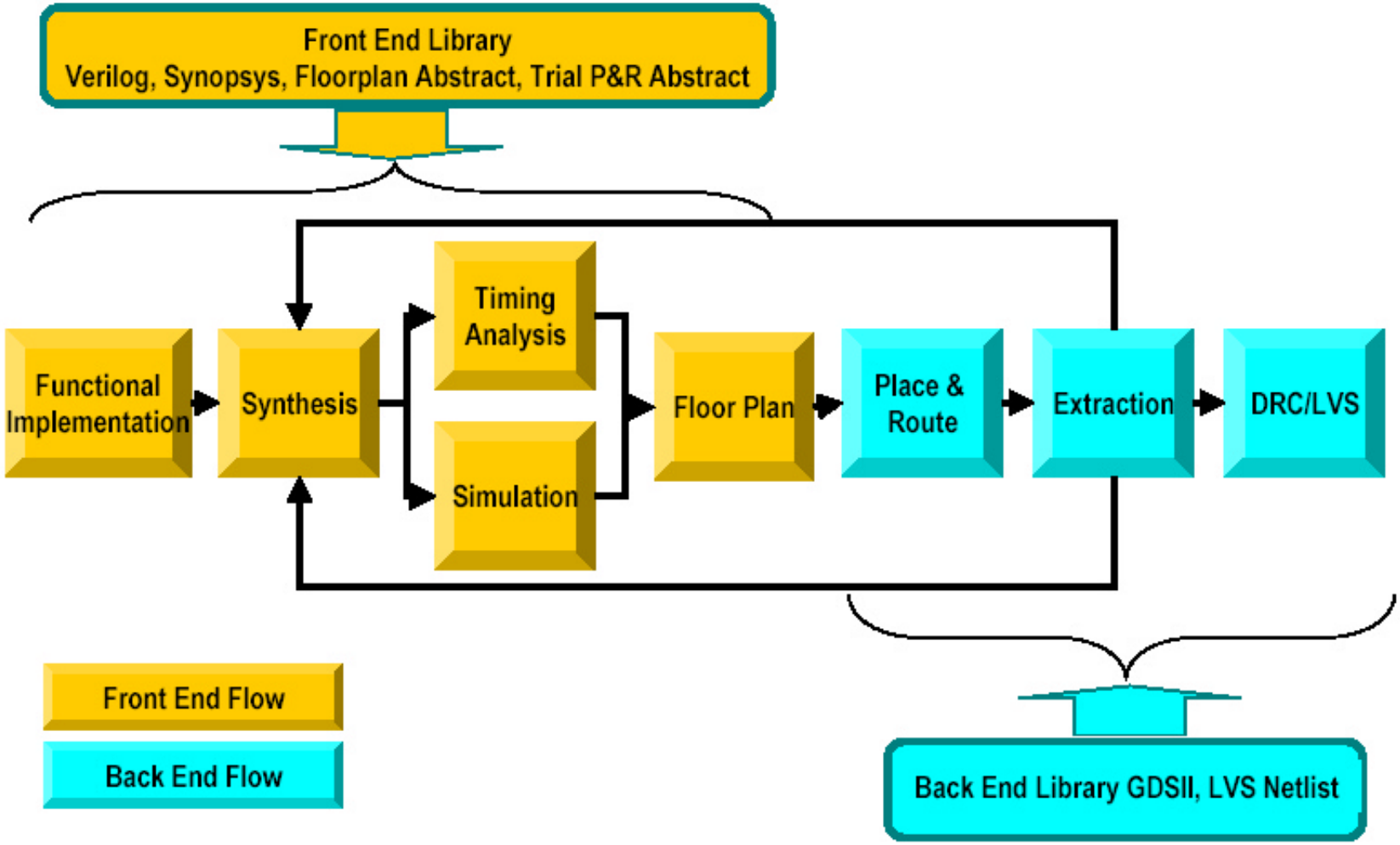
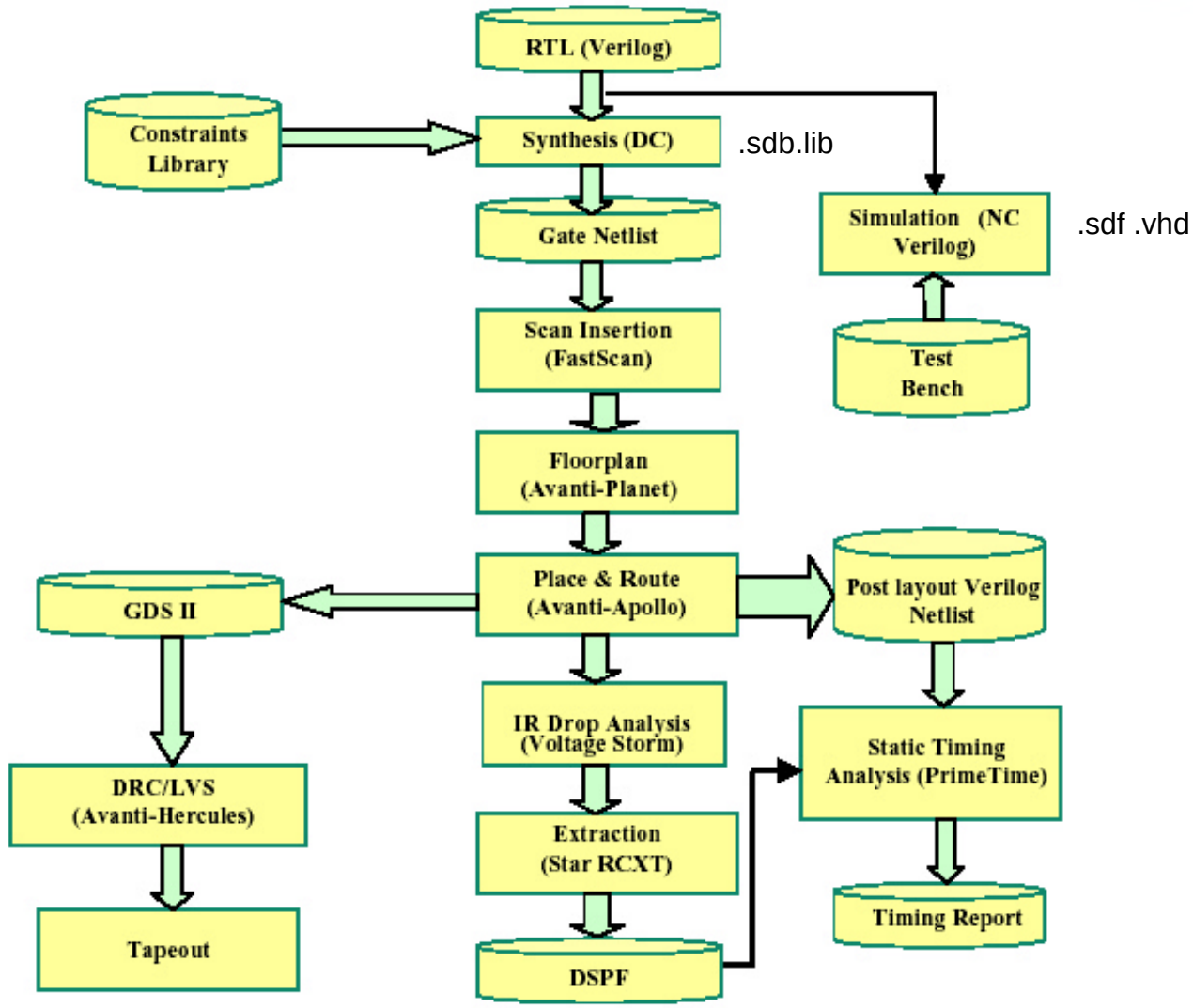
Generic Custom Digital Design Flow



Example of Standard Cell Design Flow



New Challenges in IC Design

Modern challenges in advanced semiconductor product designs can be divided into three broad areas:

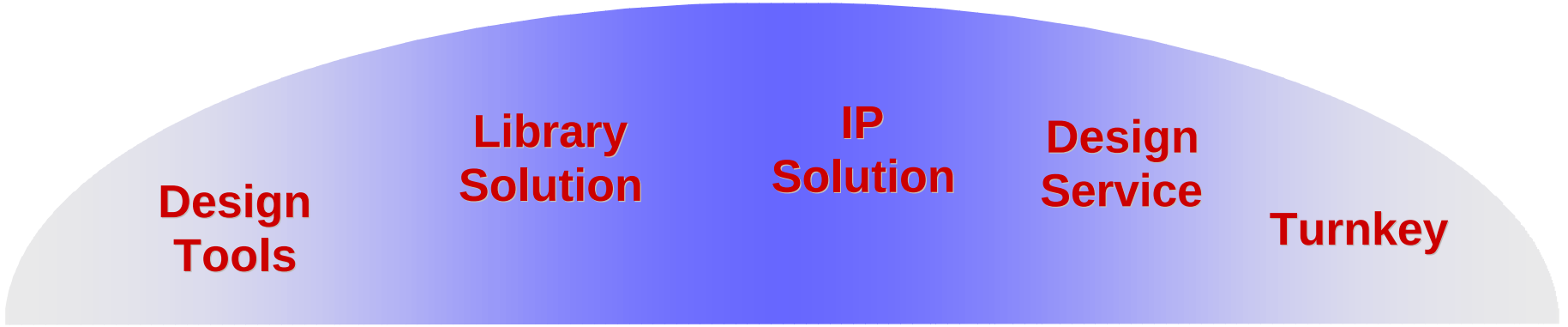
1. **Challenges in traditional design hierarchy (such as logic design, layout design) due to increased product functionality and SoC integration.**
   => New EDA tools, technique, and methodology. (This is expected to lead to further consolidation among EDA and design IP vendors).

2. **Challenges related to shrinking technology: new materials, exponentially increasing leakages currents, increasingly complex interconnect structures, design related yield loss.**
   => The merger of design and manufacturing process development
   => Further development of Design For Yield (DFY).

3. **Challenges related to IP acquisition and management; mass production know-how.**
   => New emerging IP industry.
   => Technology research and manufacturing "constellations" (between major foundries and IDMs)

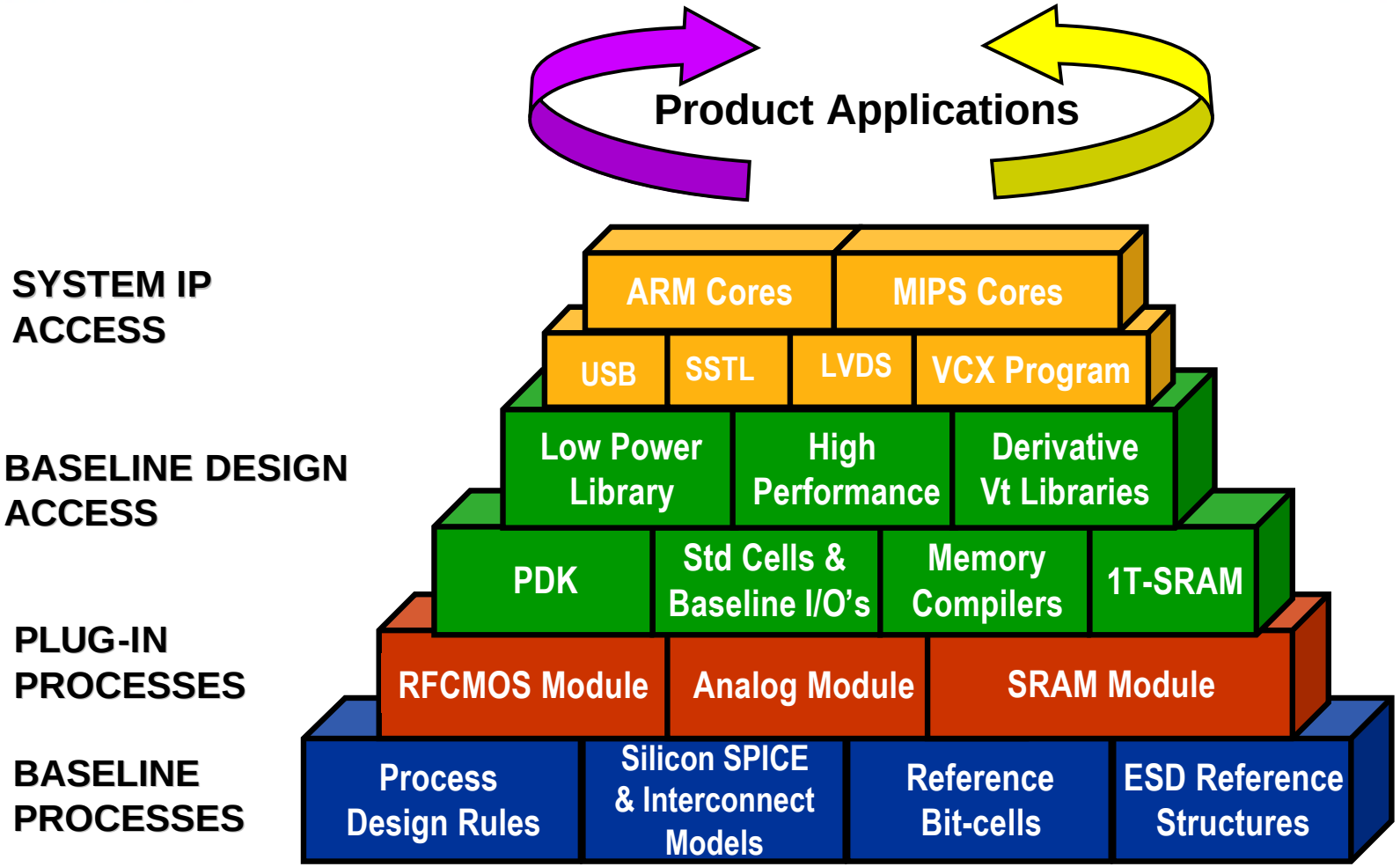
Access to Complete Design Solutions

Various design solutions are available through foundries



cadence
SYNOPSYS
simplex
Mentor Graphics
SYNOPSYS
Artisan COMPONENTS
cadence
VIRAGE LOGIC
UNIVE
ARM
MoSys
FUJITSU
MIPS TECHNOLOGIES INC
VIRTUAL COMPONENT EXCHANGE VCX
eSilicon
Think IC DESIGN
GDA Technologies
FLEXTRONICS

Design Solutions: Foundry Pyramid



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Design Access Considerations

Due to complexity of the problem and long term design engagements, serious considerations have to be given to access design solutions from a foundry.

Next we will examine some of the major aspects of design IP access which needs to be analyzed and reviewed prior to foundry engagement.

Design Access Considerations: IP Offering

1. Key points to consider in EDA IP offerings from foundry:

- Foundry's EDA partner selection
- IP suitability for current and future design projects
- Schedule of IP availability
- Cost model of EDA IP access (cost of acquisition, NRE and royalty structure)
- Portability of library and IP solution (open model vs. captive model)
- IP deliverables to customer
- IP selection: libraries for process variants, special digital IP blocks (i.e. IOs, ARM, etc.), analog IP.

Design Access Considerations: IP verification

2. EDA IP verification and characterization methodology:

- **Foundry methodology to validate EDA libraries, compilers, etc.**
  - **resources: expertise and tools**
  - **silicon verified vs silicon hardened**
- **Process/SPICE changes:**
  - **approval of changes in regards to EDA IP**
  - **EDA IP characterization: time, schedule (before the changes or after)**
  - **foundry's flexibility for existing and on-going designs**

Design Access Considerations: Design Support

3. Design support from foundry:

- Local expertise in different IP
- Foundry resources:
  - engineers vs project managers
  - design tools used at foundry
- Foundry support model
- Design services

Design Access Considerations: Final

4. IP Tapeout support:

- **Procedures for "black box" models (i.e. ARM)**
- **IP tagging for royalty payments (i.e. specialized vs industry standard VSIA)**

Conclusion:

Selection of design IP from foundry makes a significant difference in the long term success of foundry engagement. The key elements discussed above need to be considered.

Foundry Design Solutions

- Libraries
- Technology Files and PDK
- Memory
- IP Initiatives

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Foundry EDA Library Components

EDA library design solutions provided by major foundries usually consist of:

1. **Standard Cell Libraries;**
2. **IO libraries;**
3. **Memory compilers and embedded special memories such as embedded 1TSRAM, E^2PROM, OTPROM, etc.**

Each part of library solution has its unique challenges and requires special considerations.

Standard Cell Libraries: Architecture

- Cell height optimized for each process technology, driven by
  - –Back-end process
  - –Transistor performance (i.e. I_{Dsat}, I_{OFF}, V_t, G_m, etc.)
- Cell height is consistent across a library, however a library can have double height cells.
- Cell dimensions are reported in terms of routing grids or tracks

  i.e. two-input NAND gate is typically 3 tracks wide and 8-10 tracks tall depending on the technology
- Cells are designed to share power & ground rails - “Flip and Abut”
- Input/Output pins can be staggered to improve router effectiveness.
- Cells designed to be “Tiled” together.

Typical Third Party Standard Cell Library Design Kit

Standard cell libraries from major IP providers typically include:

- **Front End Views**
  - Behavioral models
  - Simulation timing models:
  - Cadence NC-Verilog, NC-VHDL,Verilog-XL
  - Synopsys synthesis models
  - Design Compiler, Module Compiler, Physical Compiler,
  - Power Compiler
  - Synopsys PrimeTime Static Timing Models
  - Floorplan abstract
- **Back End Views**
  - Abstract Files for Place & Route Tools
  - CDL Netlists for LVS Verification
  - Physical (Layout) Files for Streaming Out GDSII Database
- **Documentation**: data-books, application notes

IO Library: Important Parameters

Key parameters of IO libraries:

- **Pad Structure**:
  – In-line pads for core limited designs: wide and short
  – Staggered pads for pad limited designs: narrow and tall
- **IO cell height**
- **Pad pitch and pad opening**
  – must be designed to meet particular assembly capabilities
- **Separate I/O power rail**
  – Accommodate I/O drive voltage requirement
  – Isolate “Noisy” I/O power from core power
- **Simultaneous Switching Outputs** - SSO
  – Guideline for the number of power pin pair requirements

Open Model Library Access: Chartered Semiconductor

Open Model Library Access

Partners	0.35µm	0.25µm	0.18µm	0.13µm
Synopsys	Standard Cell Library IO Pad Library Memory Compilers	Standard Cell Library IO Pad Library Memory Compilers	Standard Cell Library IO Pad Library Memory Compilers	Standard Cell Library IO Pad Library Memory Compilers
Artisan	N.A	Standard Cell Library IO Pad Library	Standard Cell Library IO Pad Library Memory Compilers	Standard Cell Library IO Pad Library Memory Compilers
Virage	Memory Compilers (SPSRAM, 2P Regfile)	Memory Compilers (SPSRAM, DPSRAM, 1P & 2P Regfile)	Memory Compilers (SPSRAM, DPSRAM, 2P Regfile, ROM)	Memory Compilers (SPSRAM, DPSRAM, 1P & 2P Regfile, ROM)

Source: Chartered Semiconductor Manufacturing web site (http://www.charteredsemi.com/design/library_support.asp)

0.13µm Library Offerings

0.13µm Library Offerings

Partner	Synopsis (Visa)			Artisan		Virage Logic
Components	Standard Cell Library			SAGE-X Standard Cell Library		Sync Single Port SRAM Compiler
	In-line I/O Library 3.3/2.5V			In-Line I/O Library 3.3V		Sync Dual Port SRAM Compiler
	Staggered I/O Library 3.3/2.5V			Staggered I/O Library 3.3V		2 Port Register File Compiler
	Sync Single Port SRAM Compiler			Sync Single Port SRAM Compiler		1 Port Register File Compiler
	Sync Dual Port SRAM Compiler			Sync Dual Port SRAM Compiler		Sync ROM Compiler
	Async 2 Port SRAM Compiler			2 Port Register File Compiler		
	Sync ROM Compiler			Sync ROM Compiler		
Design Kits	Now	Now	Q203	Now	Now	Now
Si-Proven	Q203	Q403	Q403	Q203	Q403	Now

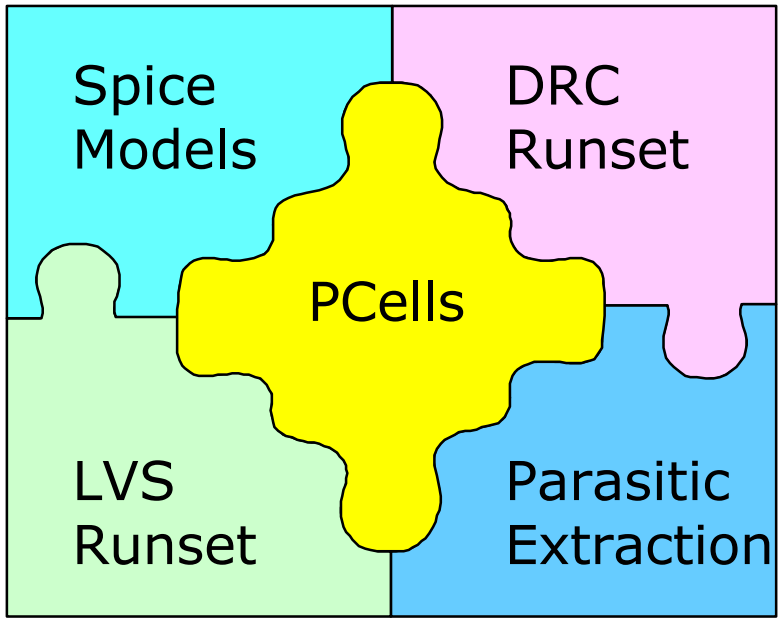
Source: Chartered Semiconductor Manufacturing web site (http://www.charteredsemi.com/design/library_support.asp)

Design Solutions

- Libraries
- Technology Files and PDK
- Memory
- IP Initiatives

What is a Foundry Process Design Kit (PDK)?

- A PDK is a complete set of building blocks, generated from foundry's technology files, that enables customers to create a custom IC design . PDK is most commonly implemented in Cadence design environment format. It must be aligned and verified with foundry's process technology.



- PDK is the equivalent of a Standard Cell Library for digital design, providing an 'off the shelf', easy to install design environment tuned to a specific process technology.

Foundry-supported EDA Tech Files, Models & Tools

EDA support form foundries covers all major aspect of the design flow and all major EDA tools.

Source: TSMC web site (http://www.tsmc.com/download/enliterature/eda_bro_2003.pdf)

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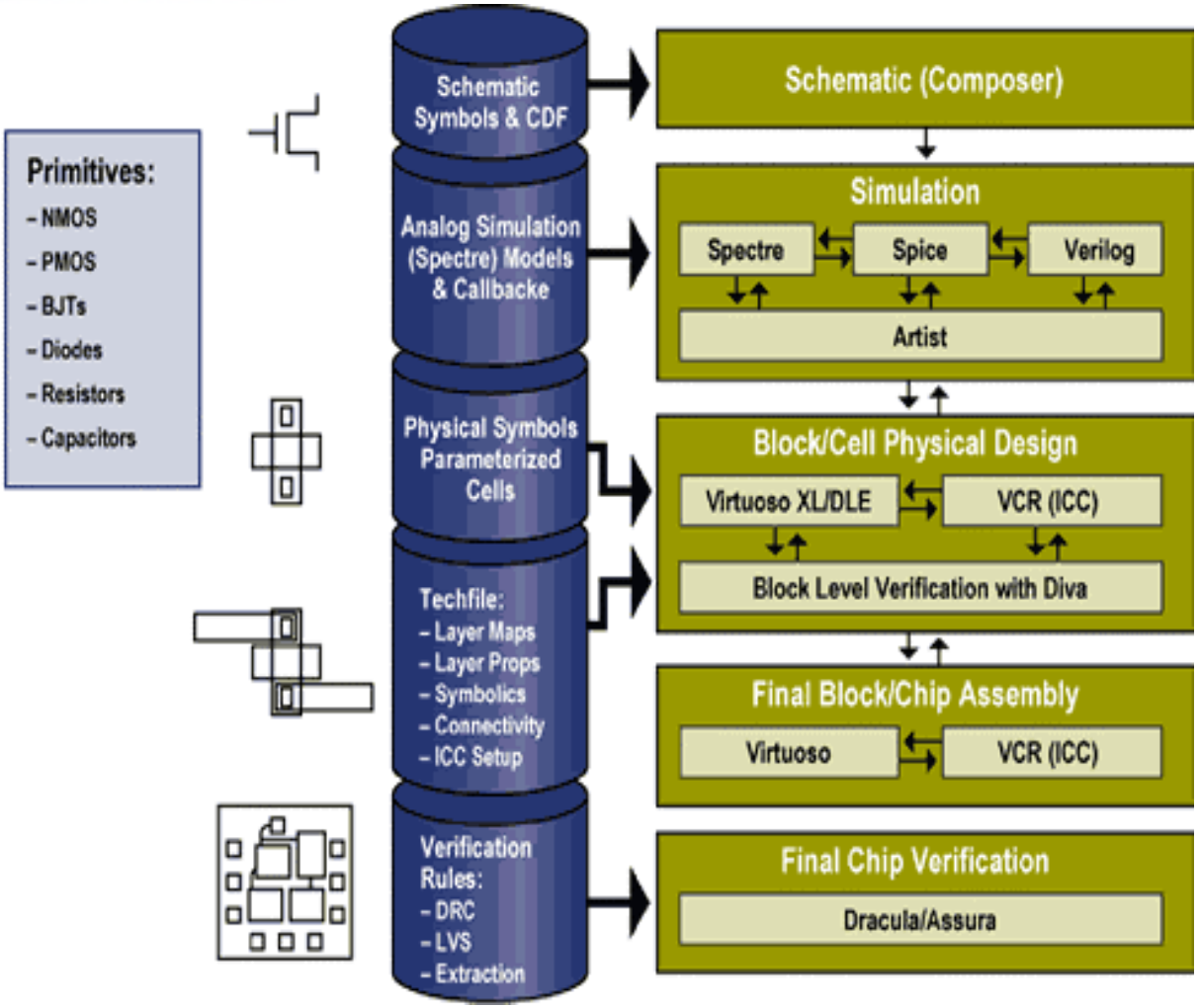
PDK Example: Cadence / Chartered PDK



Consistent with foundry technologies capabilities

Customers are able to design, simulate, layout, extract, verify & tape-out from transistor level upwards.

Source: Chartered Semiconductor Manufacturing web site (http://www.charteredsemi.com/design/pdks.asp)

Foundry PDK

Foundry provided PDKs have to be used with caution and full understanding of their advantages, limitations and tradeoffs, as compared to in-house developed PDK.

EETIMES
THE INDUSTRY SOURCE FOR ENGINEERS & TECHNICAL MANAGERS WORLDWIDE

Panelists cite shortcomings of process design kits

By Ron Wilson, EE Times, Mar 23, 2004 (http://www.eedesign.com/showArticle.jhtml?articleID=18401470)

Key points:

- **Change of process may not be reflected in PDK.**
- **With the growing complexity and rate of change in processes, IP vendors will be unable to keep their IP current with the process... "It's very likely that the IP you use will have been developed with a different PDK from the one you are using. That will be trouble." - Dan Hillman, VP Virtual Silicon**
- **PDK revision control.**

Design Solutions

- Libraries
- Technology Files and PDK
- **Memory**
- IP Initiatives

EDA Library: Memories

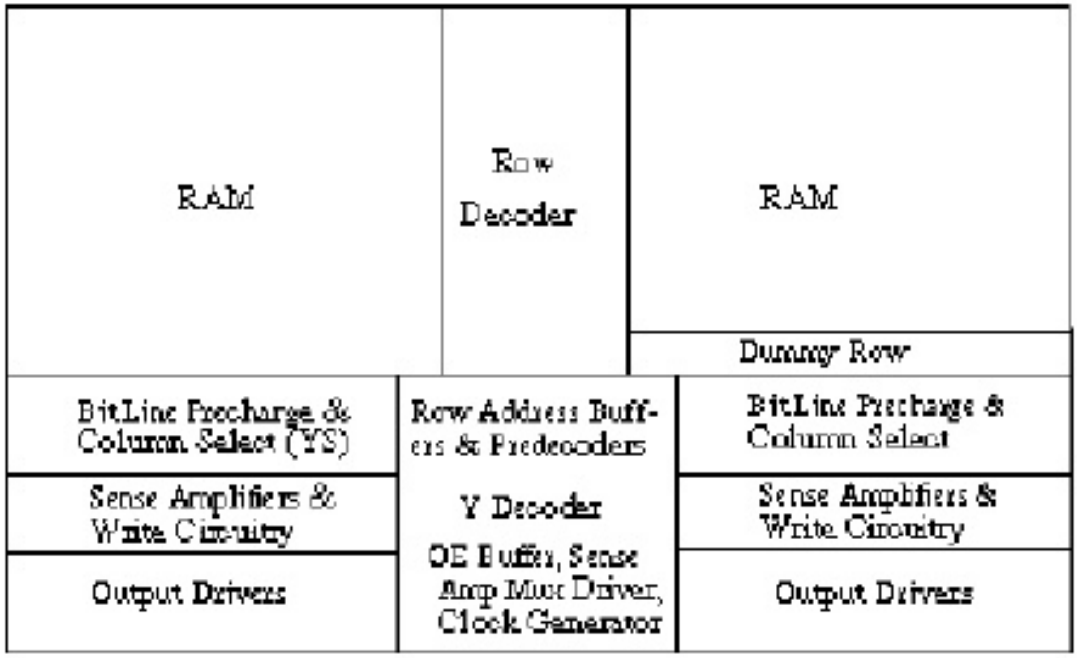
Memory Compilers -- Software Packages to build User Defined Memory Blocks

Type of memory compilers typically offered as part of foundry EDA library:

- **Single Port Sync SRAM**
  - 6 Transistor bit cell architecture
  - Read/Write from a single port
- **Dual Port Sync SRAM**
  - 8 Transistor bit cell architecture
  - Two fully independent read/write ports, each with its own clock
- **2 Port SRAM**
  - 8 Transistor Bit Cell Architecture Most Common
  - One port used for read, one port used for write
- **ROM**
  - Diffusion (smaller)
  - Via ROM (more flexible)
- **Register File –** alternative to embedded SRAM
  - Single port and Dual port

Compiled SRAM: Example

Typical Compiled embedded SRAM Architecture



A lot of memory "overhead" is part of generated SRAM.
Compiled register file may be a good alternative to small SRAM.

Design Solutions

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- Technology Files and PDK
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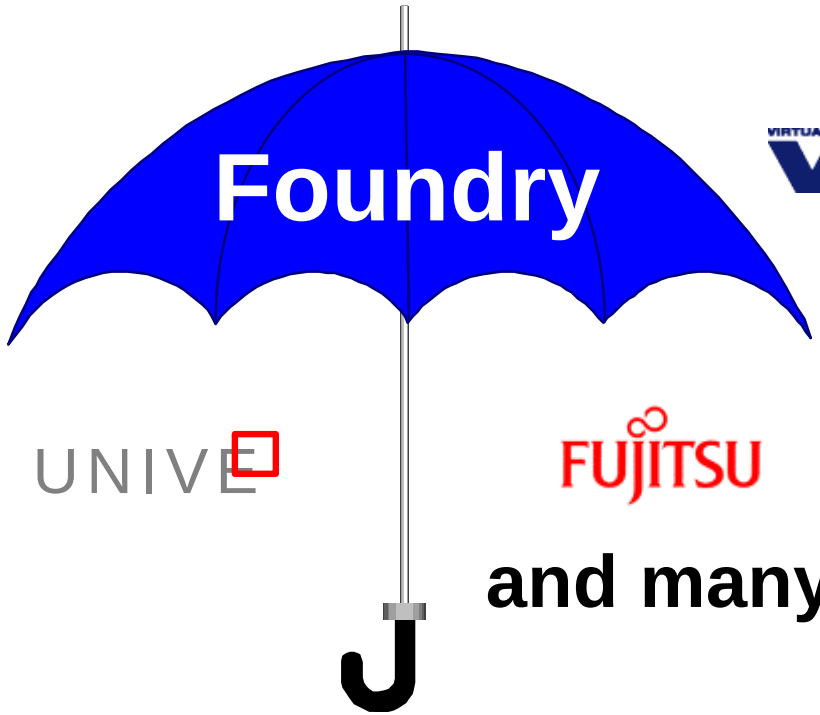
Available Foundry IP Initiatives



ARM

MIPS TECHNOLOGIES INC

MoSys

VIRTUAL COMPONENT EXCHANGE VCX™

UNIVE

FUJITSU

and many many others …

Benefits for Customers

Foundry supported IP alliances program allows:

- **Compare and select from various third-party IP solutions**
- **Silicon hardened and proven at various foundries**
- **IP is listed against industry standard specifications, e.g. VSIA (Virtual Socket Integration Assoc.)**
- **IP provider states level of validation and specific silicon processes in which it has been hardened**
- **Customers have access to more silicon hardened IP, reducing risk and exposure**
- **IP flexibility and ownership are understood prior to engagement**

New Economical Realities for Custom IC

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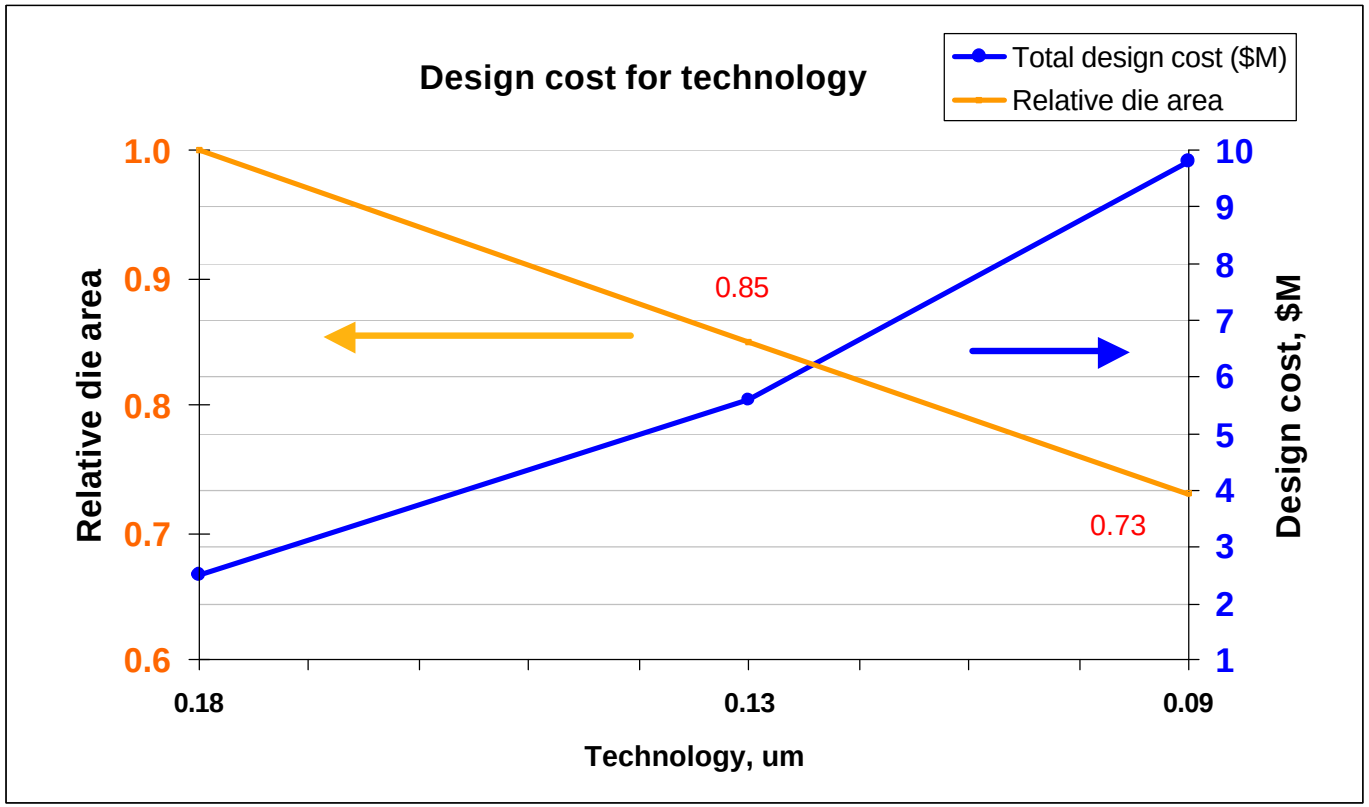
New World of Custom IC Product Design

Cost of new ASIC designs increase with every technology generation:



Average design cost: EDA/COT tools, design engineering, mask set, prototyping, test.

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New World of Custom IC Product Design

The business dynamics of custom IC products changed:

ASIC [1] LOW COST

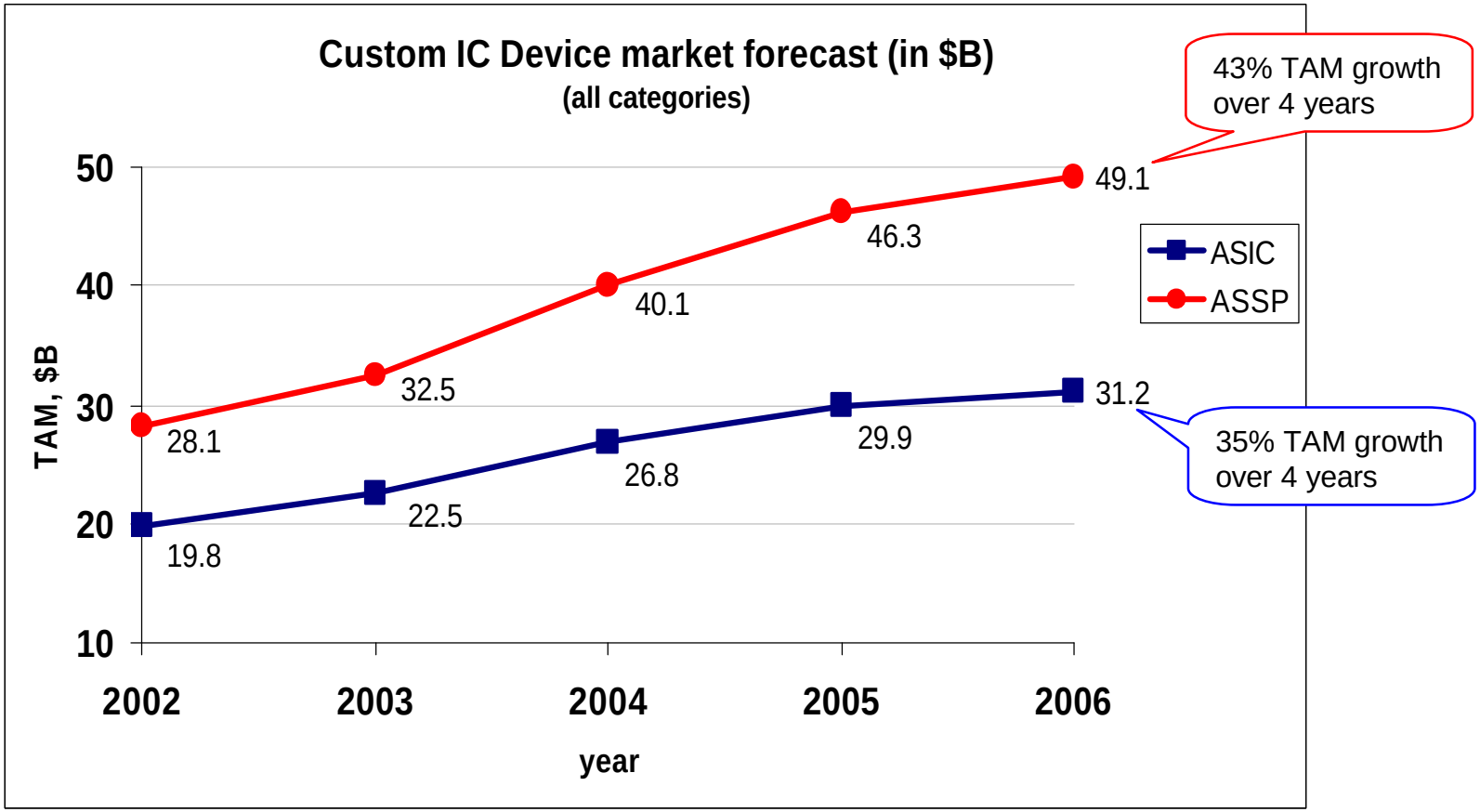
Market response:

- **High volume ASIC applications (i.e. consumer electronics)**
- **High performance ASIC applications (at premium cost)**
- **ASSP**
- **New technologies such as FPGA core with standard cell ASIC:**

  for example, from IBM/Xilinx, reconfigurable ASIC core from LSI, etc.

ASIC vs ASSP

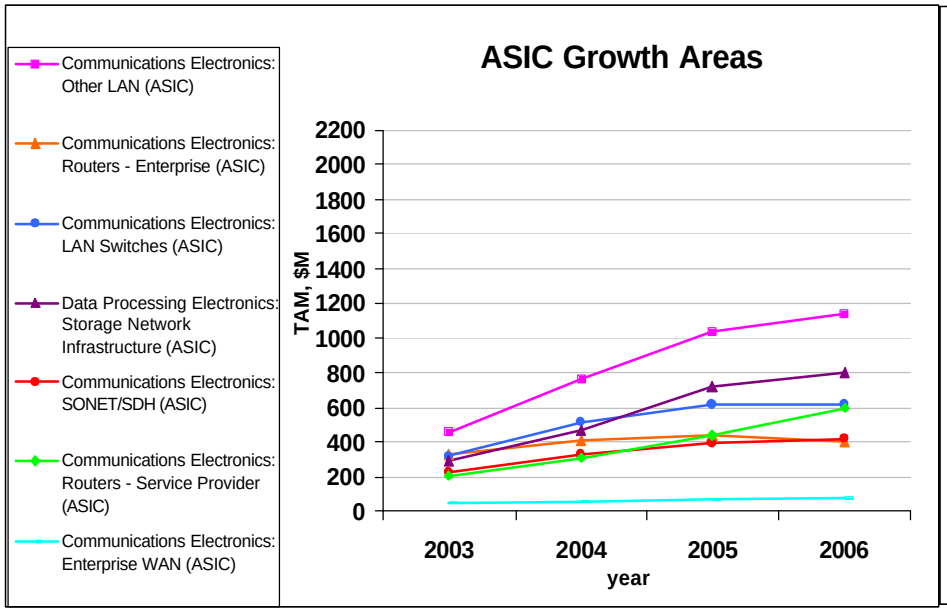
The gap between ASIC and ASSP is projected to widen

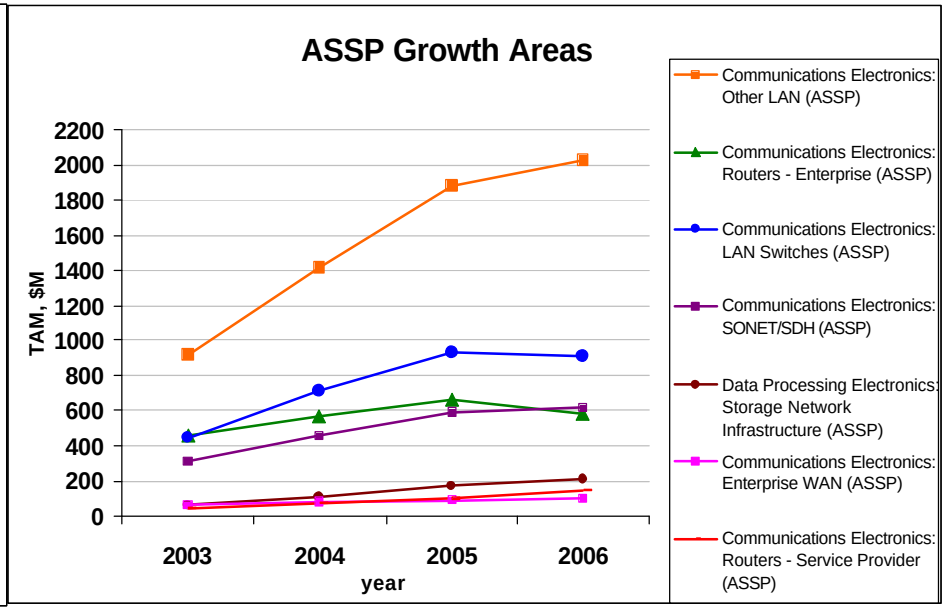


Source: Gartner Research Semiconductor Forecast, 2003

ASIC and ASSP Growth Areas

Growth areas for ASIC and ASSP in communication sector





ASIC top 3 growth areas:
- **LAN (switches and access)**
- **Enterprise routers**
- **Storage network infrastructure**

TAM = $1.4 billion in 2003
TAM = $2.8 billion in 2005

ASSP top 3 growth areas:
- **LAN (switches and access)**
- **Enterprise routers**
- **SONET/SDH**

TAM = $2.1 billion in 2003
TAM = $4.2 billion in 2005

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Source: Gartner Research Semiconductor Forecast, 2002

Summary

- **Foundries offer complete design access in addition to process, tech files, and libraries**
- **Foundries are becoming active participants in design process.**
- **Foundries EDA IP engagements need to be carefully evaluated against current and future design needs**
- **Design IP access model needs to be taken into considerations for a long term foundry engagement.**
- **Cost of custom designs is increasing rapidly for more advanced technologies.**
  First time TO success is crucial for success => extensive and accurate simulation, virtual prototyping, design for yield.