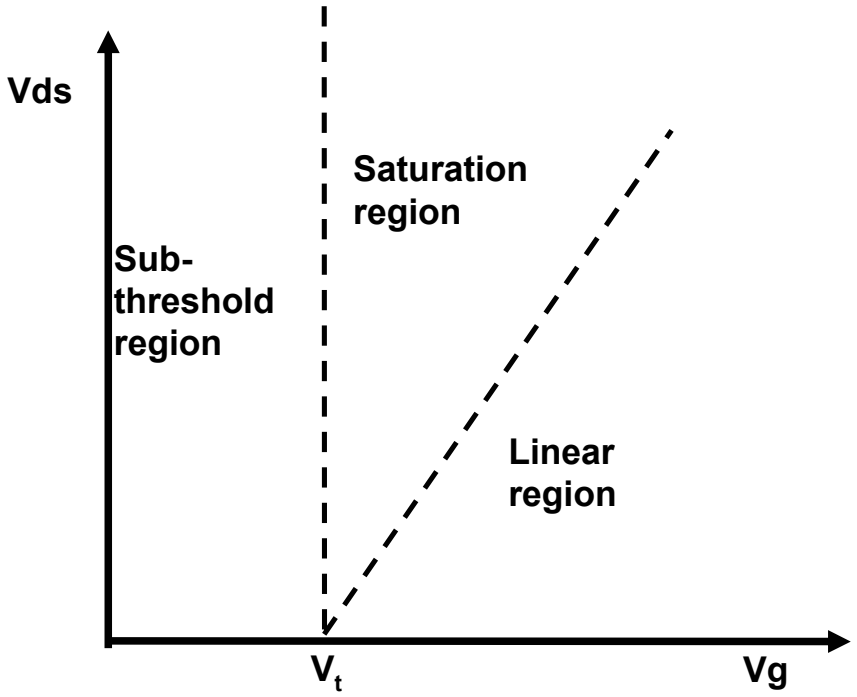
Sub-Threshold Region Behavior of Long Channel MOSFET

Sub-threshold Region

- So far, we have discussed the MOSFET behavior in linear region and saturation region
- Sub-threshold region is refer to region where Vt is less than Vt
- Sub-threshold region reflects how fast the MOSFET can switch

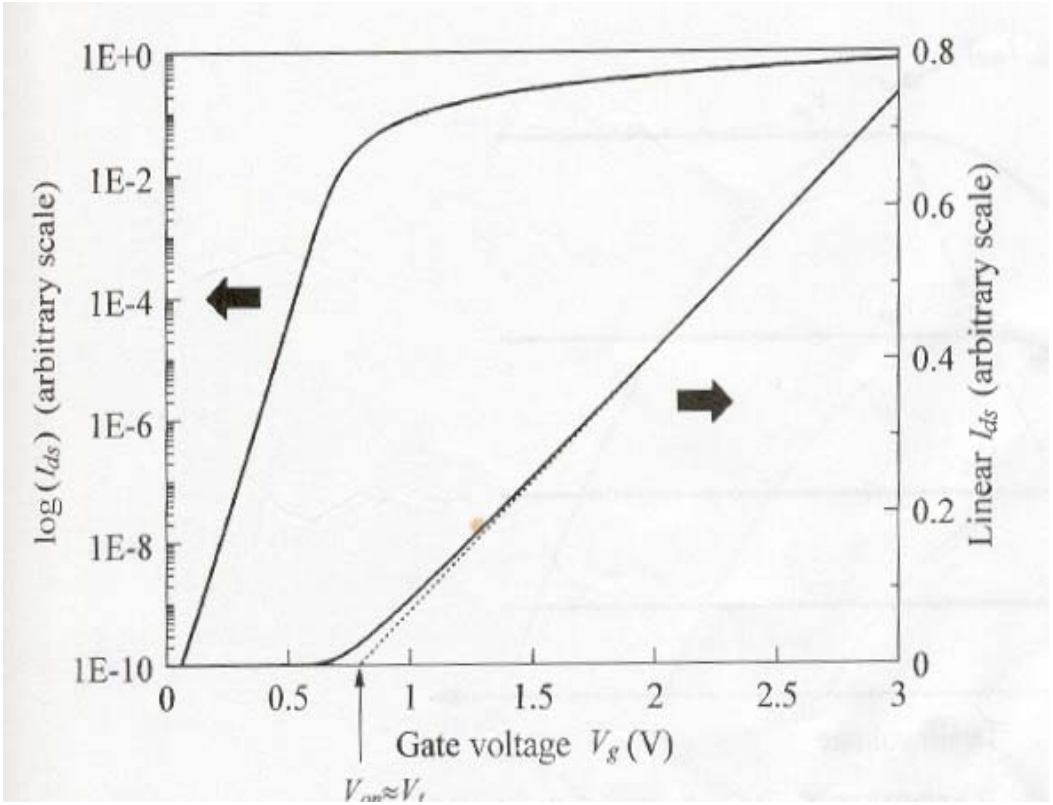


Sub-Threshold Region Behavior of Long Channel MOSFET

Sub-threshold Current

Observation

- Sub-threshold current has an exponential relationship with V_{gs}



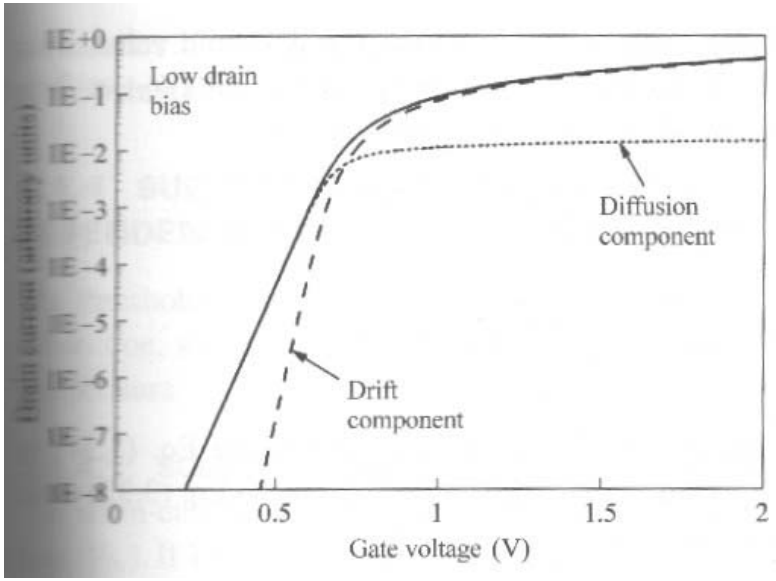
Sub-Threshold Region Behavior of Long Channel MOSFET

Sub-threshold Current

- Unlike the strong inversion region, in which the drift current dominates, sub-threshold conduction is dominated by the diffusion conduction mechanism

- Because Vg is below Vt, almost no electrons inverted at the surface, so the surface potential is determined by the depletion region under that gate and has the nearly same value along the channel. Thus, the electric field along the channel direction is approaching zero, which makes almost no drift current

- Besides, it is also clear from the simulation result of Charge-Sheet Model that diffusion current dominates at sub-threshold region.



Sub-Threshold Region Behavior of Long Channel MOSFET

Sub-threshold Current

- Since the sub-threshold current is dominated by diffusion current. Then,

$$I_{ds}(y) = WD_n \frac{dQ_i}{dy} = \mu_{eff} W \frac{kT}{q} \frac{dQ_i}{dy}$$

- Integrating from y=0 to y=L

$$I_{ds} = \mu_{eff} \frac{W}{L} \frac{kT}{q} \int_{Q_i(y=0)}^{Q_i(y=L)} dQ_i = \frac{W}{L} \mu_{eff} \frac{kT}{q} [Q_i(y=L) - Q_i(y=0)]$$

where, Qi(y=0) and Qi(y=L) are the inversion charge density at source and drain at sub-threshold region (or weak inversion)

- Recall: from MOS-C part, the inversion charge density at weak inversion

$$Q_i = \frac{\sqrt{2qN_A\varepsilon_{Si}}}{2\sqrt{\psi_S}} \frac{kT}{q} e^{q(\psi_S - 2\psi_B)/kT}$$

Sub-Threshold Region Behavior of Long Channel MOSFET

Sub-threshold Current

- Then, with source grounded and drain bias of Vds, the Qi source and drain ends of the channel in a MOSFET under weak inversion can be written as follows:

$$Q_i(y=0) = q\frac{\sqrt{2qN_A\varepsilon_{Si}}}{2\sqrt{\psi_{S0}}}\frac{kT}{q}e^{q(\psi_{S0}-2\psi_B)/kT}$$

$$= \frac{\gamma C_{ox}}{2\sqrt{\psi_{S0}}}\frac{kT}{q}e^{q(\psi_{S0}-2\psi_B)/kT}$$

$$Q_i(y=L) = q\frac{\sqrt{2qN_A\varepsilon_{Si}}}{2\sqrt{\psi_{S0}}}\frac{kT}{q}e^{q(\psi_{S0}-2\psi_B-V_{ds})/kT}$$

$$= \frac{\gamma C_{ox}}{2\sqrt{\psi_{S0}}}\frac{kT}{q}e^{q(\psi_{S0}-2\psi_B-V_{ds})/kT}$$

Here, ψ_{S0} is the surface potential at source end of the channel

- The drain current can be solved as

$$I_{ds} = \frac{\mu_{eff}}{2}\frac{W}{L}\frac{C_{ox}\gamma}{\sqrt{\psi_{S0}}}\left(\frac{kT}{q}\right)^2 e^{q(\psi_{S0}-\psi_B)/kT}\left(1-e^{-qV_{ds}/kT}\right)$$

Sub-Threshold Region Behavior of Long Channel MOSFET

Sub-threshold Current

- Re-arranging the above equation and replacing the ψ_B term, we have

$$I_{ds} = \frac{\mu_{eff}}{2}\frac{W}{L}\frac{C_{ox}\gamma}{\sqrt{\psi_{S0}}}\left(\frac{kT}{q}\right)^2\left(\frac{n_i}{N_A}\right)^2 e^{q\psi_{S0}/kT}\left(1-e^{-qV_{ds}/kT}\right)$$

- Inside above equation, ψ_{S0} can be calculated as below

$$V_g = V_{fb} + \psi_{S0} + V_{ox} = V_{fb} + \psi_{S0} - \frac{Q_S}{Cox} \approx V_{fb} + \psi_{S0} + \frac{|Q_d|}{C_{ox}}$$

here we assume that Q_S=Qd due to weak inversion. Then

$$V_g = V_{fb} + \psi_{S0} + \frac{\sqrt{2\varepsilon_{Si} q N_A \psi_{S0}}}{C_{ox}}$$

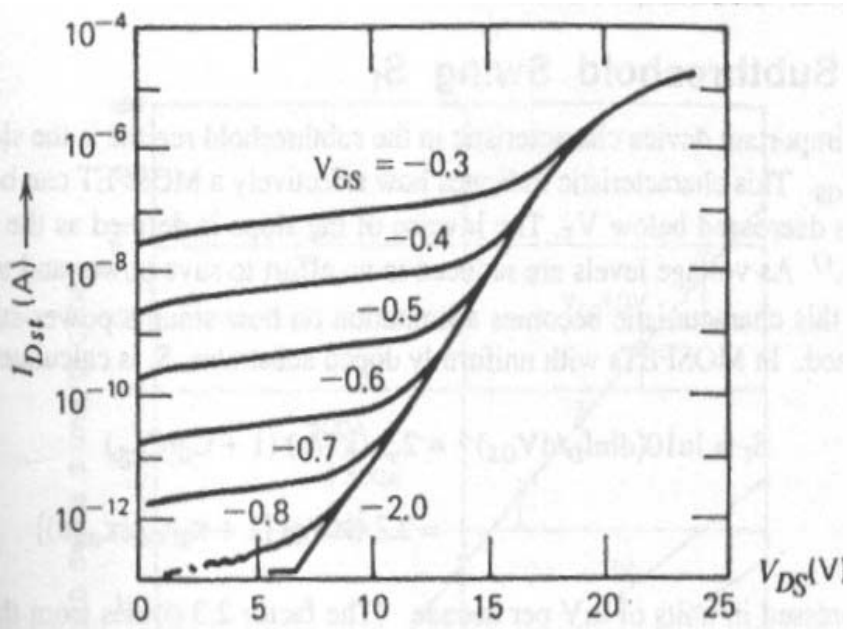
- For each Vg, we are able to calculate ψ_{S0}, and then drain current I_{ds}.

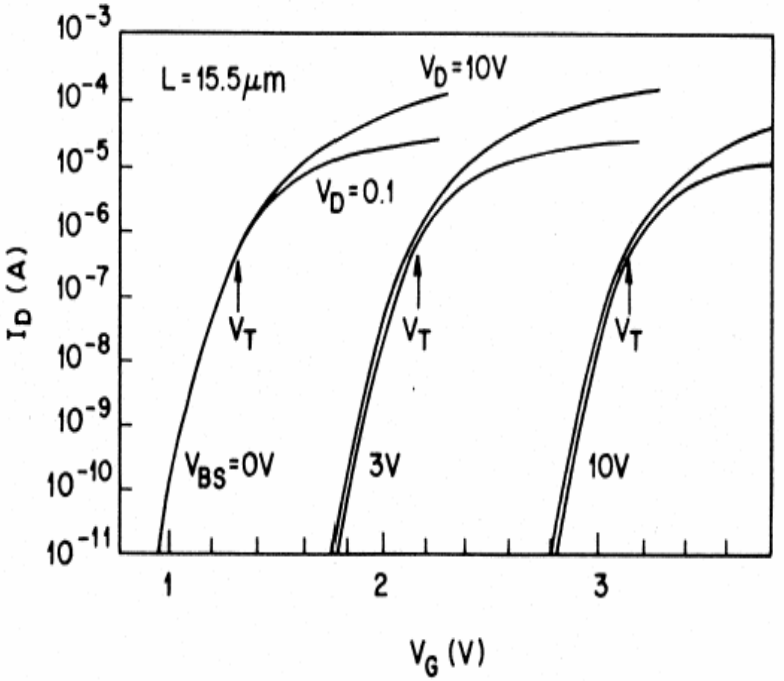
Sub-Threshold Region Behavior of Long Channel MOSFET

Discussion of Sub-threshold Current

Gate voltage dependence

- Sub-threshold current has an exponential relationship with ψ_{S0}, which is corresponding to Vg, so the sub-threshold current increases exponentially with gate voltage Vg.





Sub-Threshold Region Behavior of Long Channel MOSFET

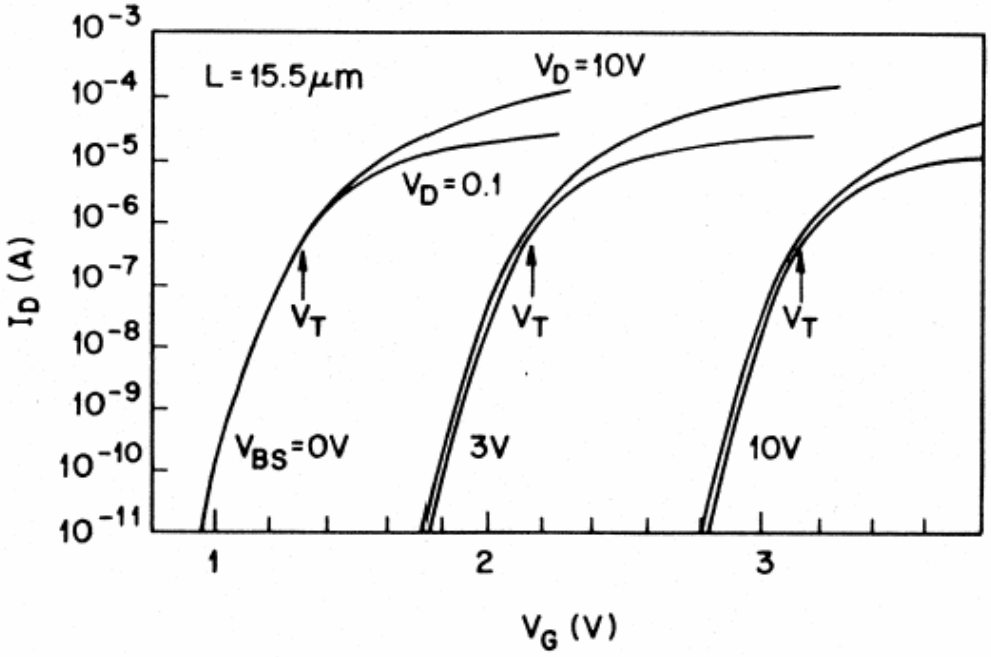
Discussion of Sub-threshold Current

Drain voltage dependence

- Sub-threshold current depends on Vds when Vds is small by

$$I_{ds} \propto (1 - e^{-qV_{ds}/kT})$$

- Sub-threshold current independent with Vds when Vds larger than a few kT/q.



Sub-Threshold Region Behavior of Long Channel MOSFET

Sub-threshold Swing (S)

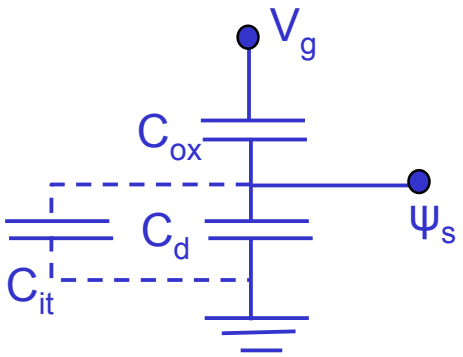
Alternating sub-threshold current form:

- introducing two parameters:
  (i) depletion region capacitance C_d

$$C_d \equiv \partial Q_b/\partial \psi_s = \gamma C_{ox}/(2\sqrt{\psi_s})$$

  (ii) factor η:
  as ψ_s is linearly related with V_{gs}, we introduce η by:

$$\psi_s - 2\psi_B = (V_{gs} - V_t)/\eta$$



- physical view of η:
  capacitive coupling between the gate and silicon surface

$$\eta = 1 + \frac{C_d}{C_{ox}} = 1 + \frac{\gamma}{2\sqrt{2\psi_B}}$$

  If there is a significant trap density (C_{it}: surface state capacitance)

$$\eta = 1 + \frac{C_{it}}{C_{ox}} + \frac{C_d}{C_{ox}}$$

- sub-threshold current:

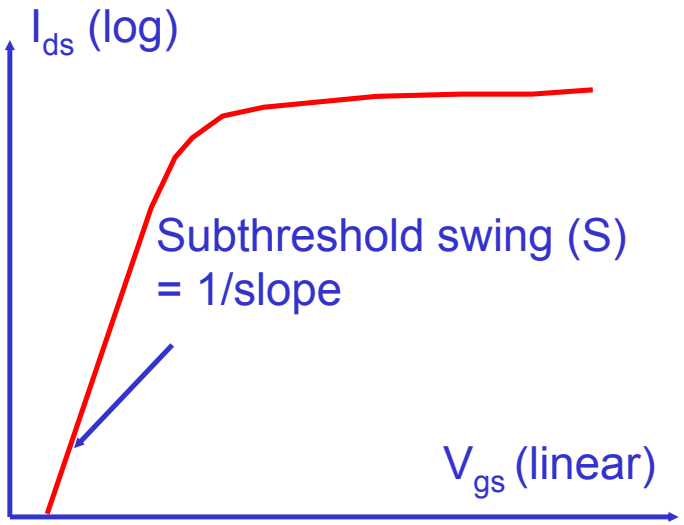
$$I_{ds} = I_{pf}\exp\left[\frac{q(V_{gs}-V_t)}{\eta kT}\right](1 - e^{-qV_{ds}/kT}),\ V_{gs}<V_t$$

where, $I_{pf} = \beta\,(C_d/C_{ox})(kT/q)^2 = \beta\,(\eta-1)(kT/q)^2$, is a pre-factor term.

Sub-Threshold Region Behavior of Long Channel MOSFET

Sub-threshold Swing (S)

- Sub-threshold swing is another important device characteristics in the sub-threshold region
- defined as the change in the gate voltage V_{gs} required to reduce sub-threshold current I_{ds} by one decade
  $S=dV_{gs}/d(\log I_{ds})$
- after detailed calculation, sub-threshold swing (S)
  $S=\eta(kT/q)\ln 10 \approx 2.3(kT/q)\eta$
- smaller value of S, better turn-on performance of device
- minimum swing S_{min} is
  $S_{min} = 2.3(kT/q)= 60$ mV/dec
  at 300K when when the oxide thickness approaches to zero
- S is a convenient measure of the importance of the interface traps on device performance



Sub-Threshold Region Behavior of Long Channel MOSFET

Sub-threshold Swing (S)

$$S = 2.3\frac{kT}{q}\eta = 2.3\frac{kT}{q}\left(1+\frac{C_d}{C_{ox}}+\frac{C_{it}}{C_{ox}}\right)$$

Key dependences of sub-threshold swing (S)

- Gate oxide thickness
  $t_{ox}\downarrow \rightarrow C_{ox}\uparrow \rightarrow \eta\downarrow \rightarrow$ sharper sub-threshold
- Substrate doping
  $N_A\uparrow \rightarrow C_d\uparrow \rightarrow \eta\uparrow \rightarrow$ softer sub-threshold
- Substrate bias
  $|Vbs|\uparrow \rightarrow Cd\downarrow \rightarrow \eta\downarrow \rightarrow$ sharper sub-threshold
- Temperature
  $T\uparrow \rightarrow$ softer sub-threshold

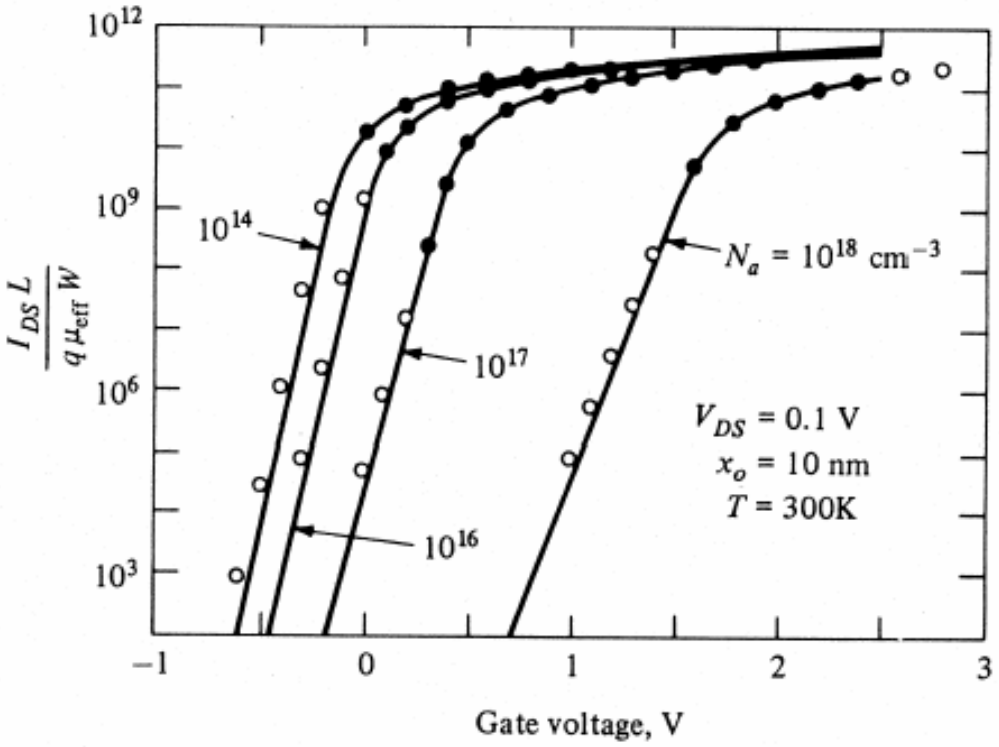
η reflect electrostatic competition between the top gate and body (bottom gate)

Sub-Threshold Region Behavior of Long Channel MOSFET

Sub-threshold Swing (S)

Substrate doping dependence

- Lower substrate doping can have a thicker depletion layer, a lower depletion capacitance, and a smaller S.
- This also reflects that it is easier for the gate electrode to control the lower doping substrate.

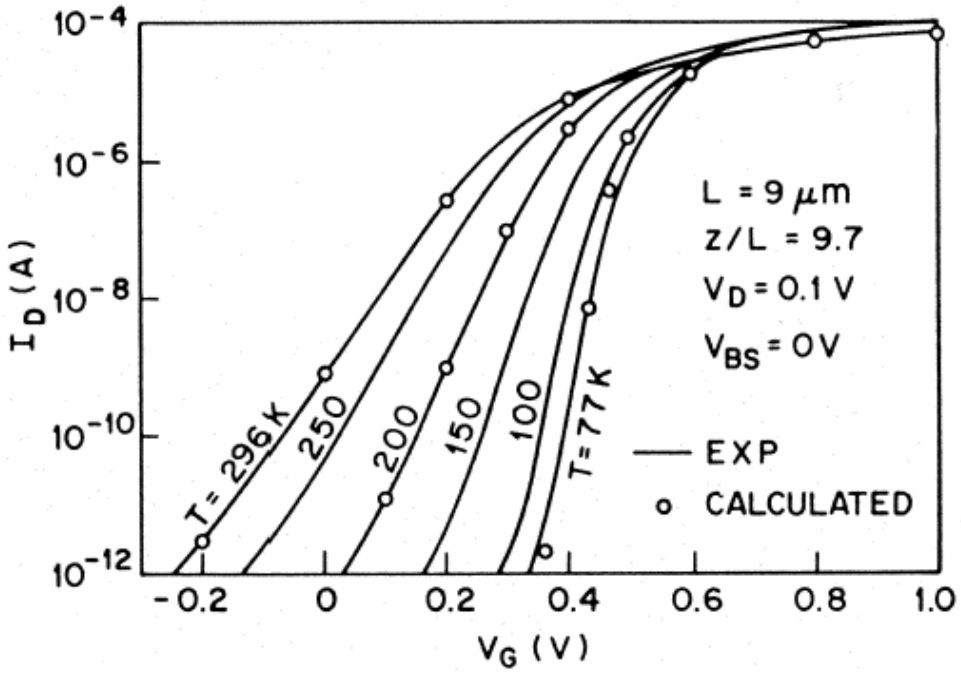


Sub-Threshold Region Behavior of Long Channel MOSFET

Sub-threshold Swing (S)

Temperature dependence

- At room temperature (300K), the ideal limit of S is 60mV/dec
- Normally, devices always work in a higher temperature ambient due to heat dissipation; the S at higher temperature will be higher than room temperature
- S at low temperature can be lowered down significantly
- This is due to that the sub-threshold drain current vs. gate voltage curve is indeed proportional to 1/T

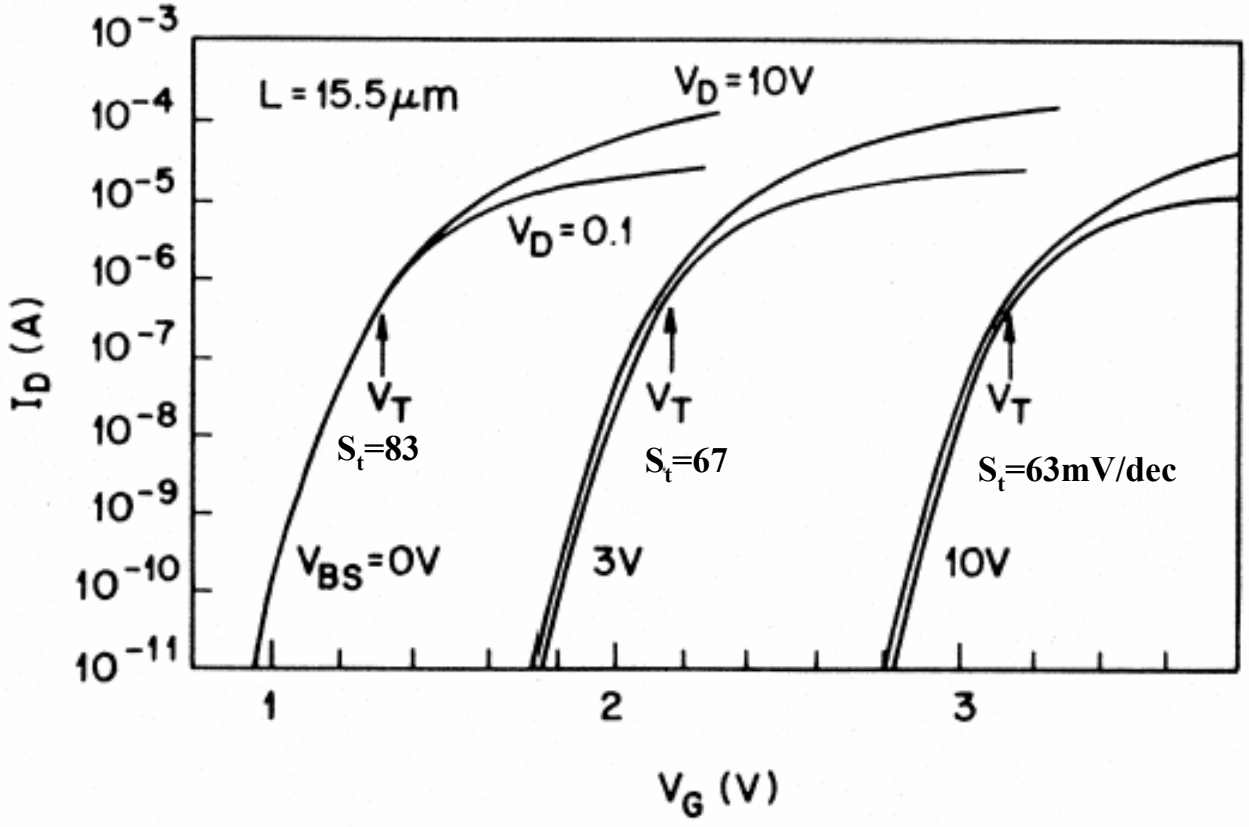


Sub-Threshold Region Behavior of Long Channel MOSFET

Sub-threshold Swing (S)

Substrate bias dependence

- Since the depletion thickness increases when a substrate bias is applied, the sub-threshold swing decreases also



Sub-Threshold Region Behavior of Long Channel MOSFET

Sub-threshold Swing (S)

Off current

- Sub-threshold region is important since it determines the off current

$$I_{off} = I_{ds}(V_{gs} = 0V) \approx \mu_{eff} \frac{W}{L} (\frac{kT}{q})^2 \exp(-qV_t / \eta kT)$$

- To achieve I_{off} ↓

  (i) L↑ → Performance↓

  (ii) V_t↑→ Performance ↓

  (iii) η↓ → N_A↓ → "short channel" effect↑
  → t_{ox}↓→ field on gate oxide↑→ reliability issue

- I_{off} is a critical design goal in logic devices since it contributes to DC power dissipation in CMOS

Sub-Threshold Region Behavior of Long Channel MOSFET

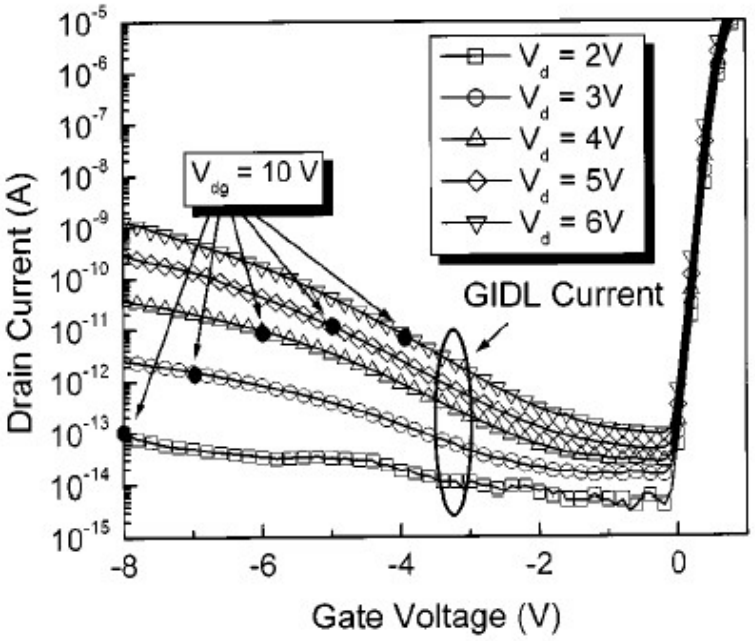
Gate Induced Drain Leakage (GIDL) Current

Observation

- it was observed that the excess drain current exist when gate bias further reduce below V_t and move to negative side, which is called Gate Induced Leakage (GIDL) current

- The GIDL current dominates at a negative bias of Vgs and positive bias of Vds. The larger difference between Vds and Vgs (i.e., Vds-Vgs), the higher GIDL current will have.

- Since the GIDL current can generate excessive heat dissipation, it needs to be maintained below some specified value, for example, 10pA/μm.

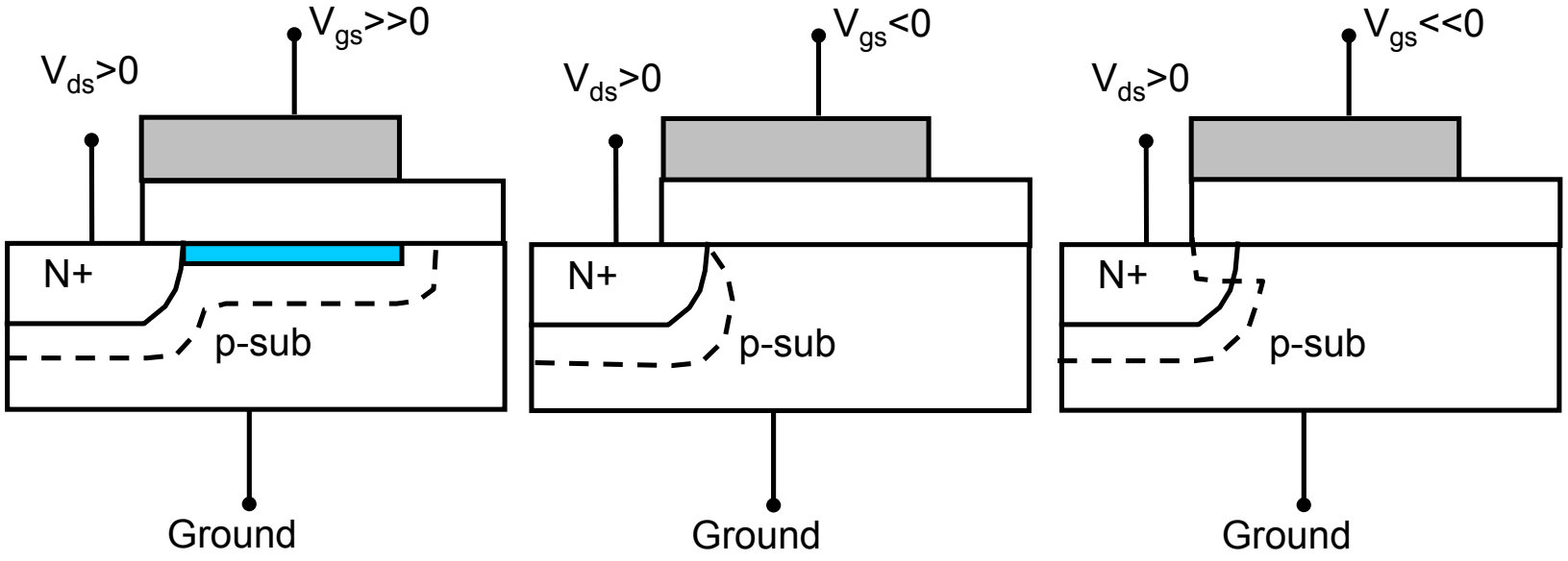


Sub-Threshold Region Behavior of Long Channel MOSFET

Gate Induced Drain Leakage (GIDL) Current

Depletion regions at MOS gated diode

Case (a): Vds>0, Vgs>>0: channel Inversion
Case (b): Vds>0, Vgs<0: channel accumulation
Case (c): Vds>0, Vgs<<0: surface of n+ region is depleted or inverted



Sub-Threshold Region Behavior of Long Channel MOSFET

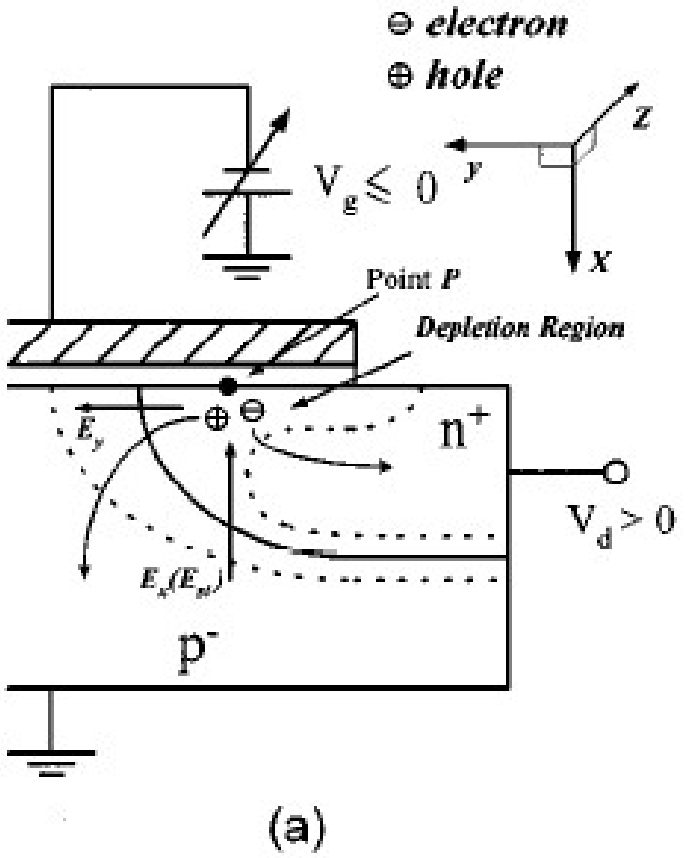
Gate Induced Drain Leakage (GIDL) Current

Analysis of GIDL Current

- Tunneling creates electron and hole pairs
- Electron will tunnel through the barrier height and collected by the n+ drain, which positive biased.

- Hole will be collected by substrate since it is grounded

- A lot of mechanisms may involve during the electron tunneling, such as band-to-band direct tunneling, trap assisted tunneling, etc, depending on the biases of Vgs and Vds.

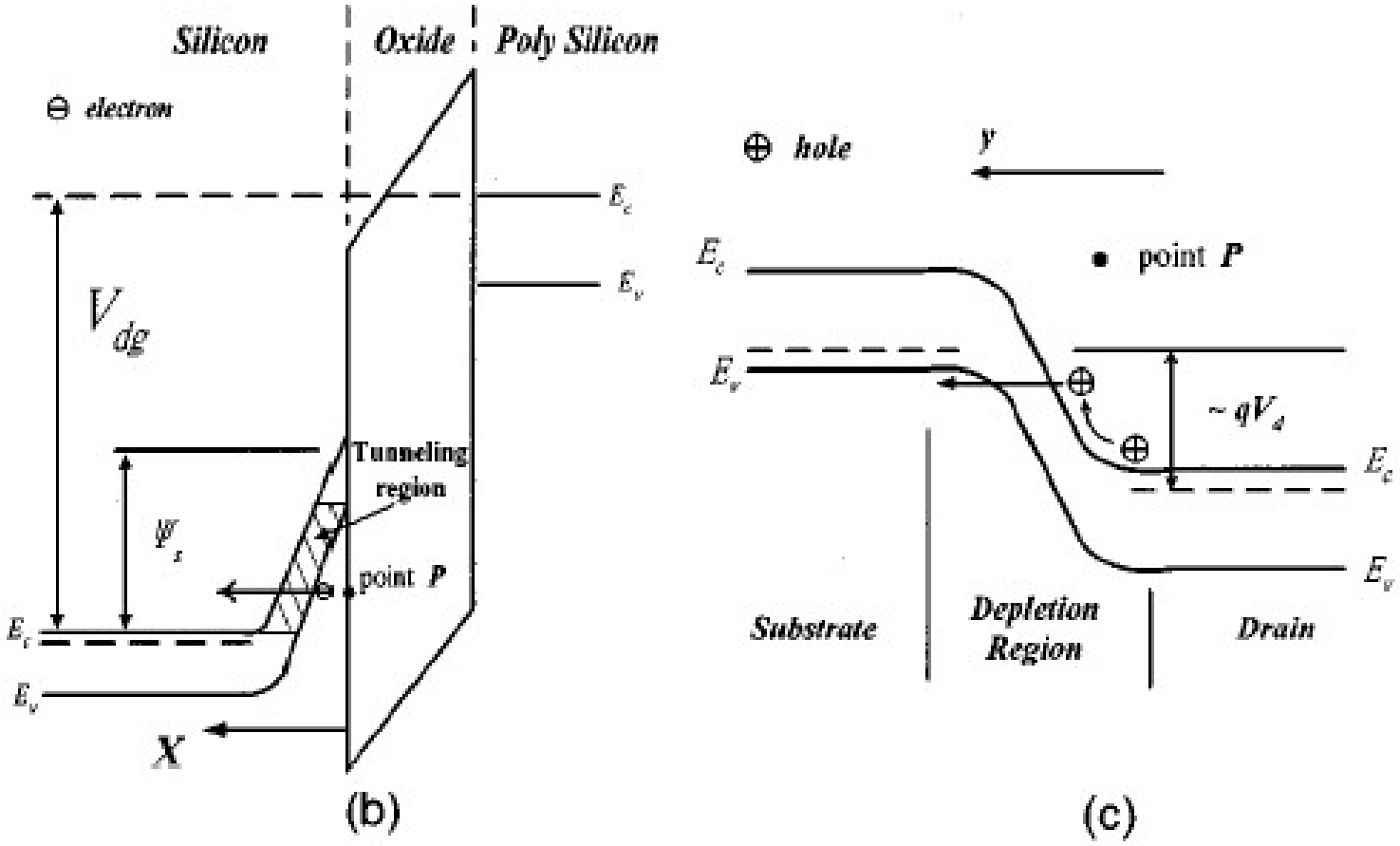


(a)

JH Chen, et al, "An analytic three-terminal band-to-band tunneling model on GIDL in MOSFET," IEEE TED, Vol. 48, pp. 1400, 2001.

Sub-Threshold Region Behavior of Long Channel MOSFET

Gate Induced Drain Leakage (GIDL) Current

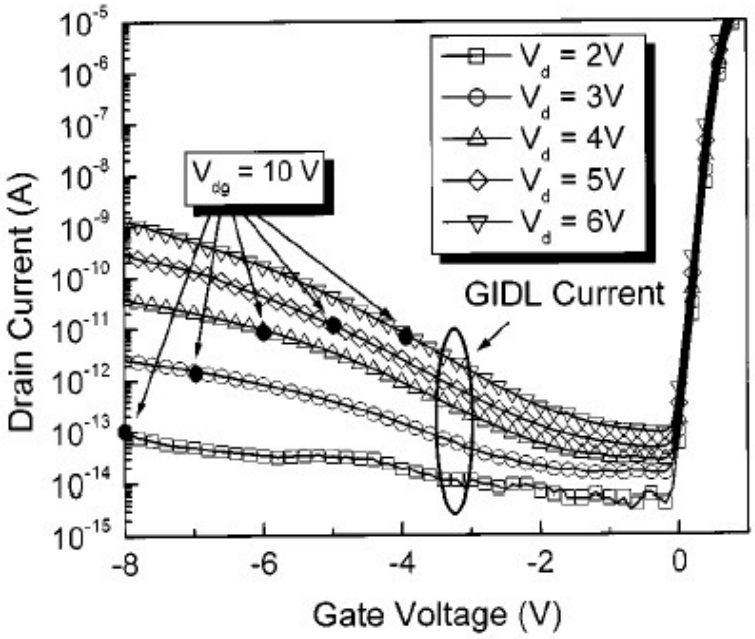


Sub-Threshold Region Behavior of Long Channel MOSFET

Gate Induced Drain Leakage (GIDL) Current

Analysis of GIDL Current

- For the same Vgs, higher Vds (more positive) will make the barrier more steeper and cause the tunneling easier to happen, so leads to a higher GIDL current.
- For the same Vds, a more negative Vgs will also make the barrier more steeper and causes the tunneling easier to happen, so also leads to a higher GIDL current
- When a lot of impurities are involved in the drain region, more traps will be introduced, make the trap-assisted tunneling easier to happen, and hence a higher GIDL current.



Sub-Threshold Region Behavior of Long Channel MOSFET

Gate Induced Drain Leakage (GIDL) Current

How to reduce GIDL Current

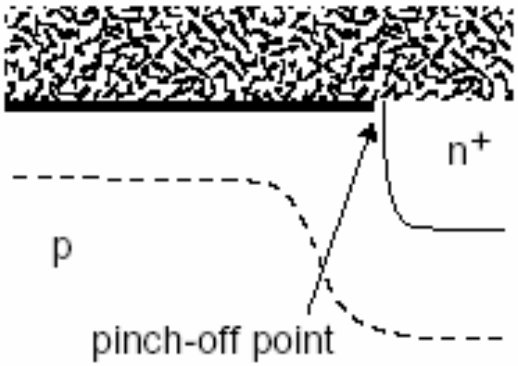
- Increase the oxide thickness *tox* to reduce the electric field
- Using LDD (lightly doped drain: LDD) structure to reduce the electric field near the drain side
- Decrease the trap density
- Increase the doping concentration of the drain to decrease the depletion layer width

Beyond Saturation Behavior of Long Channel MOSFET

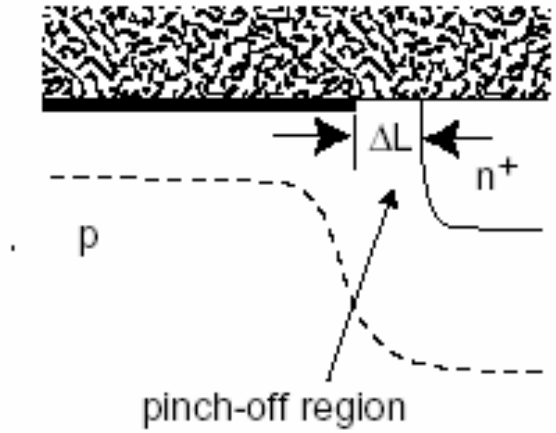
Channel Length Modulation (CLM)

As V_{ds} increase and beyond V_{dssat}

- V_{ds}-V_{dssat}↑→ effective channel length↓ (L→L-ΔL) → drain current↑→ no more staurated



b) pinch-off $V_{DS}=V_{DSsat}$



c) saturation regime $V_{DS}>V_{DSsat}$

Beyond Saturation Behavior of Long Channel MOSFET

Channel Length Modulation (CLM)

- Considering CLM, the drain current in saturation region becomes

$$I_{ds} = \frac{I_{dssat}}{1-\frac{\Delta L}{L}} \approx I_{dssat}\left(1+\frac{\Delta L}{L}\right)$$

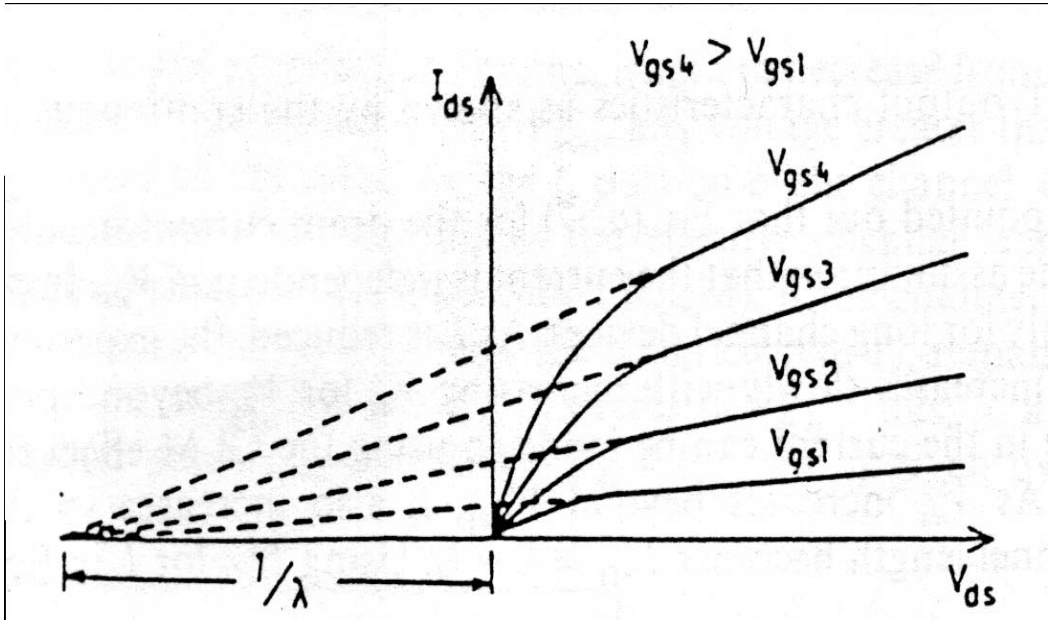
- Introducing an empirical relation

$$1+\frac{\Delta L}{L} = 1+\lambda V_{ds}$$

we can obtain

$$I_{ds} = I_{dssat}(1+\lambda V_{ds})$$

where λ is defined as Channel Length Modulation Parameter, representing small influence of drain voltage on drain current.

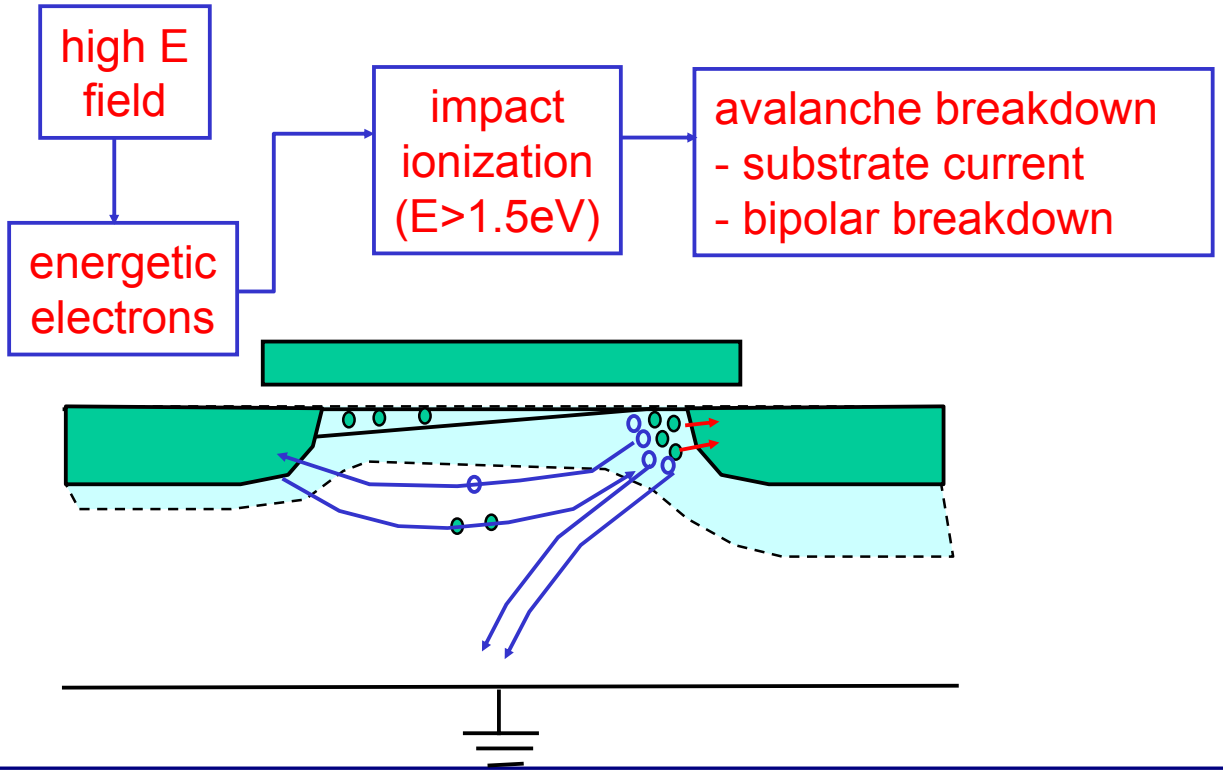


- The λ can be determined by extrapolating the *Ids-Vds* curves backward, as shown in the figure above.

Beyond Saturation Behavior of Long Channel MOSFET

MOSFET Breakdown

- impact of high channel field
  - ⇒ high field leads to energetic (hot) electrons
  - ⇒ hot electrons cause impact ionization
  - ⇒ and leading electrons go to drain and holes go to substrate to form the substrate current



Beyond Saturation Behavior of Long Channel MOSFET

MOSFET Breakdown

- MOSFET breakdown

  $\Rightarrow$ as I_{sub} flows to the body terminal, a body potential of $I_{sub}R_{sub}$ is developed

  $\Rightarrow$ when $I_{sub}R_{sub}$ < 0.6 V (the turn-on voltage of a PN junction), the increase in body potential reduces V_{th} (same as applying a body bias) and leading to drain current increase

  $\Rightarrow$ when $I_{sub}R_{sub}$ > 0.6 V, source/body junction turns on and electrons injected from source to body

  $\Rightarrow$ these injected electrons diffuse through the substrate and collected at the reverse biased drain/body junction (in fact, leading parasitic bipolar transistor npn action)

  $\Rightarrow$ thus, the maximum drain voltage is limited

Different Types of MOSFET

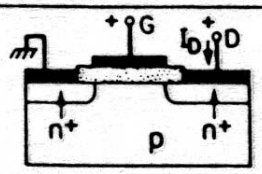
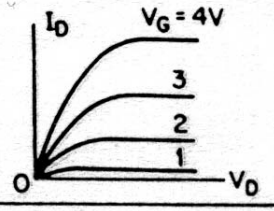
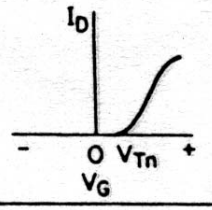
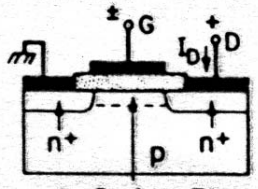
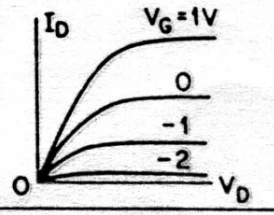
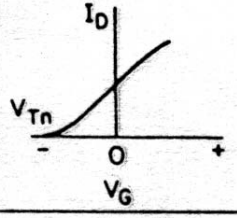
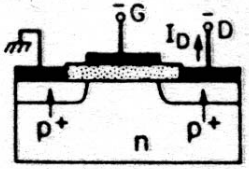
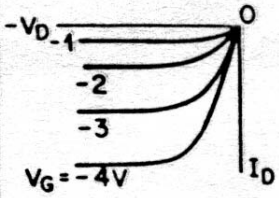
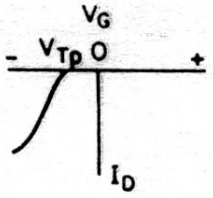
Classification of MOSFETs

- Enhancement mode
  - ⇒ normally off
  - ⇒ channel doping is same as substrate doping type
  - ⇒ always called inversion mode

- Depletion mode
  - ⇒ normally on
  - ⇒ channel doping is opposite of the substrate doping type

Different Types of MOSFET

Classification of MOSFETs

TYPE	CROSS SECTION	OUTPUT CHARACTERISTICS	TRANSFER CHARACTERISTICS
n-CHANNEL ENHANCEMENT (NORMALLY OFF)			
n-CHANNEL DEPLETION (NORMALLY ON)			
p-CHANNEL ENHANCEMENT (NORMALLY OFF)			
p-CHANNEL DEPLETION (NORMALLY ON)