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EKV 3.0: An Analog Design-Oriented MOS Transistor Model

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ABSTRACT:
The EKV 3.0 compact MOS transistor model for advanced analog IC design and simulation is presented. The model is based on the surface potential approach combined with inversion charge linearization. The ideal long-channel model is coherent for static and dynamic aspects including noise. The ideal model is extended for high-field effects in deep submicron CMOS technologies. Scalability over channel length and width is achieved while retaining a reduced number of parameters. The EKV 3.0 model is applicable over a large range of CMOS technologies.

INTRODUCTION

The original approach to MOSFET modeling [1][2] called EKV was the first to propose a symmetric, bulk-referred handling of the MOS transistor (MOST), applicable to all levels of inversion including weak and strong inversion. The transconductance-to-current ratio, an important quantity for analog CMOS IC design, could be expressed with a continuous, although empirical function, offering for the first time a continuous solution to model the MOS transistor from weak to strong inversion, in a symmetric way.
More recently, a charge-based and truly physical solution [3] led to the development of the so-called EKV 2.6 MOST compact model [4][5][6], which has found a wide distribution in many circuit simulators [5] and which is used by a number of analog IC design groups today for a wide range of CMOS technologies.

The EKV 3.0 Compact MOST Model

The research activities since 1997, while maintaining the fundamental aspects, have brought important innovations in many ways [6][7][8][9][10] [11][12][13][14][15][16][17]. These aspects and further research are at the time of writing being concretized as the EKV 3.0 MOST model. Its main characteristics are the following:

- Based on surface-potential description of the MOS physics.
- Inversion charge linearization vs. surface potential (including when polydepletion [10] and quantum effects [14] are present) leading to analytical relationships among charge, current, terminal voltages.
- A consistent normalization of all model internal quantities facilitates analysis and understanding of MOS physics.
- Symmetric handling of source and drain sides, and using bulk as the reference terminal.
- Static, dynamic quasi-static [8][9] and non-quasi-static [11][12] models, as well as thermal noise [9], can be expressed within the same coherent charge-based approach.
- The local charges description is used to build an advanced mobility model [7][9][17] including different scattering mechanisms as well as velocity saturation and channel length modulation.
- The model considers non-uniform vertical [7] and lateral doping profiles and oxide charge [15] leading to reverse short-channel effect (RSCE).
- The model is further extended to account for short- and narrow-channel effects such as drain induced barrier lowering (DIBL), charge-sharing [17].
- Extended scaling abilities including combined short/narrow channel effects, while maintaining a reasonable number of parameters.
- Extended RF capabilities including non-quasi-static small-signal modeling [11][12], hot-carrier related increase of short-channel thermal noise [9] and accounting for RF-layout related aspects such as number of fingers.
- Availability of design-oriented features such as level-of-inversion-centered information, the possibility to include local mismatch [4] in statistical circuit simulation via intrinsic matching parameters, and the possibility of simulating stacked (series) transistors.

The model's basic formulation and characteristics will be illustrated in the present paper. Important relationships among model quantities are established.
One aspect that distinguishes this model resolutely from other common MOSFET models is its orientation towards advanced analog design-practice, which is combined as well with characterization techniques addressing not only strong inversion but also and specifically moderate and weak inversion [18][19].

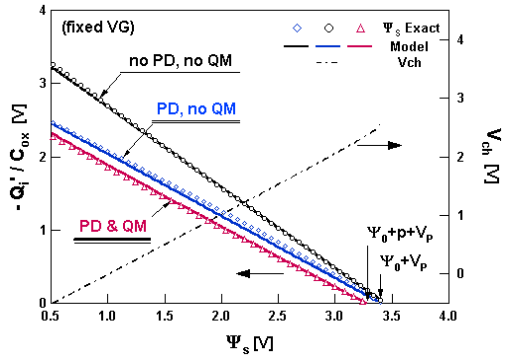

Figure 1. *Inversion charge vs. surface potential at fixed gate voltage; effect of polydepletion and quantum effects, numerical (markers) and linearization (lines).*

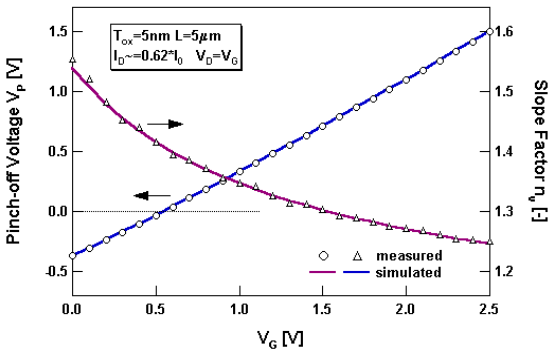

Figure 2. *Pinch-off voltage and slope factor vs. gate voltage for an NMOS transistor of a deep submicron CMOS technology.*

EKV 3.0 MODEL FORMULATION

Linearization of Inversion Charge vs. Surface Potential

The relationship between gate voltage V_G, surface potential y_S and inversion charge Q_i' in a MOS structure can be written [2][20],

$$V_G - V_{FB} = y_S + g\sqrt{y_S} - Q_i'/C'_{ox} \quad (1)$$

where V_{FB} is the flat-band voltage, g the substrate effect factor, and C'_{ox} the gate oxide capacitance. As can be seen in Fig. 1., the relationship between Q_i' and y_S for a fixed V_G is essentially linear – even in the case where polydepletion [10] and quantum effects [13][14] are considered in (1). This allows us to define the *charge linearization factor*, n_Q [3][9][10][13][14]:

$$dQ_I'/C_{OX}' = n_Q \cdot dy_S \quad (2)$$

Approximating $y_S \cong V_{ch} + y_0$ in strong inversion where V_{ch} is the channel voltage and y_0 approximately twice the Fermi potential, and assuming $Q_i' \approx 0$ in (1), the pinch-off voltage V_P is defined and approximately expressed as [2],

$$V_P \cong \frac{V_G - V_{TO}}{n_v} \qquad n_v \cong 1 + \frac{g}{2\sqrt{V_P + y_0}} \quad (3)$$

where $V_{TO} = V_{FB} + y_0 + g\sqrt{y_0}$ is the *threshold voltage* and n_v the *slope factor* (defined as the inverse derivative of V_P vs. V_G), both shown in Fig. 2, measured according to the procedure described in [21]. The slope factor has typical values $1.6 > n_v > 1$; n_v is notably governing the relationship among source and gate transconductance as discussed later. n_v depends mainly on g and on the gate voltage.

Relationships among voltage, inversion charge, drain current and transconductances

The current transport equation [20],

$$I = W \cdot m \cdot \left(U_T \cdot \frac{dQ_i'}{dx} - Q_i'(x) \cdot \frac{dy_S}{dx} \right) \quad (4)$$

is combined with (2), integrated along the channel, and results in an expression for the drain current as a symmetric function of a forward and a reverse current [1][2],

$$I_D = I_F - I_R \quad (5)$$

$$I_{F(R)} = I_0 \cdot i_{f(r)} \;;\; I_0 = 2n_q U_T^2 m C'_{ox} \frac{W}{L} \quad (6)$$

where I_0 is the *specific current*, U_T the *thermal voltage*, and m the *mobility*. The inversion charge densities at source and drain are written,

$$Q'_{iS(D)} = Q_0 \cdot q_{f(r)} \qquad Q_0 = 2n_q U_T C'_{ox} \quad (7)$$

which can be related to the forward and reverse currents as [9][11][15][16],

$$i_{f(r)} = q_{f(r)}^2 + q_{f(r)} \;;\; q_{f(r)} = \sqrt{\frac{1}{4} + i_{f(r)}} - \frac{1}{2} \quad (8)$$

Channel conductance and inversion charge are related as [2],

$$\frac{dI}{dV_{ch}} = m\frac{W}{L}(-Q_i') \Rightarrow -\frac{di_{f(r)}}{dv_{S(D)}} = q_{f(r)} \quad (9)$$

representing the small-signal relationship, which, in terms of normalized current, is written [6][8][9][15][16],

$$-\frac{di_{f(r)}/dv_{S(D)}}{i_{f(r)}} = \frac{1}{\sqrt{\frac{1}{4} + i_{f(r)}} + \frac{1}{2}} \quad (10)$$

This fundamental relationship corresponds to the normalized transconductance-to-current ratio [2][6][9], shown in Fig. 3. – a universal quantity that characterizes CMOS technology, independently of the

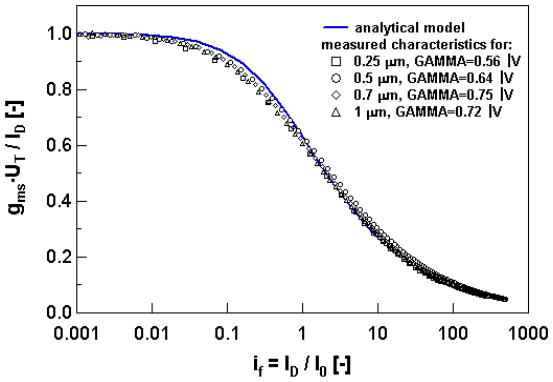

Figure 3. *Normalized source transconductance to current ratio vs. normalized current, measured (markers) in saturation from various CMOS technologies, and analytical model.*

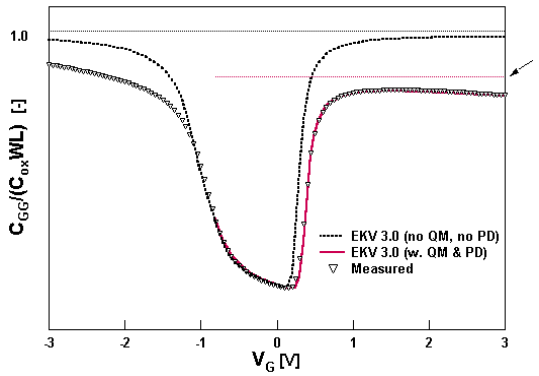

Figure 4. *Gate capacitance vs. gate voltage, measured (markers) for a deep submicron CMOS process, EKV 3.0 model with (line) and without (dashed) polydepletion and quantum effects.*

channel type, gate voltage, temperature, as well as transistor geometries [9] as long as no strong short-channel effects arise [15].

Supposing operation in saturation, current levels in weak inversion correspond to roughly $i_f < 0.1$, moderate inversion to $0.1 < i_f < 10$, and strong inversion to $i_f > 10$. The center of moderate inversion corresponds to $i_f \cong 1$. The normalized source transconductance to current ratio reaches its maximum of 1 in weak inversion. The level-of-inversion-centered information is particularly suitable to qualitative and quantitative understanding and analysis of the fundamental variables in the MOS transistor.

Integrating (10) yields the important relationship among voltage and inversion charge [6][8][9][11],

$$v_P - v_{S(D)} = 2q_{f(r)} + \ln(q_{f(r)}) \quad (11)$$

where $v_P = V_P / U_T$ and $v_{S(D)} = V_{S(D)} / U_T$. The relationship (11) cannot be analytically inverted; however, in a computer implementation, this can be done efficiently with analytical approximations.

From the above relations, all important model quantities can be obtained. Notably, a description of local inversion and depletion charge densities are obtained, from which total node charges can be obtained through integration along the channel [8][9]. Transcapacitances are obtained via derivation of the node charges, completing the quasi-static description of the MOS structure. Figure 4 illustrates the modeling of total gate capacitance, including notably the polydepletion and quantum effects, for a deep submicron CMOS technology.

Furthermore, a small-signal analysis allows the derivation of a complete non-quasi-static (NQS) dynamic model [11][12][16] which is entirely coherent with the quasi-static model.

Finally, thermal noise is proportional to the total inversion charge in the MOS channel [2][9].

Transconductances may be defined as,

$$g_m \equiv \frac{dI_D}{dV_G} \quad g_{ms} \equiv -\frac{dI_D}{dV_S} \quad g_{md} \equiv \frac{dI_D}{dV_D} \quad (12)$$

Useful relationships among the transconductances can be established,

$$g_m = \frac{g_{ms} - g_{md}}{n_v} \quad g_m \cong \frac{g_{ms}}{n_v} (saturation) \quad (13)$$

where the latter relationship shows that gate transconductance is always smaller than source transconductance (since $n_v \geq 1.0$).

Bias-dependence and scaling of model quantities

The above relationships stress the importance of the slope factor, which is affected in several ways. n_v depends on the doping profile [7]; it is furthermore notably increased by polydepletion and quantum effects [15]; it is however decreased by charge-sharing in short-channel devices, for which n_v indeed tends to 1. The resulting inverse weak inversion slope, $S \cong 2.3 \cdot U_T \cdot n_v$, would therefore increase for shorter channels; however, this is in practice often counterbalanced by the reduced weak inversion asymptote of the source transconductance to current ratio due to drain induced barrier lowering (DIBL) as shown in [15].

Mobility, which was assumed constant throughout the previous model derivation, is indeed dependent on the vertical and lateral field. Vertical-field dependences are modeled via charge-based expressions mobility terms, accounting for surface roughness-, phonon- and Coulomb-scattering [9][17]. The mobility expressions account for the position-dependence of mobility along the channel. Velocity saturation and channel length modulation are included similarly with charge-based expressions, a variable-order [9].

Finally, the charges approach is also used to account for series resistance within the mobility model as an option, resulting in a substantial gain in efficiency for non-critical applications.

CONCLUSIONS

Fundamental features of the EKV 3.0 MOS Transistor compact model have been outlined. The model is based on a surface potential description and uses linearization of inversion charge vs. surface potential to achieve a highly consistent analytical framework for compact modeling. All model quantities, drain current, transconductances, charges, transcapacitances, including also non-quasi-static effects, and thermal noise can be expressed within the same ideal model approach. Extensions for polydepletion and quantum effects are generalizations of the same approach. The local charges model is furthermore used to build effective-field dependent mobility expressions. Short- and narrow-channel effects are introduced mainly via bias- and geometry-dependences of the basic variables, particularly substrate effect factor and threshold voltage. The EKV 3.0 MOS transistor model is an efficient compact model, combining a coherent physics-based framework including proper extensions for high-field effects, with analytical versatility for advanced analog IC design and simulation.

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