Parasitic Turn-on of Power MOSFET – How to avoid it?

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Automotive

Never stop thinking.

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1 Abstract

The aim of this Application Note is to give an overview of the mechanism behind the parasitic turn-on of the power MOSFET and to give guidance on how to choose the proper MOSFET in order to avoid this unwanted effect.

2 Parasitic switch-on of the power MOSFET

The parasitic, or unwanted, turn-on of the power MOSFET is a phenomenon which happens in the reality more often and can cause more damage then usually known. Its appearance often leads to the destruction of the MOSFET and it is afterwards not easy, if possible at all, to divine the true cause of the failure. The mechanism of the parasitic switch-on lies in the capacitive voltage divider between drain-to-source and gate-to-source voltage.

Fig. 1.shows a basic half-bridge configuration, being a part of an H-bridge or a three-phase bridge. If the upper MOSFET is switched on, the lower one has to be switched off in order to avoid a shoot-though and thus a possible MOSFET failure due to over current.

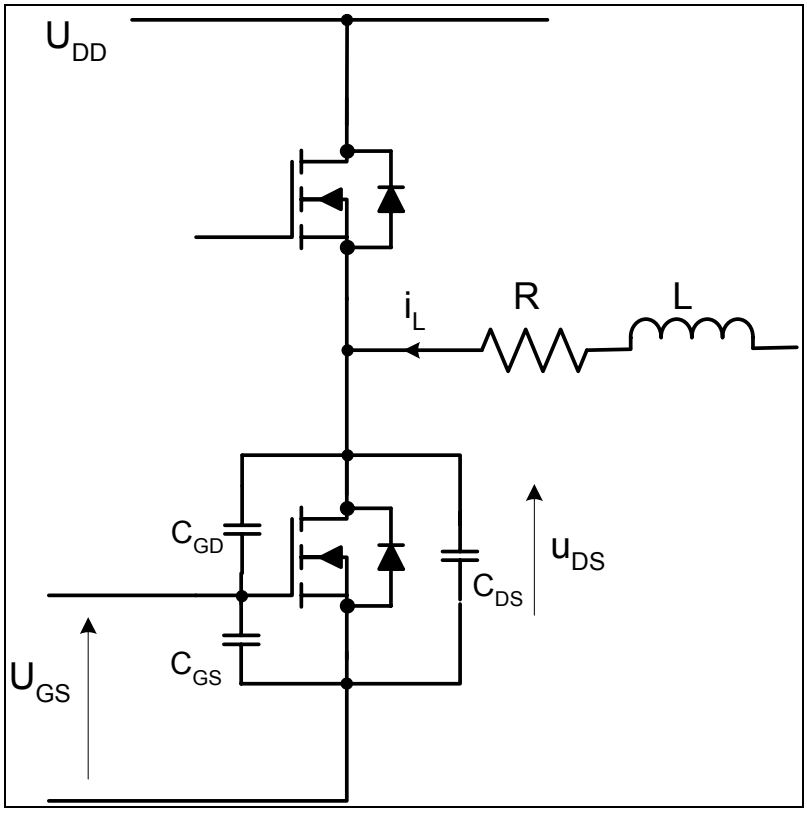

Figure 1 MOSFET half-bridge with an inductive load

In this state, the voltage between gate and source can be expressed as:

$$U_{GS} = \frac{C_{GD}}{C_{GD} + C_{GS}} U_{DS} \quad (1)$$

Therefore, even if the driver circuit tries to switch the lower MOSFET off, i.e. the voltage between gate and source is set to zero Volts (U_{GS}=0V) by driver circuit, there is always intrinsic danger that the MOSFET turns on because of the change in drain-to-source voltage and the voltage divider consisting of Miller capacitance (C_{GD}) and gate-to-source capacitance. This capacitive divider is the fastest possible voltage divider and thus reacts very quickly on all voltage transients between drain and source, especially on high frequency components of this voltage (i.e. U_{DS} components with high du/dt values). Placing a resistor between gate and source is somewhat helpful, but just a little and not against high du/dt values.

Just how high and how fast these voltages can be, is illustrated in the following example:

The basic half-bridge design of an inverter leg with parasitic components is shown in fig. 2. Parasitic inductances, resistances and capacities, as caused by layout and geometric constraints or even MOSFET bond wires, are unavoidable. On the other side, the inverter half bridge is the circuit part with the highest di/dt value, typically about 1A/ns, while the current in the phases of the motor as well as the current in the supply line changes relatively smoothly.

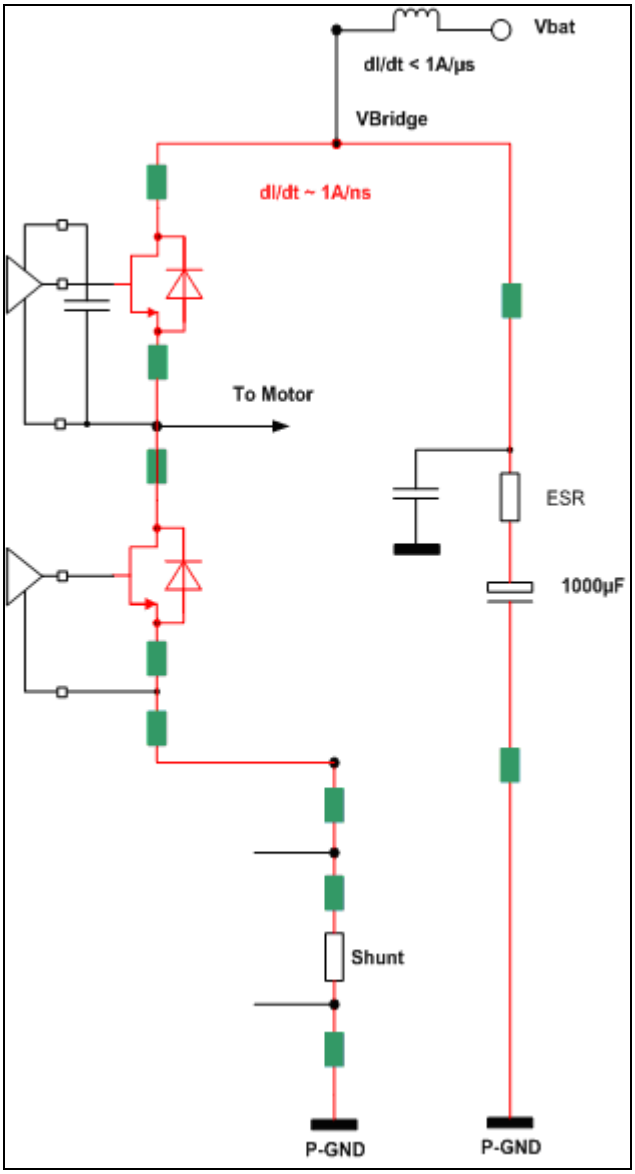

Figure 2 Basic design of inverter half bridge with some inductive parasitics (green)

The highest di/dt in the bridge is usually caused by the diode recovery pulse of the MOSFETs. The combination of parasitic inductances and high di/dt induces causes more or less high inductive voltage spikes and can cause a significant HF ringing in the bridge. Dependent on the size of the parasitic inductances, over- and under voltage spikes can be seen in 12V applications, ranging between 1-2V and several 10V. Beside the higher noise problem, these voltage spikes can endanger MOSFETs, bridge drivers and other ECU components. Exactly these voltage spikes can also cause the unwanted turn-on of the power MOSFET.

3 How to choose a power MOSFET in order to avoid parasitic turn-on

Revisiting of the equation (1) shows

$$U_{GS} = \frac{C_{GD}}{C_{GD} + C_{GS}} U_{DS} \Rightarrow \frac{U_{DS}}{U_{GS}} = \left(1 + \frac{C_{GS}}{C_{GD}}\right)$$

Since in order to prevent the parasitic switch-on the ratio U_{GS}/U_{DS} has to be as low as possible, the ratio U_{DS}/U_{GS} has to be as high as possible and therefore the ratio C_{GS}/C_{GD} has to as high as possible, as well. Thus, it can be recommended that:

In order to have a low sensitivity to parasitic turn-on, a C_{GS}/C_{GD} ratio has to be as high as possible, possibly >15 (or at the very least >10).

How to extract those values from the datasheet is given in the following example (for IPB80N04S3-03, OptiMOS-T 40V power MOSFET, optimised for electric motor drives application):

Since:

$$Ciss = C_{GS} + C_{GD}$$
$$Crss = C_{GD}$$

It can be calculated that: C_{GD_typ}=240pF and C_{GS_typ}=5360pF. The ratio C_{GS}/C_{GD} is 22.3, which is completely safe against parasitic turn-on.

IPB80N04S3-03
IPI80N04S3-03, IPP80N04S3-03

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	
Dynamic characteristics[2)]						
Input capacitance	C_{iss}	V_{GS}=0 V, V_{DS}=25 V, f=1 MHz	-	5600	7300	pF
Output capacitance	C_{oss}		-	1540	2000	
Reverse transfer capacitance	C_{rss}		-	240	350	

Figure 3 Table datasheet values for the capacitances

To get these dependencies at different supply voltages, the typical dependencies of the gate-to-drain and gate-to-source capacitances on the drain-source voltage are given in the datasheet, as shown in the fig. 4.

Figure 5 gives a comparison between state of the art MOSFETs for high current applications, like safety critical electric or electro-hydraulic power steering or starter-alternator applications. It can be seen that with IPB160N04S3-H2 the potential for parasitic turn-on is as well as not existing, while with other two MOSFETs it looks much more critical.

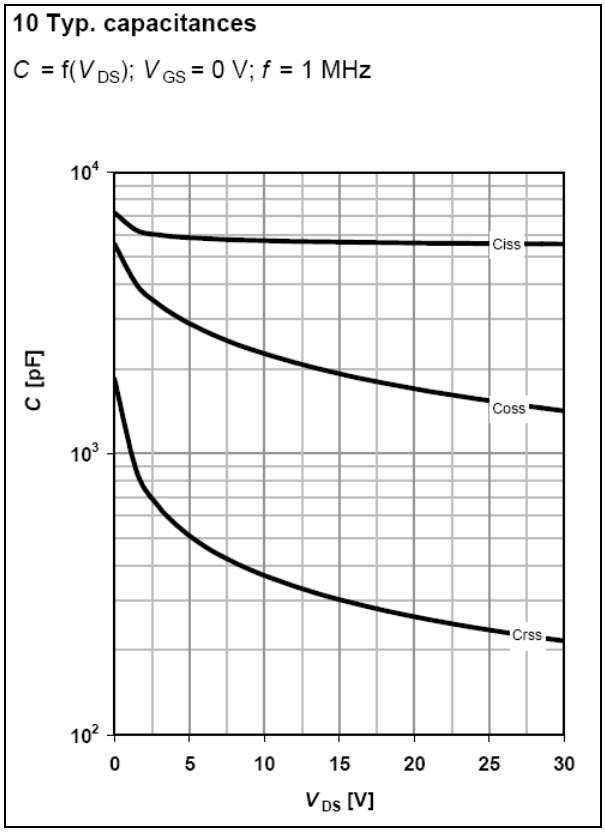

Figure 4 Typical dependencies of the gate-to-drain and gate-to-source capacitances on the drain-source voltage

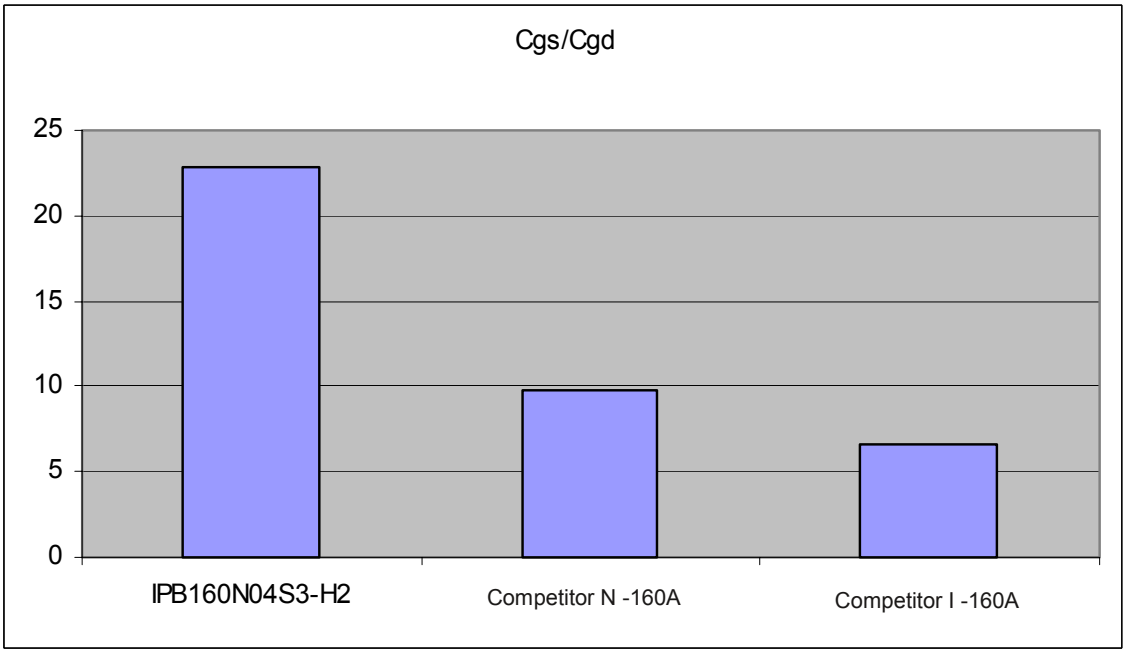

Figure 5 C_{GS}/C_{GD} ratio for state of the art high current MOSFETs

4 Conclusion

This Application Note presented an overview of the mechanism behind the parasitic turn-on of the power MOSFET and gave guidance on how to choose the proper MOSFET in order to avoid this unwanted and dangerous effect.

Edition 2008-12-29

Published by Infineon Technologies AG,
Am Campeon 1-12,
85579 Neubiberg, Germany

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