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(54) **OPTIMIZATION OF COPPER PLATING THROUGH WAFER VIA**

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H01L 21/768 (2006.01)
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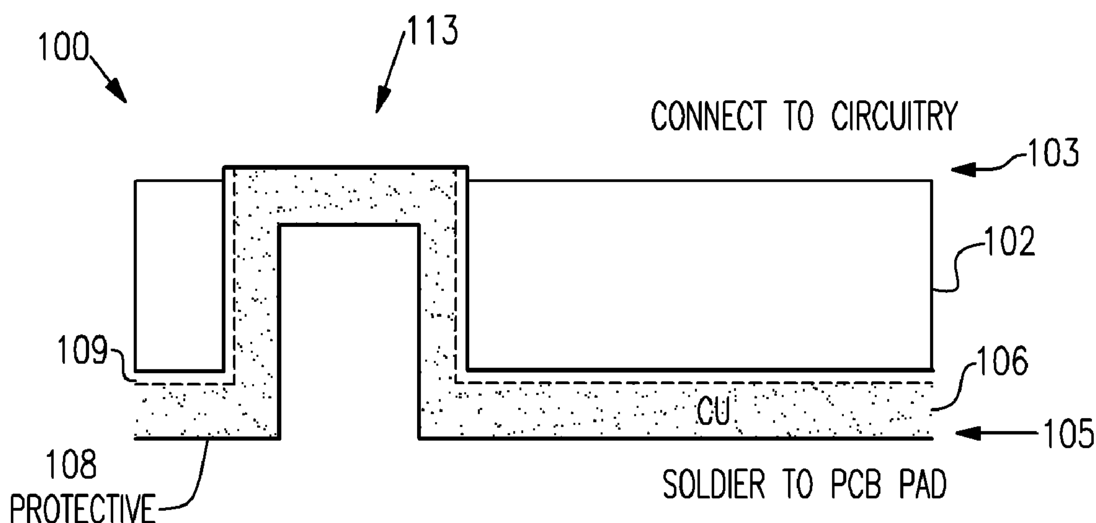
(52) **U.S. Cl.**
USPC **257/751**; 438/758; 257/741; 438/667; 257/E21.002; 257/E23.01; 257/E21.586; 257/E23.011

(57) **ABSTRACT**

Systems, apparatuses, and methods related to the design, fabrication, and manufacture of gallium arsenide (GaAs) integrated circuits are disclosed. Copper can be used as the contact material for a GaAs integrated circuit. Metallization of the wafer and through-wafer vias can be achieved through copper plating processes disclosed herein. To improve the copper plating, a seed layer formed in the through-wafer vias can be modified to increase water affinity, rinsed to remove contaminants, and activated to facilitate copper deposition. GaAs integrated circuits can be singulated, packaged, and incorporated into various electronic devices.



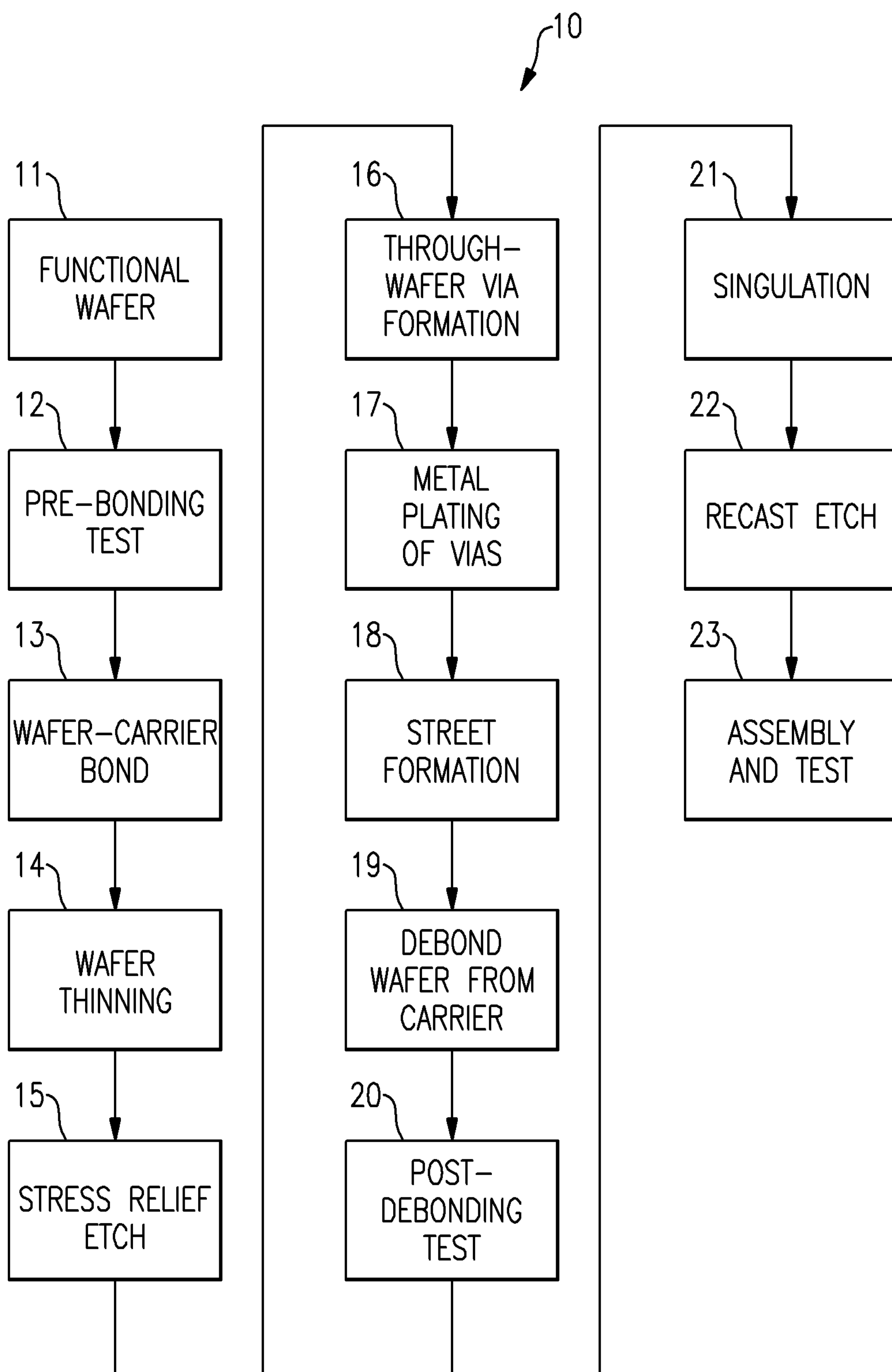


FIG.1

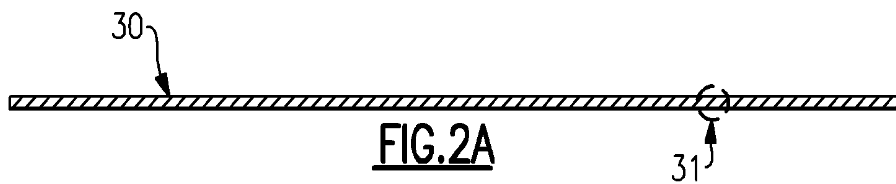


FIG.2A

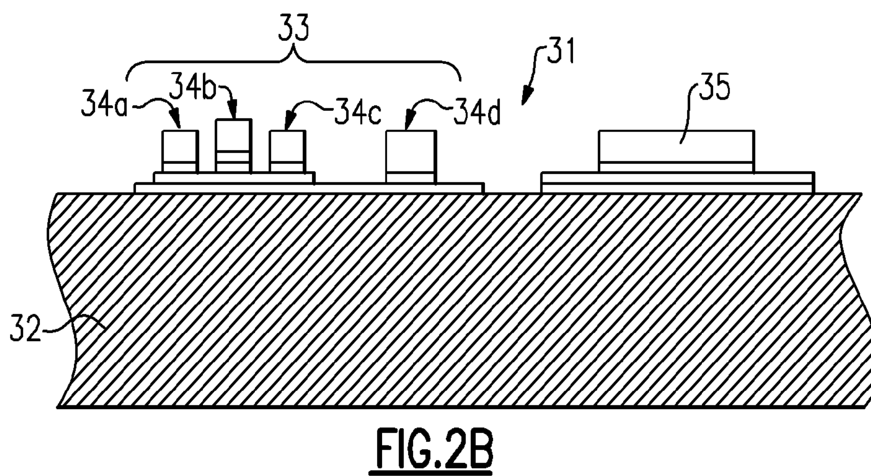


FIG.2B

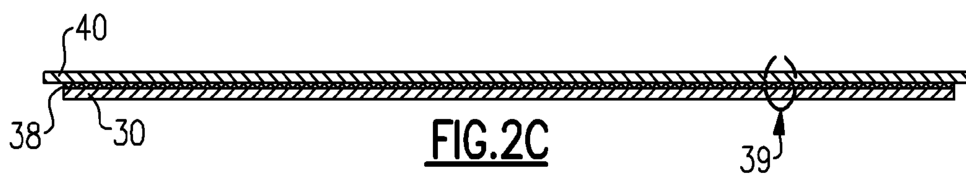


FIG.2C

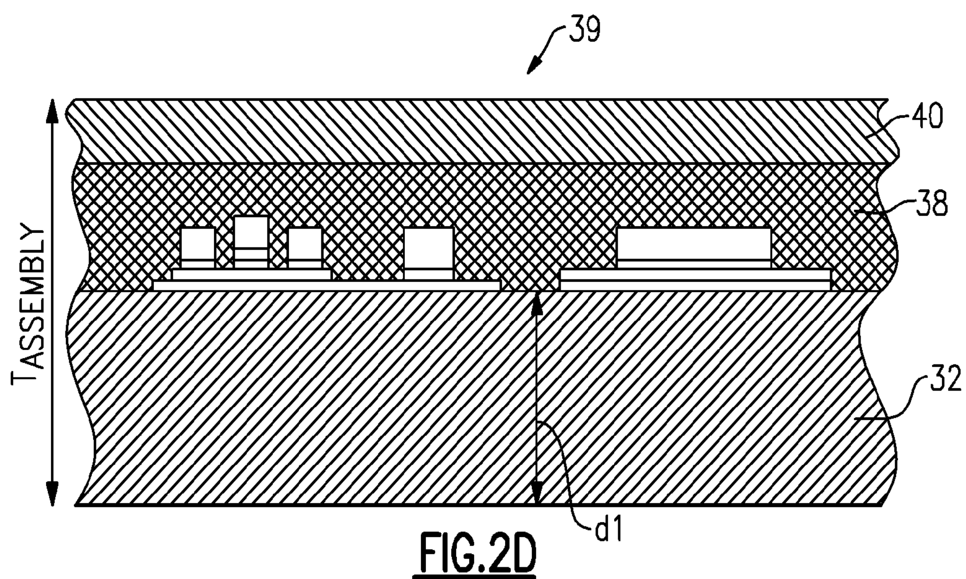


FIG.2D

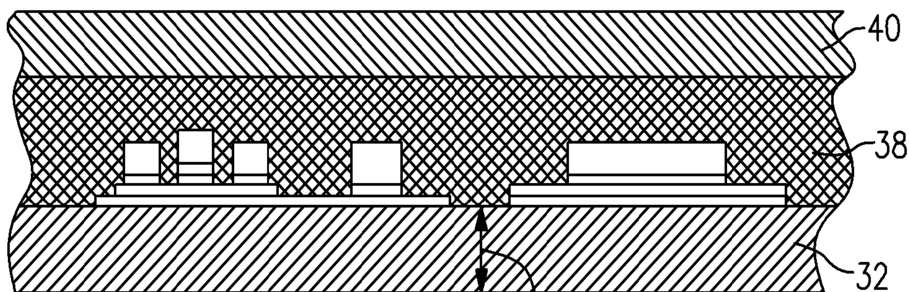


FIG.2E

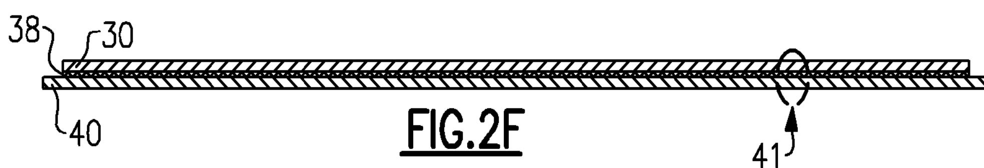


FIG.2F

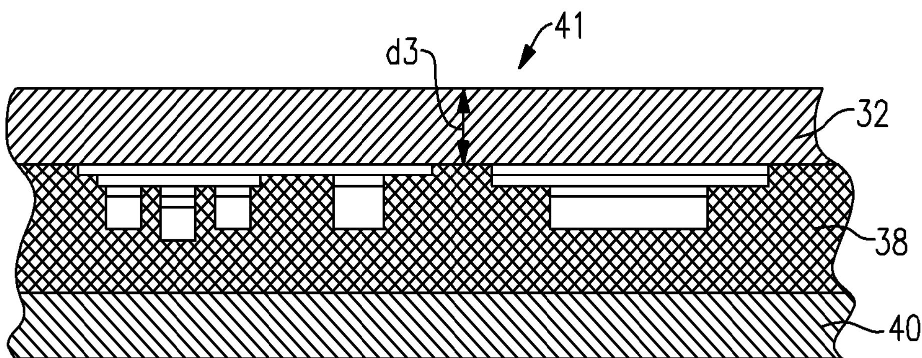


FIG.2G

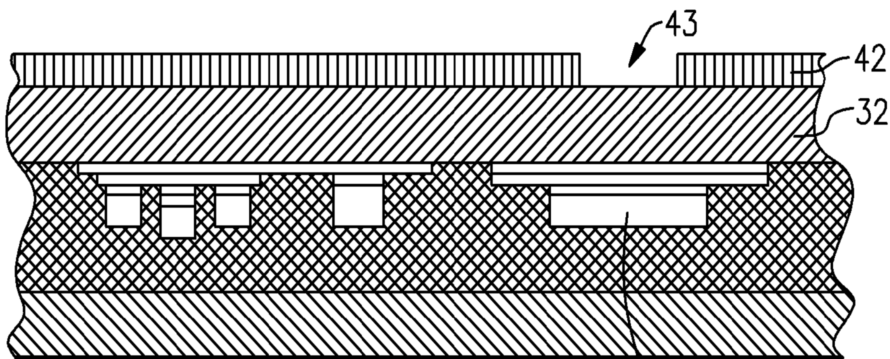


FIG.2H

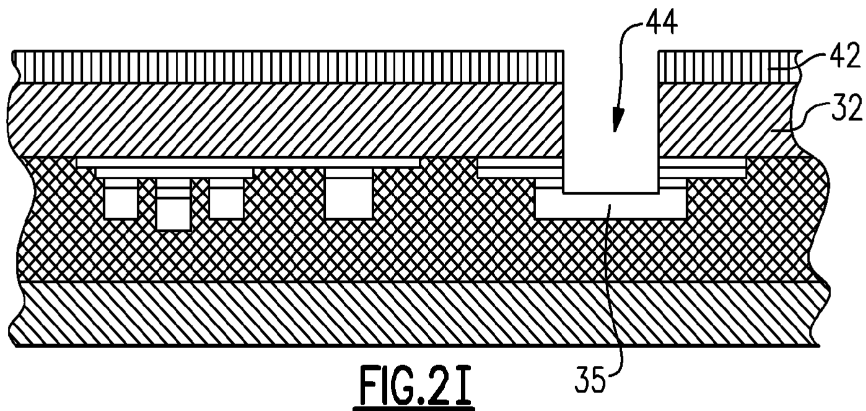


FIG.2I

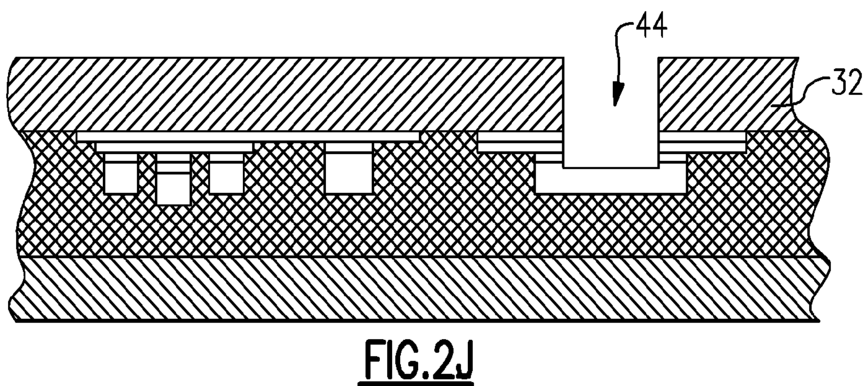


FIG.2J

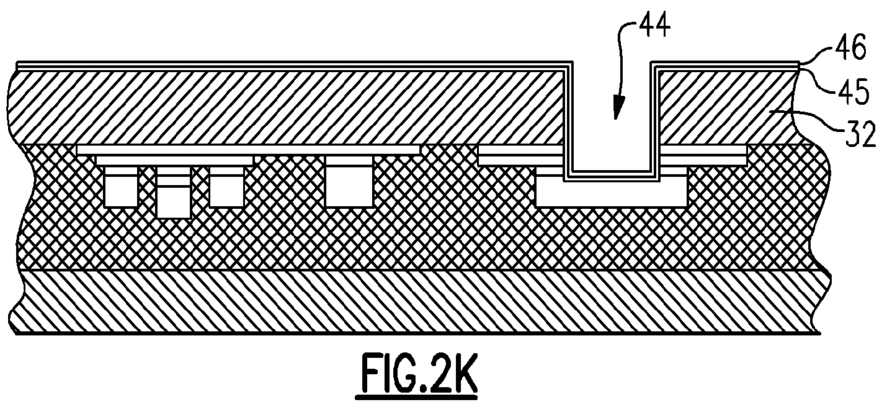


FIG.2K

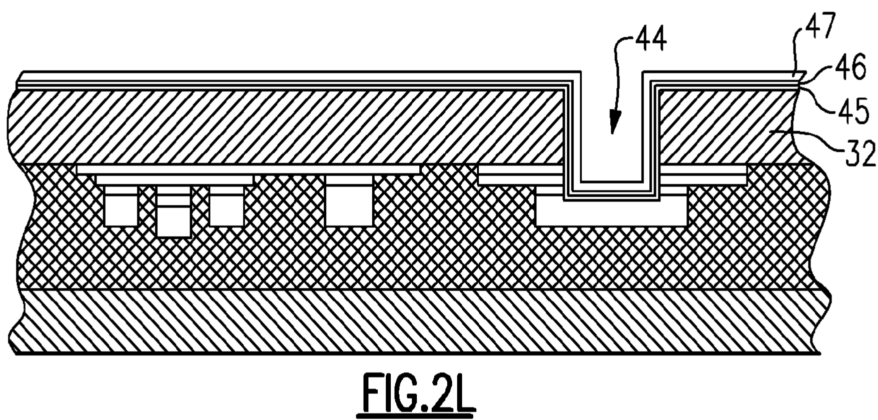


FIG.2L

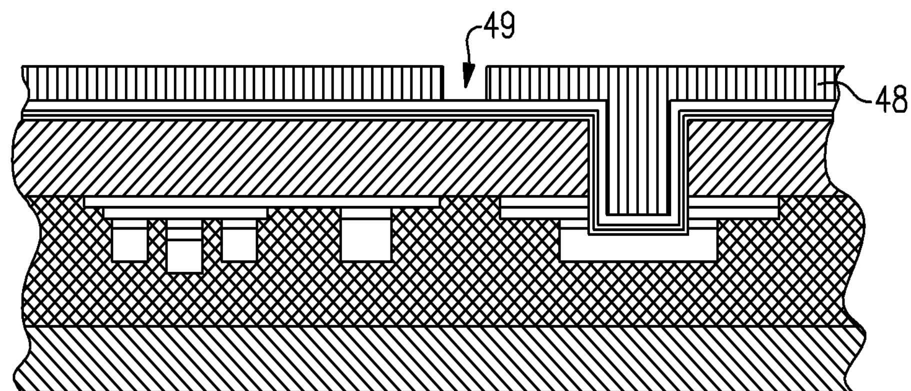


FIG.2M

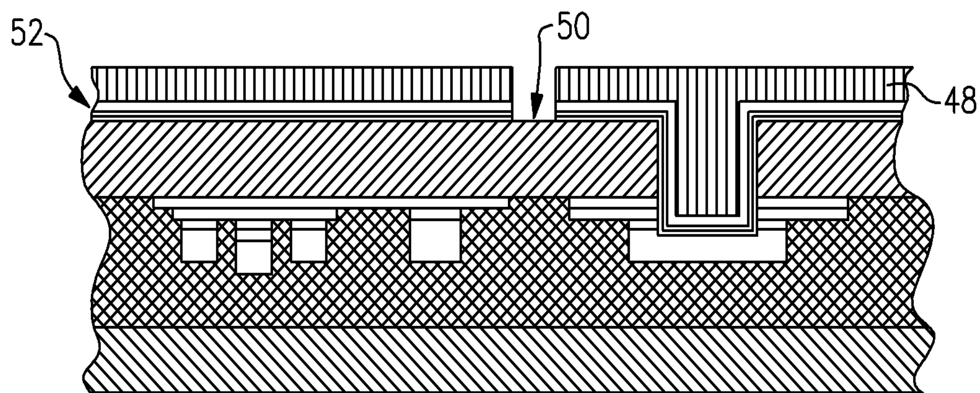


FIG.2N

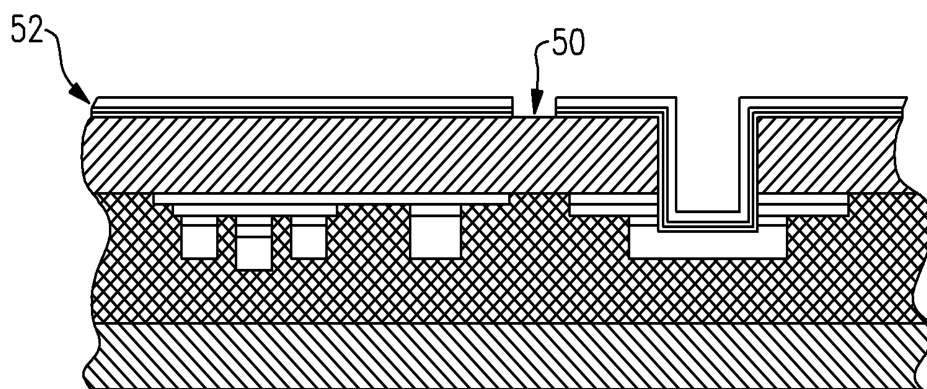


FIG.2O

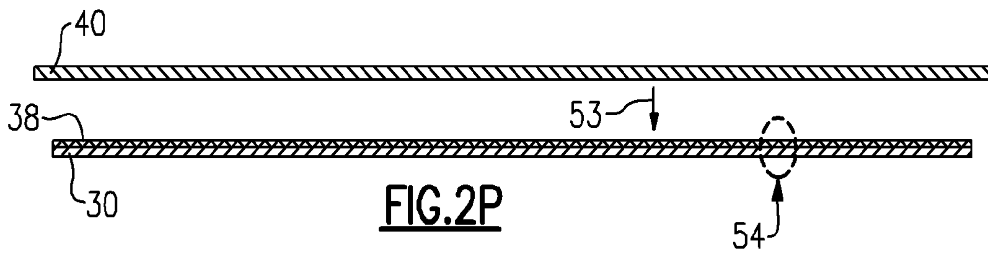


FIG.2P

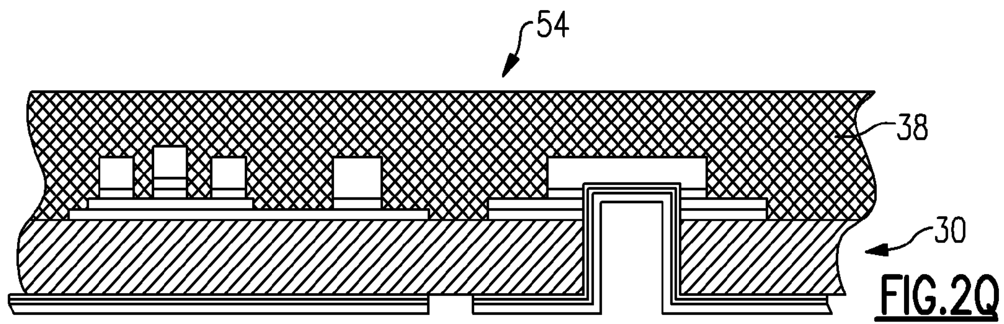


FIG.2Q

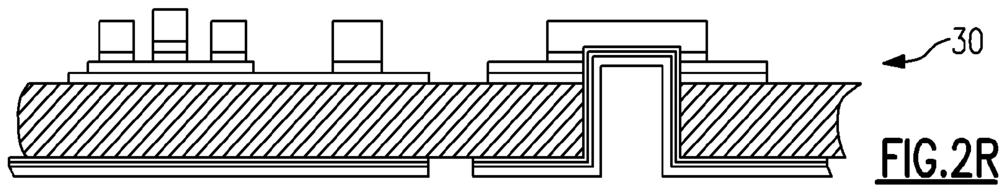


FIG.2R

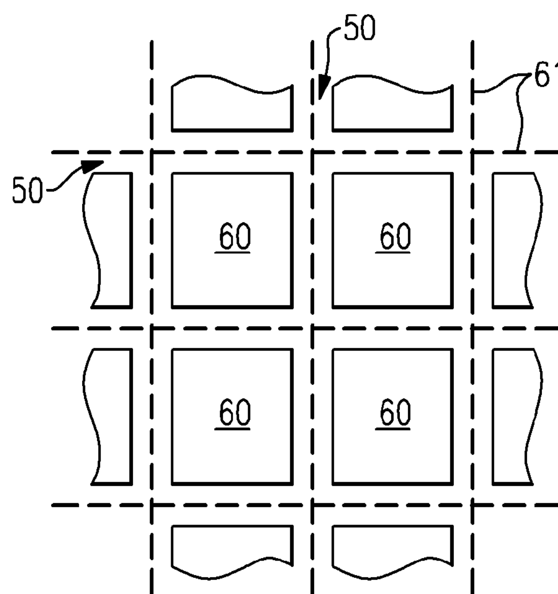


FIG.2S

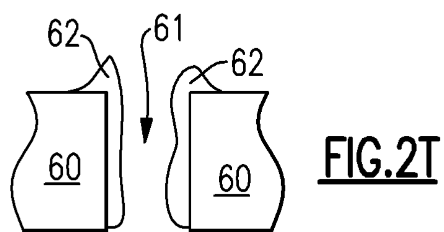


FIG.2T

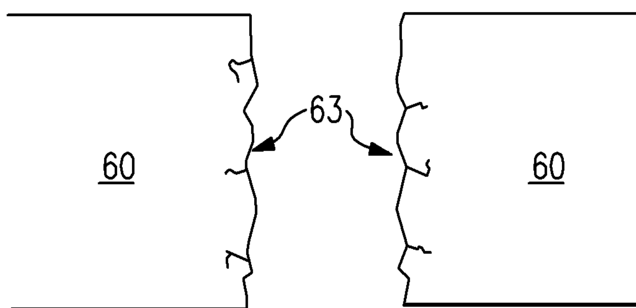


FIG.2U

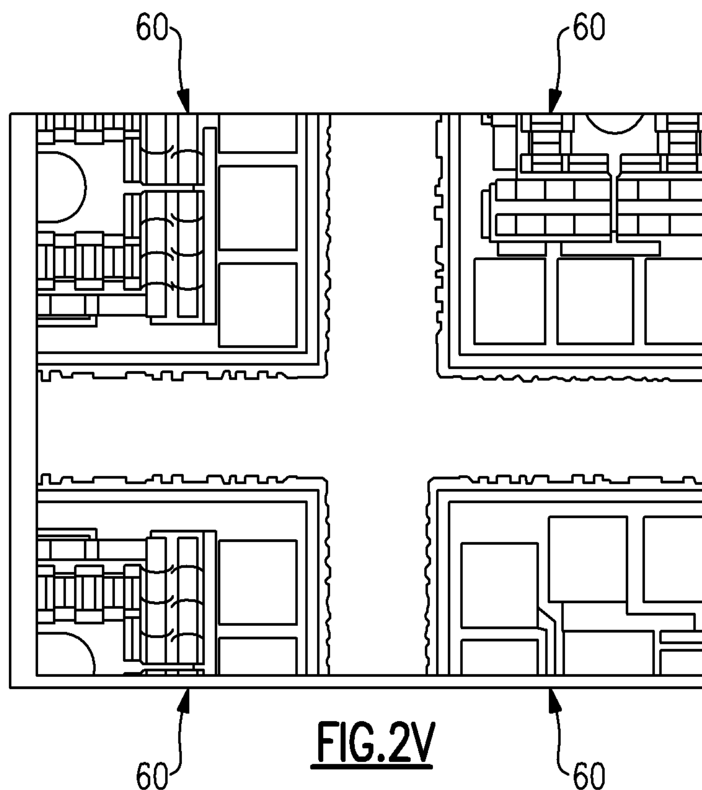


FIG.2V

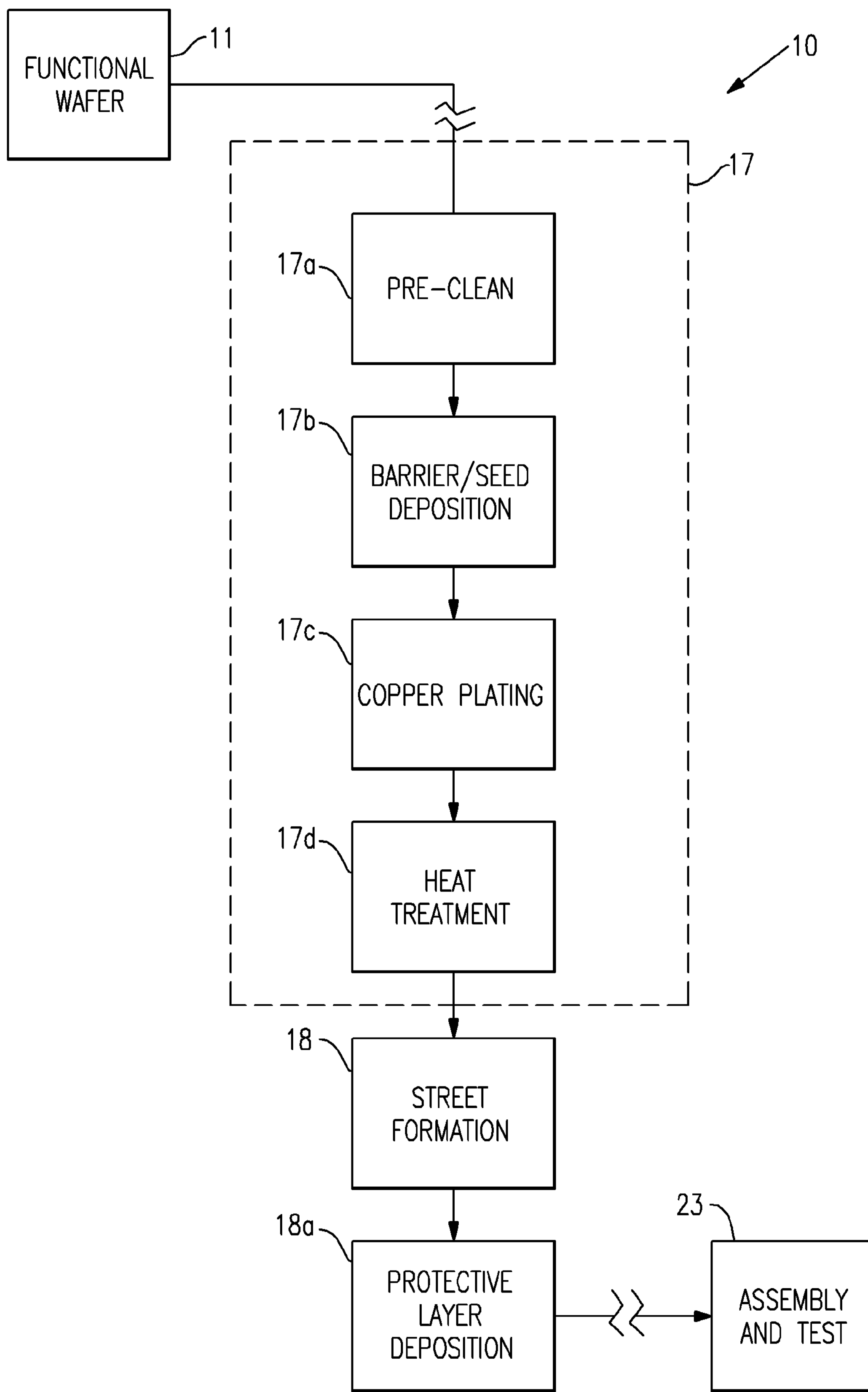


FIG.3

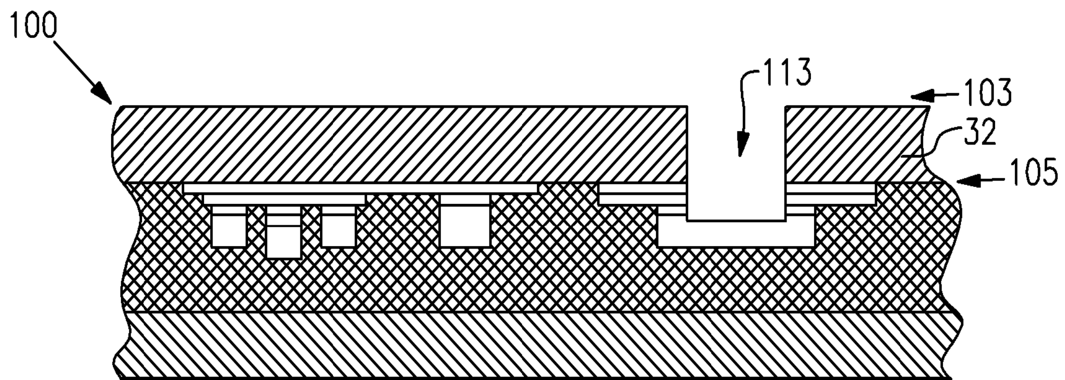


FIG.4A

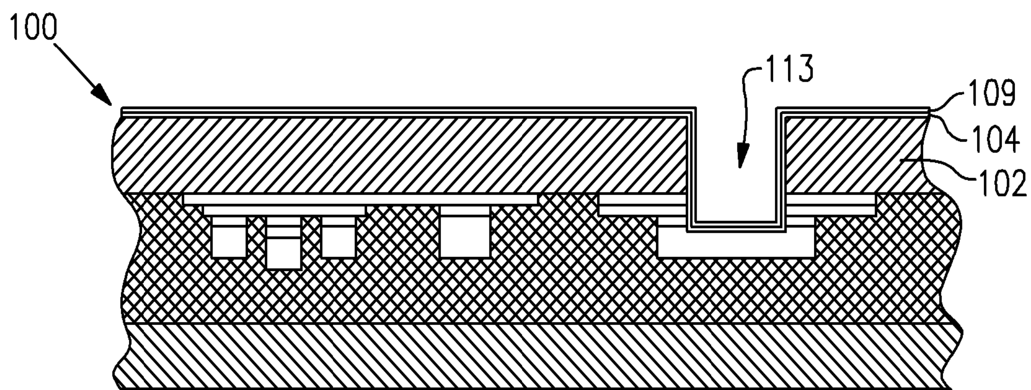


FIG.4B

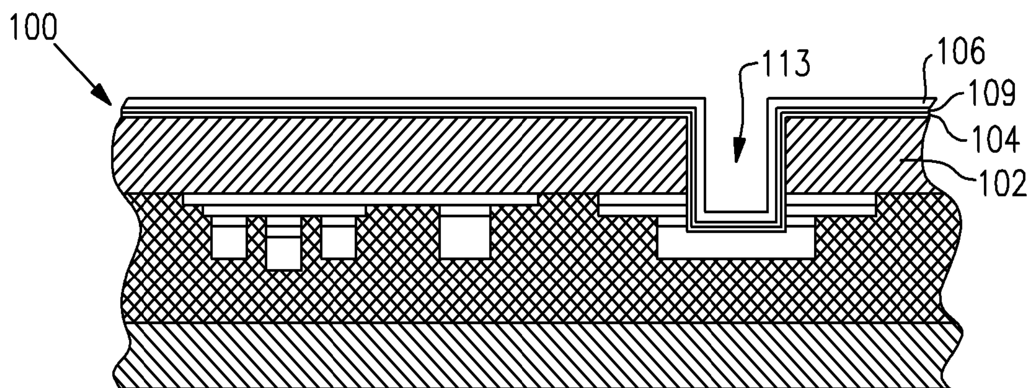


FIG.4C

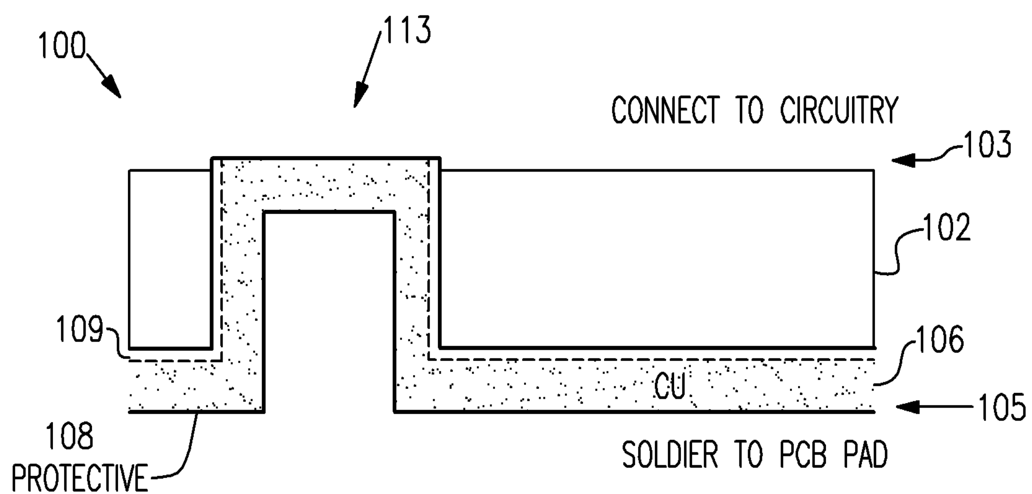


FIG.4D

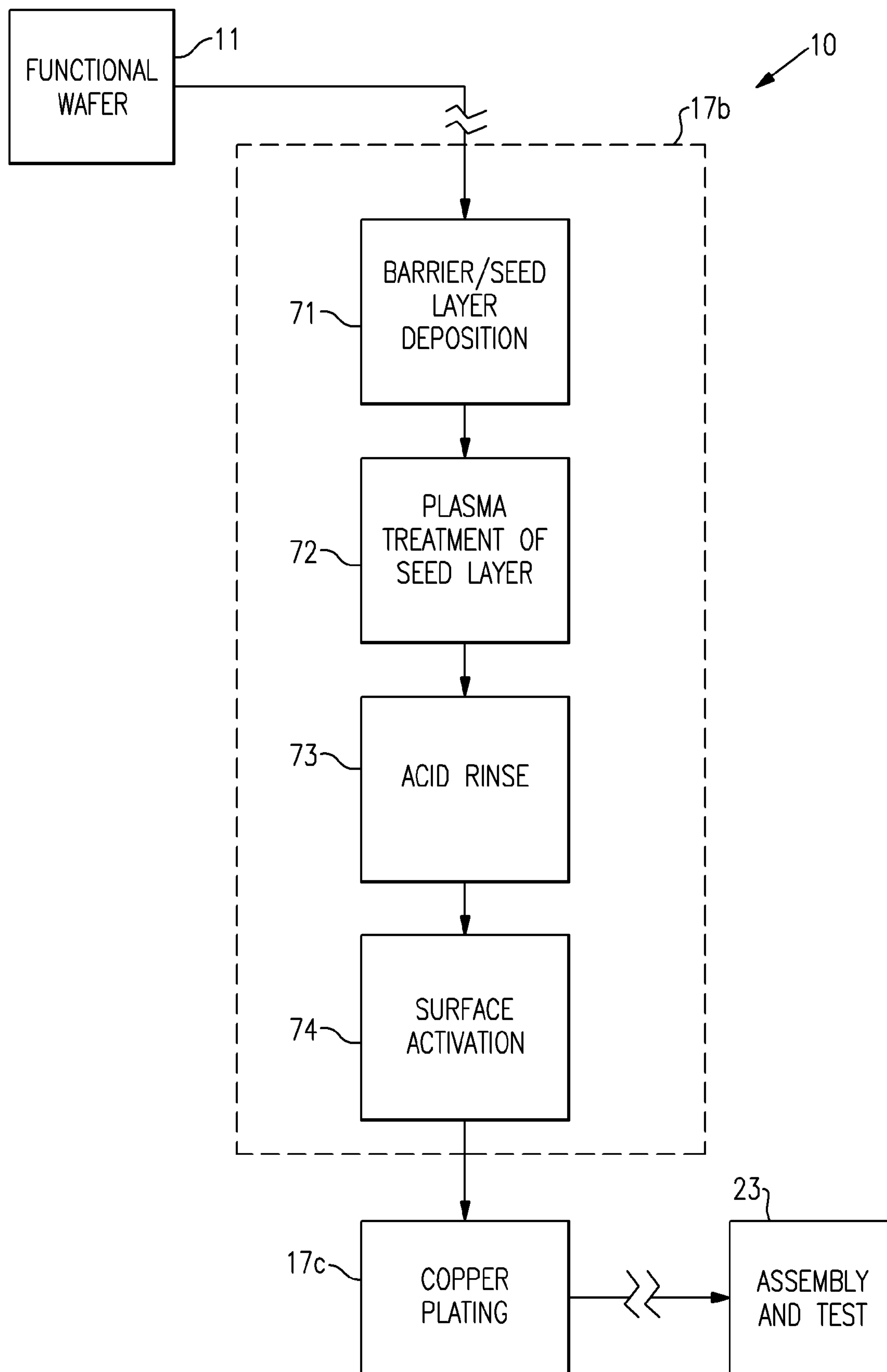


FIG.5

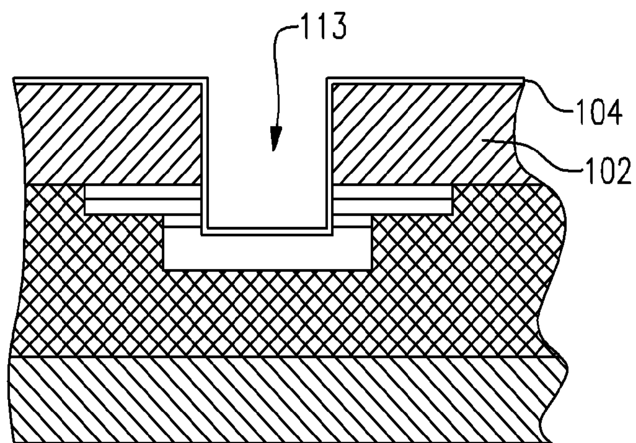


FIG.6A

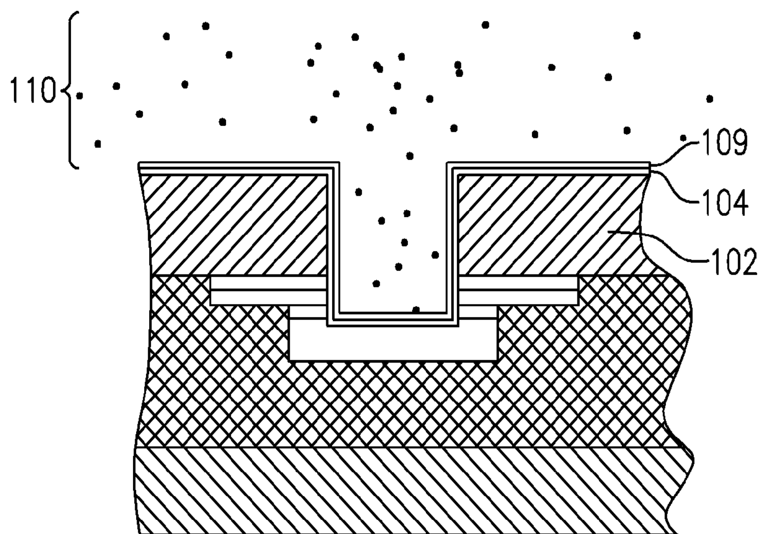


FIG.6B

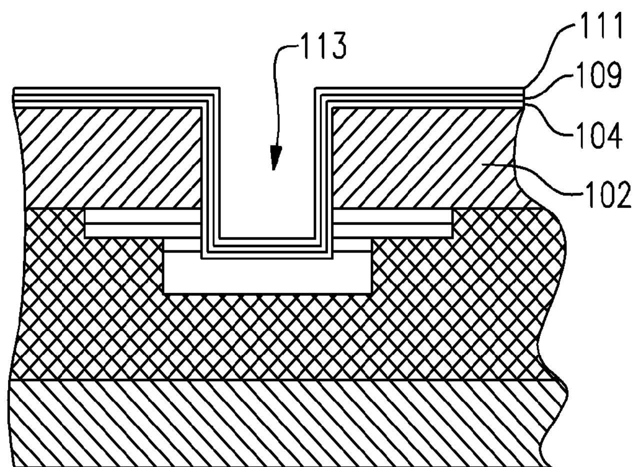


FIG.6C

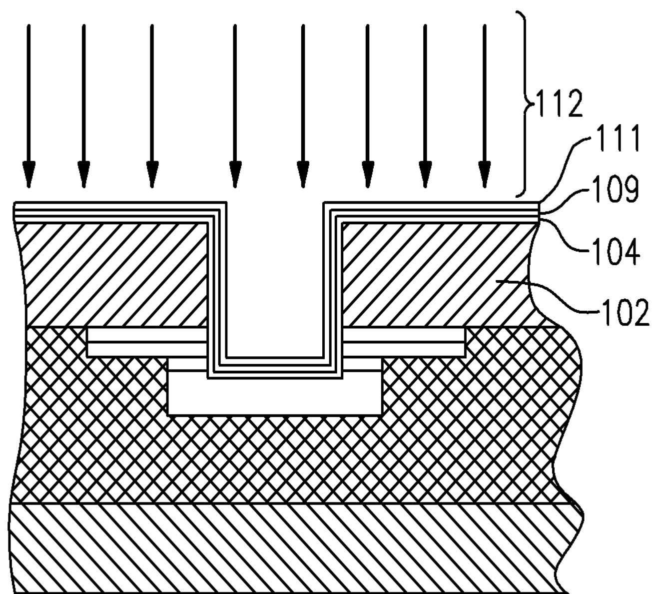


FIG.6D

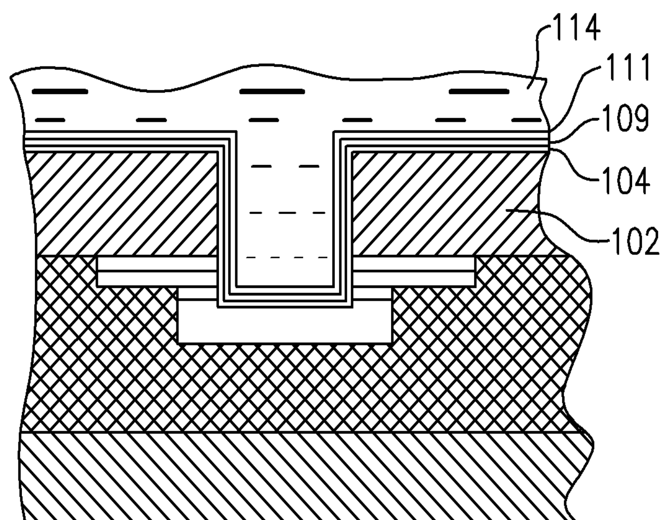


FIG.6E

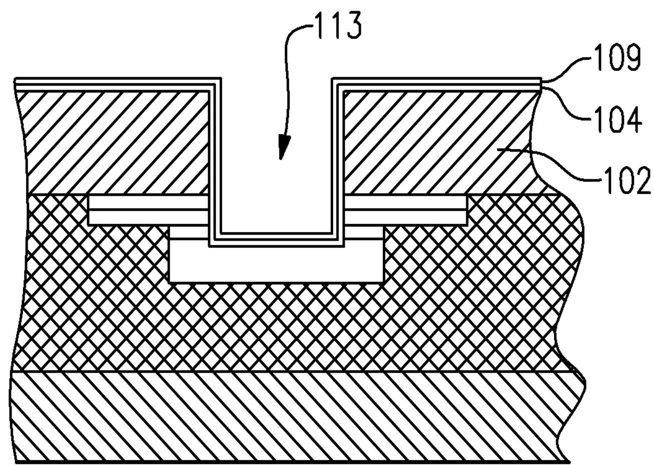


FIG.6F

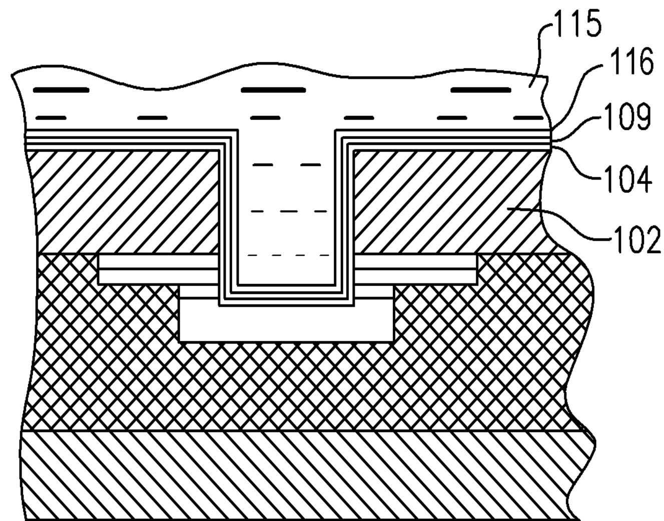


FIG.6G

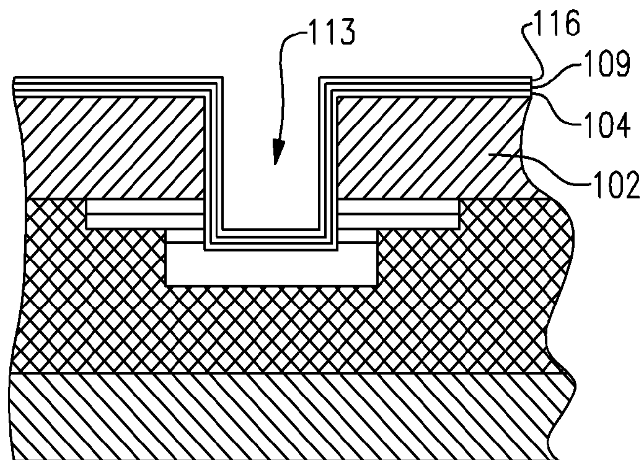


FIG.6H

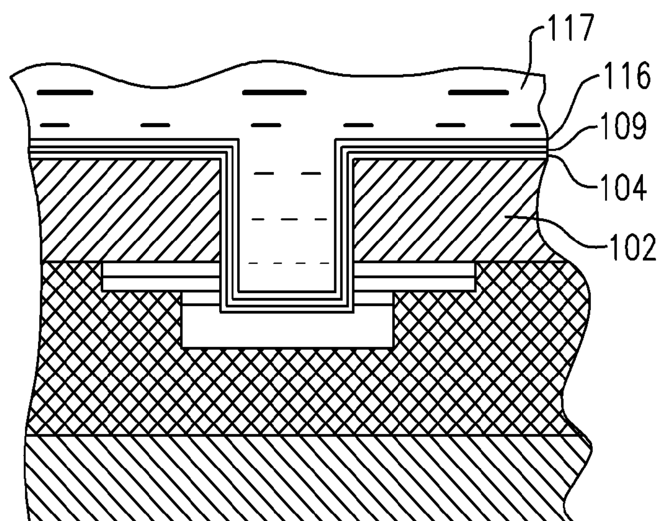


FIG.6I

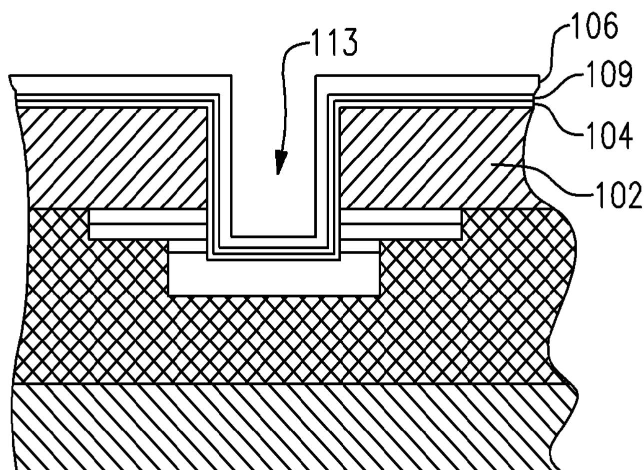


FIG.6J

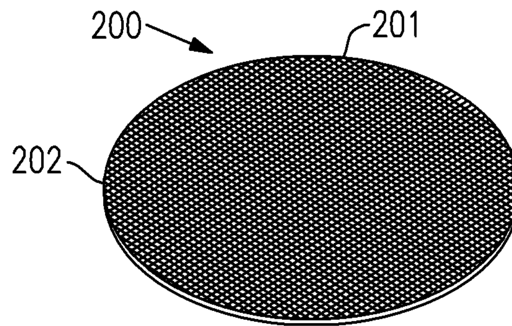


FIG.7A

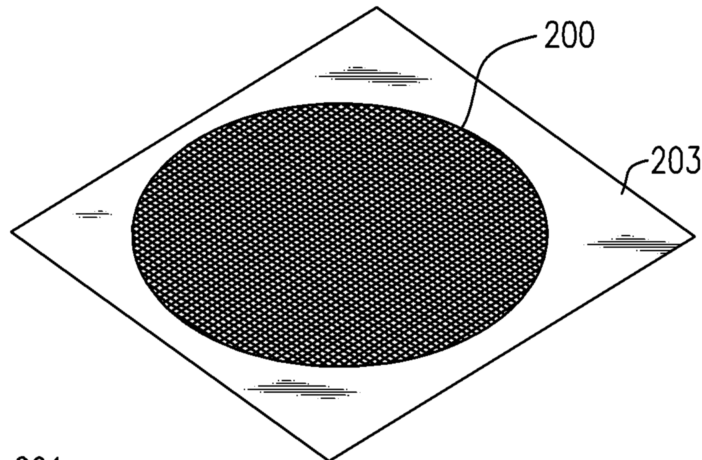


FIG.7B

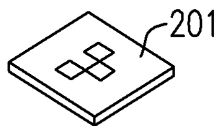


FIG.7D

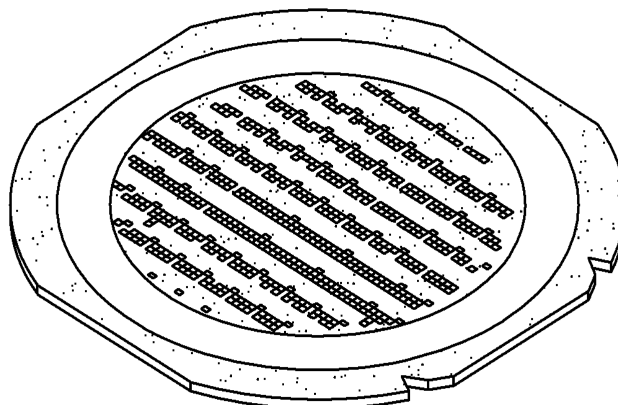


FIG.7C

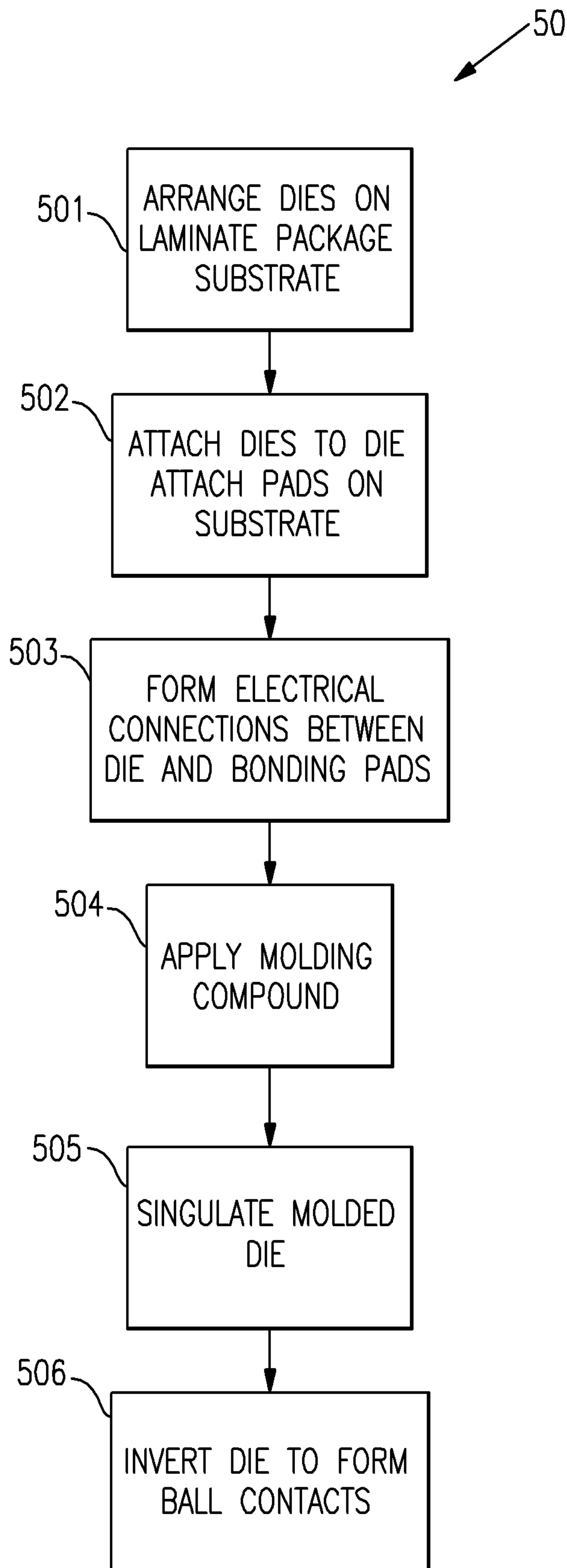


FIG.8

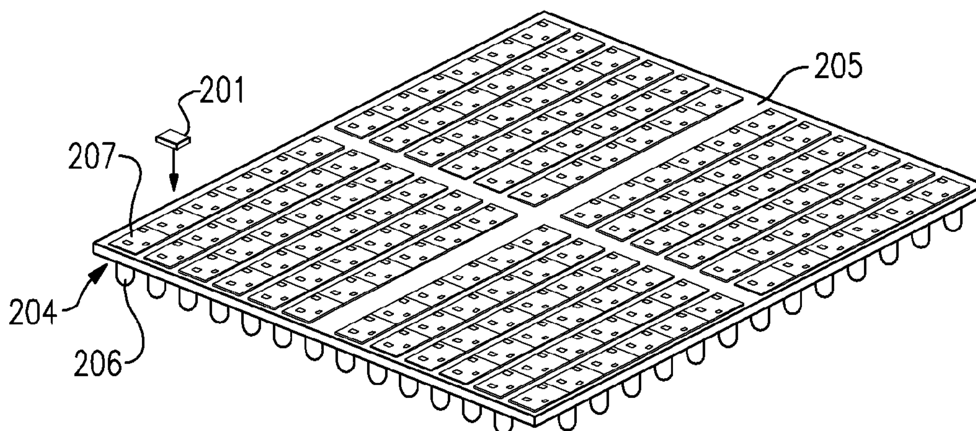


FIG.9A

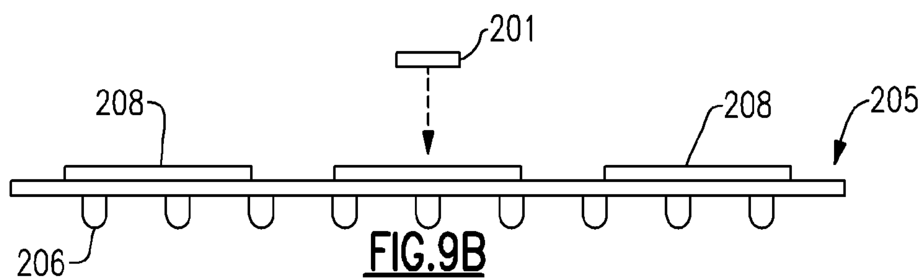


FIG.9B

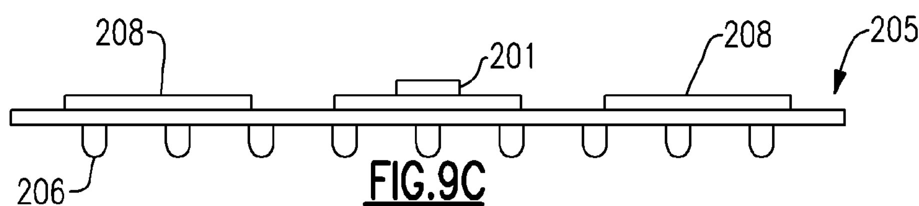


FIG.9C

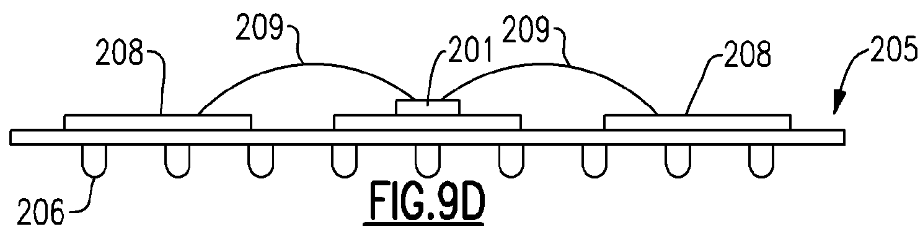


FIG.9D

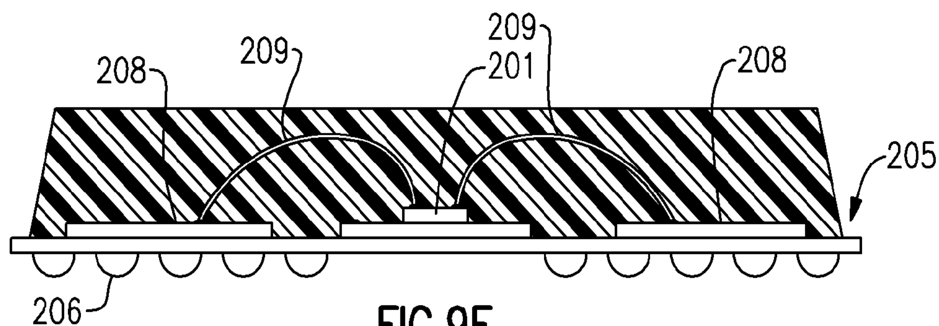


FIG.9E

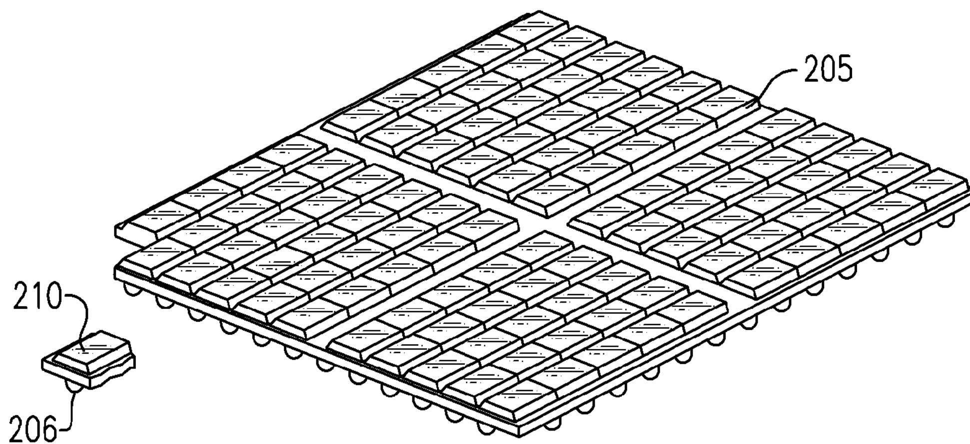


FIG.9F

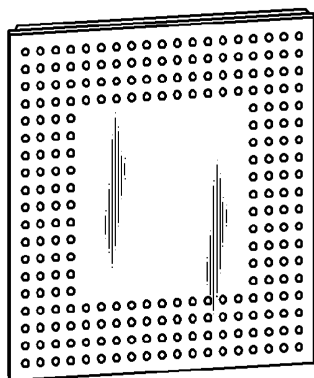


FIG.9G

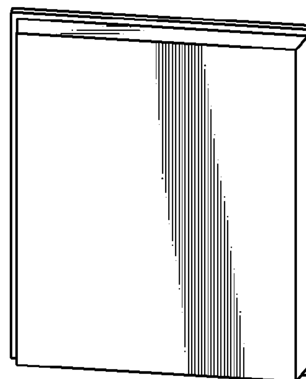


FIG.9H

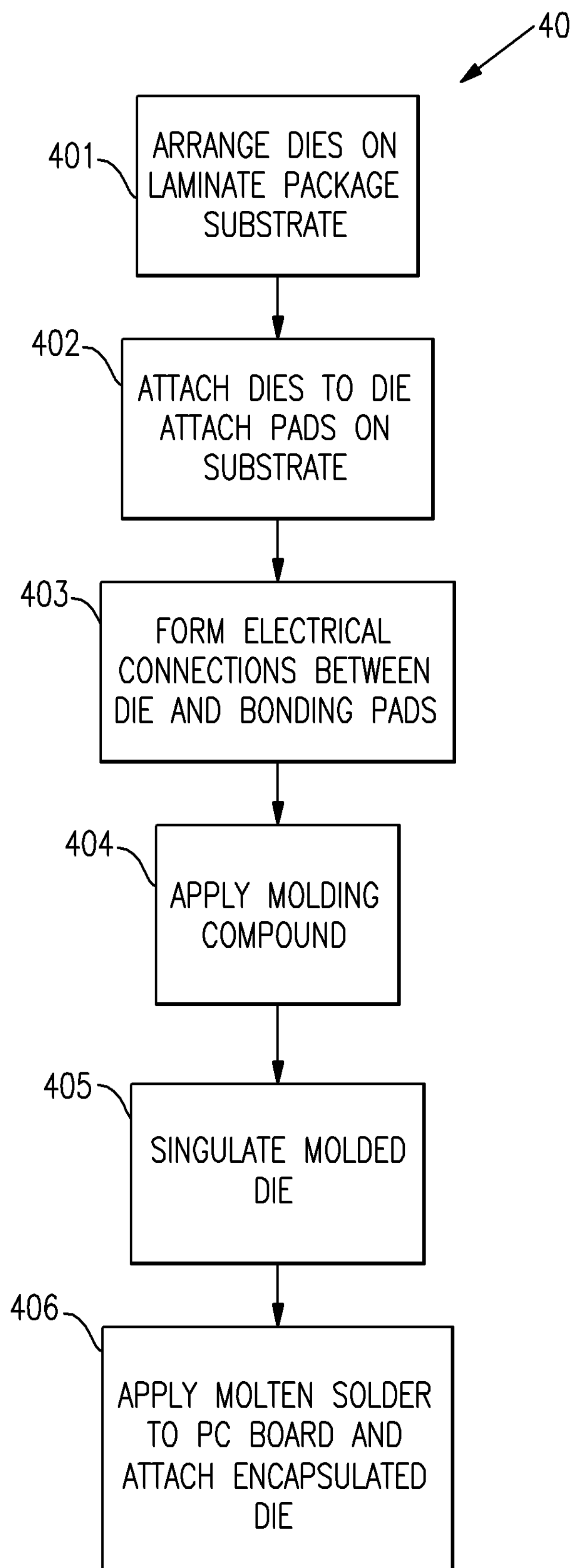


FIG.10

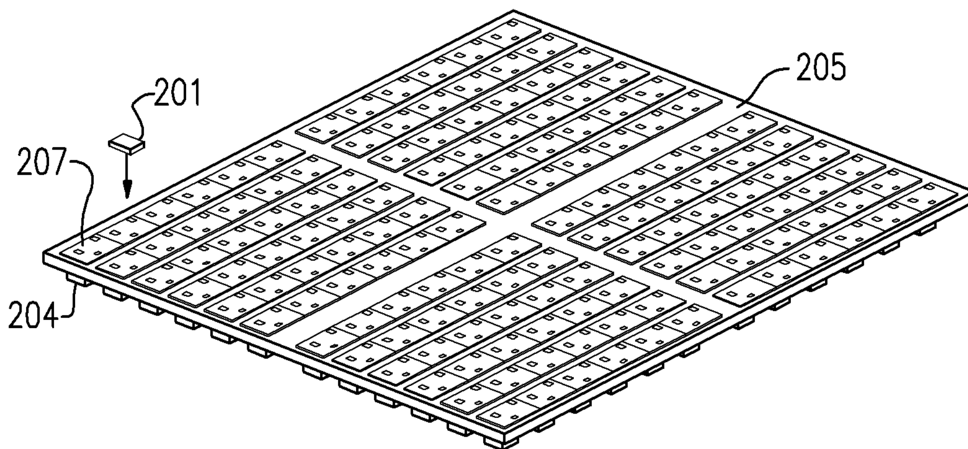


FIG.11A

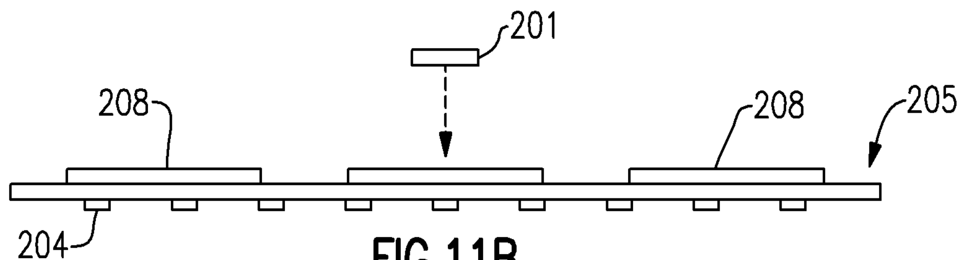


FIG.11B

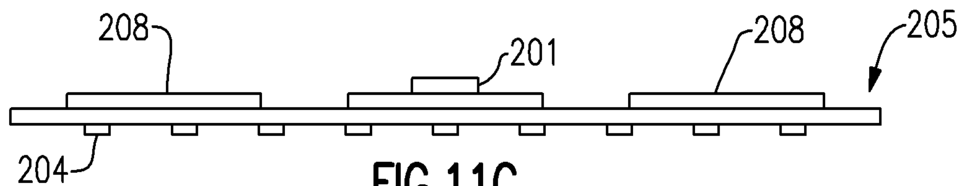


FIG.11C

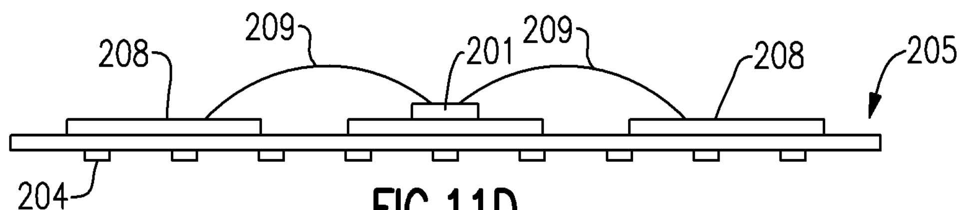


FIG.11D

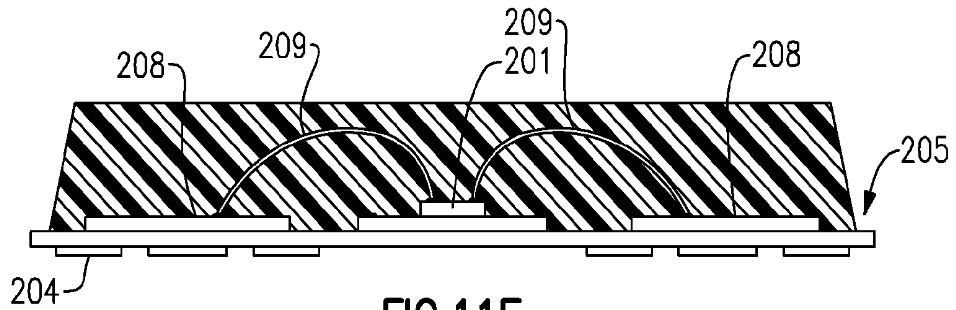


FIG.11E

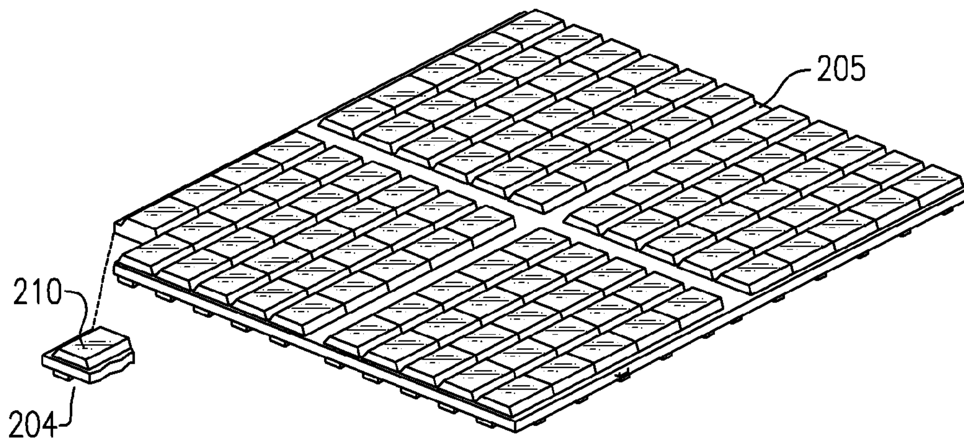


FIG.11F

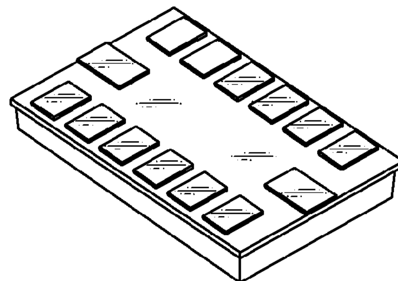


FIG.11G

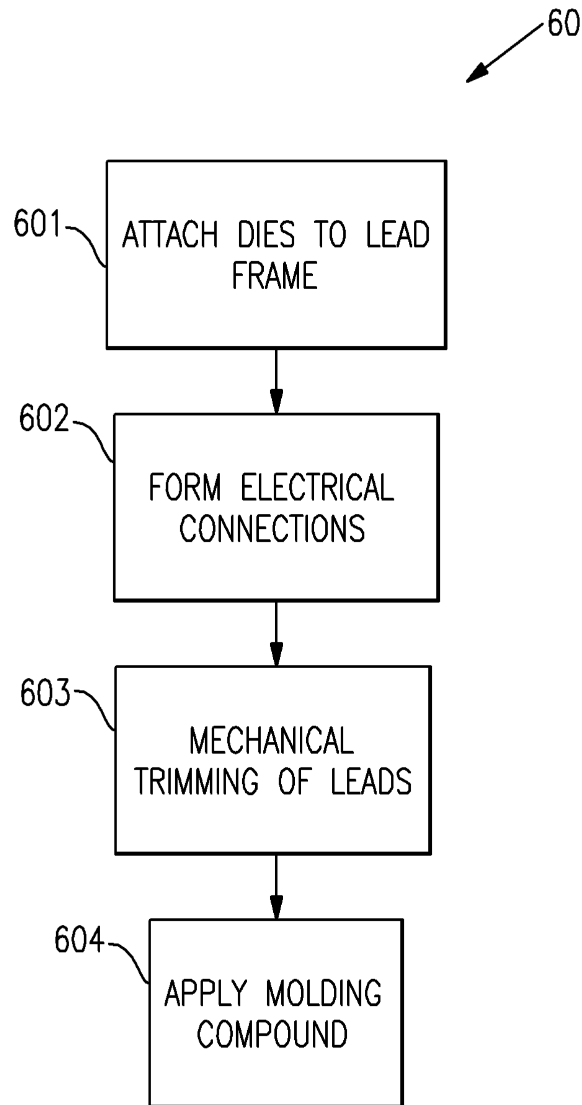


FIG.12

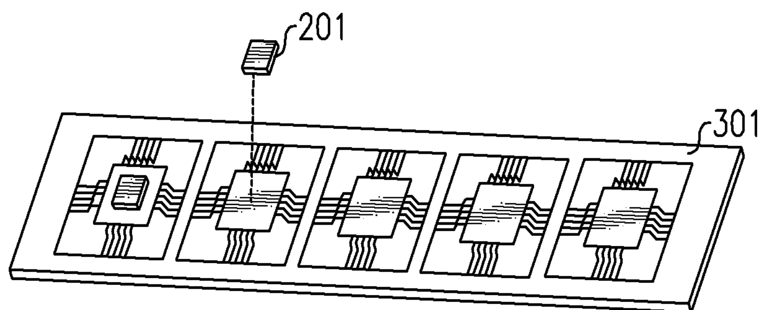


FIG.13A

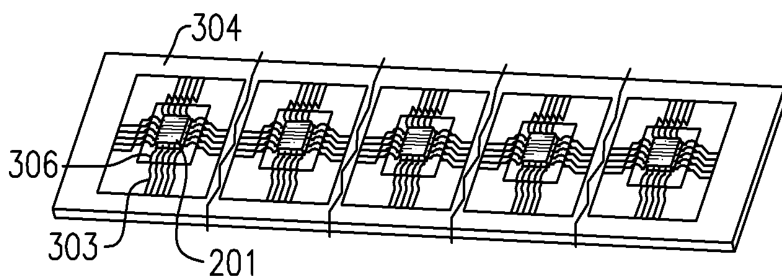


FIG.13B

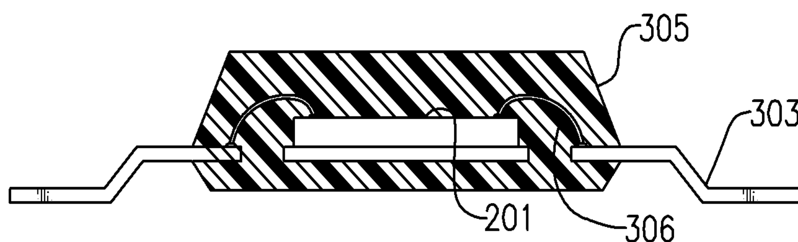


FIG.13C

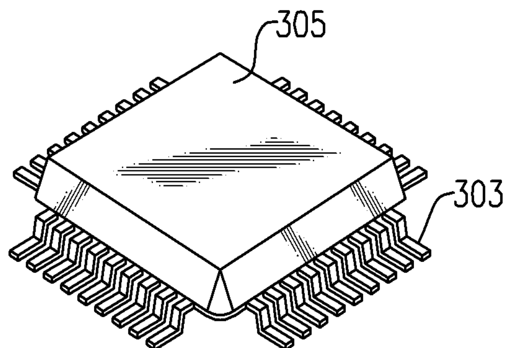


FIG.13D

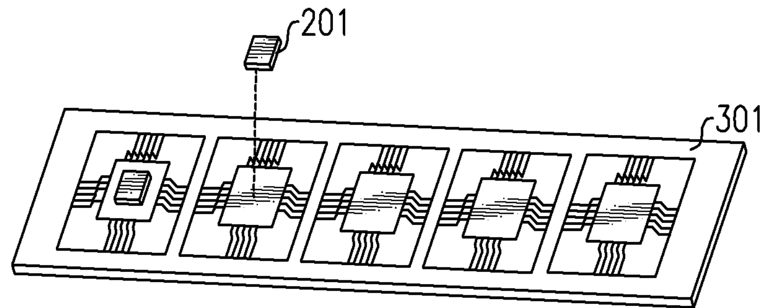


FIG.14A

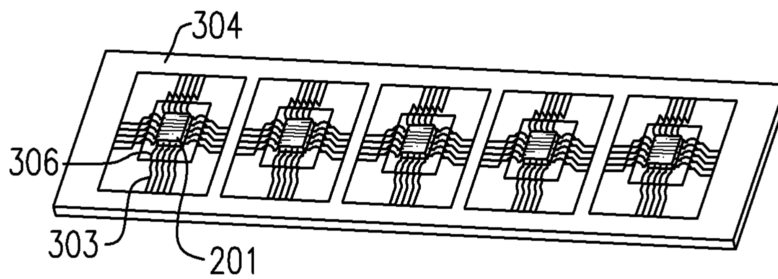


FIG.14B

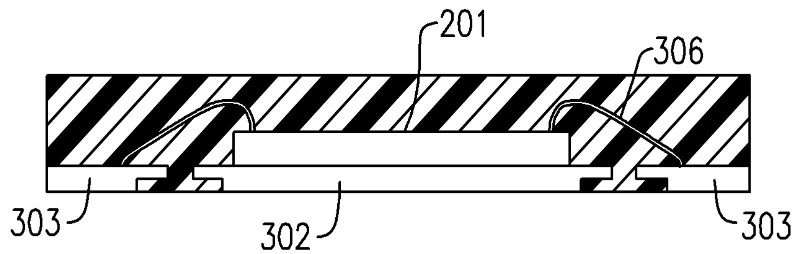


FIG.14C

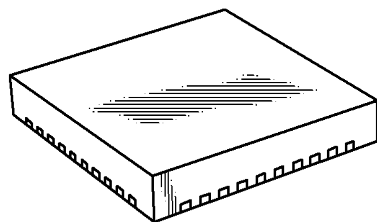


FIG.14D

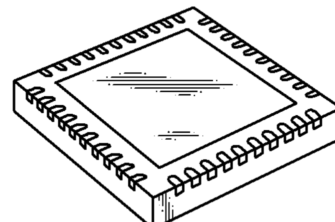


FIG.14E

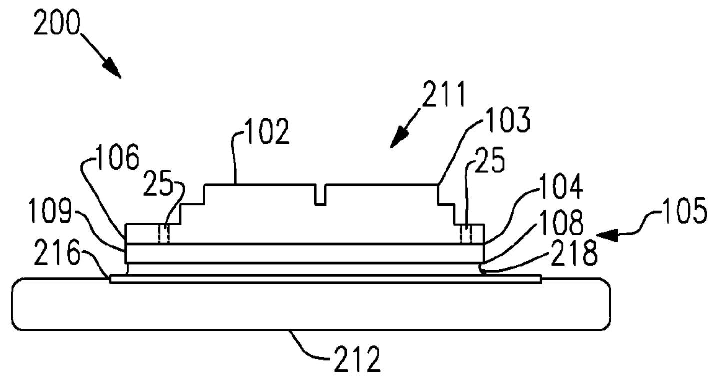


FIG.15

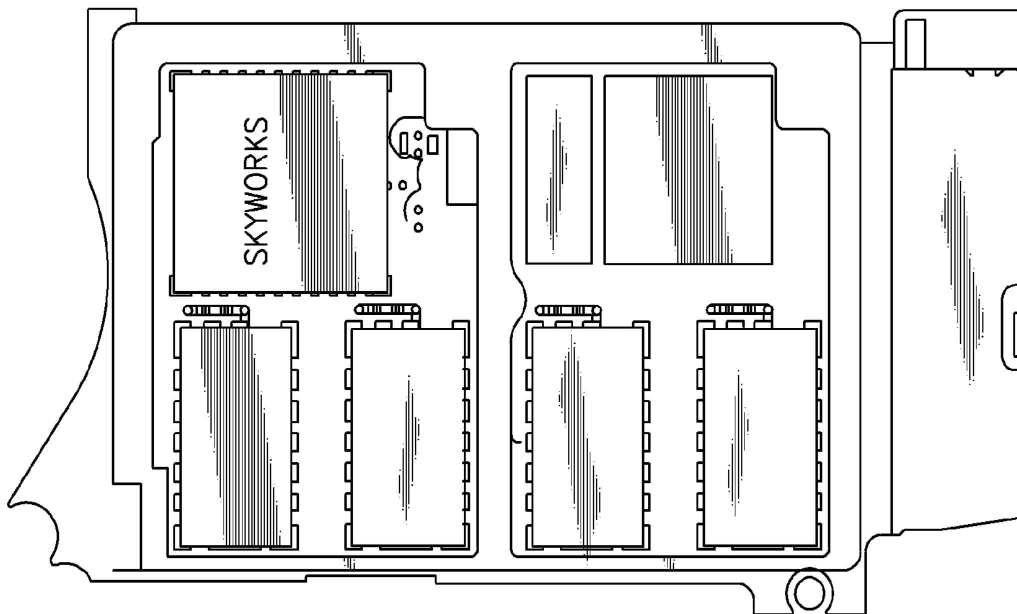


FIG.16

OPTIMIZATION OF COPPER PLATING THROUGH WAFER VIA

BACKGROUND OF THE INVENTION

[0001] 1. Field of the Invention

[0002] The present disclosure generally relates to the field of semiconductor wafer processing technology. In particular, this disclosure relates to the design, fabrication, and manufacture of gallium arsenide (GaAs) integrated circuits.

[0003] 2. Description of the Related Art

[0004] The use of GaAs substrates in the design and construction of integrated circuits has proven to have desirable effects. For example, GaAs substrates have been useful in achieving greater performance in power amplifier circuits. Typically, a GaAs integrated circuit will be used as a component in a larger circuit device or design. In order to be integrated into the circuit design, the GaAs integrated circuit is mechanically and electrically coupled to a printed circuit board for the circuit device. In other cases, the GaAs integrated device is mounted to other electronic devices.

[0005] The contact side of the GaAs integrated circuit is typically adhered to a contact pad on the device's printed circuit board. More particularly, the integrated circuit usually includes a gold layer which adheres to the printed circuit board pad using a conductive adhesive. Often, the GaAs substrate has vias which extend into or through the substrate for facilitating electrical flow vertically through the substrate. These vias are also coated with the gold conductive material. Depositing the gold layer is a time-consuming and relatively inefficient process. Also, gold is an expensive material, increasing the cost for GaAs integrated circuit products. Finally, gold has a relatively high dissolution rate in solder, and therefore is not able to be soldered to the pad of the device's printed circuit board. Instead, conductive adhesive is typically used to adhere the gold contact to the printed circuit board. The use of conductive adhesive requires an additional manufacturing step, and also requires the use of larger pads to accommodate adhesive overflow. However, even with these undesirable features, gold continues to be the standard metal used for a contact layer on GaAs integrated circuits, which significantly drives up the product cost especially in recent years due to the high price of gold.

[0006] Accordingly, there is a need for improved GaAs integrated circuits that employ less costly component materials and can be more efficiently manufactured. Furthermore, there is a need for improved processes and methods for manufacturing such GaAs integrated circuits.

SUMMARY OF THE INVENTION

[0007] Methods for surface treating a through wafer via in GaAs integrated circuits are disclosed. A seed layer is formed in the through wafer via. The surface of the seed layer is modified to increase the water affinity of the surface. The surface is rinsed to remove contaminants, followed by activation of the surface to facilitate copper deposition. According to various embodiments, the seed layer can be gold, copper, or palladium. In certain embodiments, modifying the surface of the seed layer includes treating the surface with plasma. In some embodiments, an oxygen plasma is used to modify the surface of the seed layer.

[0008] In one embodiment, a method for surface treatment of through wafer vias in GaAs integrated circuits prior to copper metallization is provided. The method includes modifying a surface of a seed layer formed in the through wafer vias to increase the water affinity of the surface; rinsing the surface to remove contaminants from the surface; and activating the surface to facilitate copper deposition onto said surface. In some implementations, the seed layer can be copper, gold and/or palladium. In some other implementations, the surface of the seed layer is modified using plasma, preferably oxygen plasma. In some other implementations, the surface is rinsed with dilute hydrochloric acid. In yet some other implementations, the surface is activated by depositing a monolayer of accelerator molecules, such as bis(sodium-sulfopropyl)disulfide (SPS), over the surface. Preferably, the GaAs integrated circuit formed using the above described methods includes a copper filled through wafer via and/or a copper contact pad, and can be incorporated in wireless telecommunication devices.

[0009] In another embodiment, a method for metalizing a through wafer via in GaAs integrated circuits is provided. The method includes pre-cleaning the through wafer via; depositing a barrier layer on a surface in the through wafer via; depositing a seed layer on the barrier layer; treating the seed and barrier layers with plasma; rinsing the seed and barrier layers with an acid; activating the seed and barrier layers; and depositing copper in the through wafer via. In some implementation, the seed and barrier layers are coated with a monolayer of accelerator molecules. In some other implementation, the seed and barrier layers are rinsed with an accelerator such that the accelerator is not removed from the seed and barrier layers before depositing copper in the through wafer via. Preferably, the GaAs integrated circuit formed using the above described methods includes a copper filed through wafer via and/or a copper contact pad, and can be incorporated in wireless telecommunication devices.

[0010] For purposes of summarizing the disclosure, certain aspects, advantages and novel features of the inventions have been described herein. It is to be understood that not necessarily all such advantages may be achieved in accordance with any particular embodiment of the invention. Thus, the invention may be embodied or carried out in a manner that achieves or optimizes one advantage or group of advantages as taught herein without necessarily achieving other advantages as may be taught or suggested herein.

BRIEF DESCRIPTION OF THE DRAWINGS

[0011] FIG. **1** shows an example sequence of wafer processing for forming through-wafer features such as vias.

[0012] FIGS. **2**A-**2**V show examples of structures at various stages of the processing sequence of FIG. **1**.

[0013] FIG. **3** is a block diagram representing the via metallization process according to various aspects of the present invention.

[0014] FIGS. **4**A-**4**D show examples of structures cross sectional diagram of a via section of a GaAs integrated circuit device in accordance with the present invention.

[0015] FIG. **5** is a block diagram representing the barrier/seed deposition process according to various aspects of the present invention.

[0016] FIG. **6**A-**6**J show examples of structures at various stages of the processing sequence of FIG. **5**.

[0017] FIGS. **7**A-**7**D show an example sequence of singulating a GaAs integrated circuit die from a wafer.

[0018] FIG. **8** shows an example shows an example sequence of ball grid array packaging of singulated GaAs integrated circuit dies, according to one embodiment.

[0019] FIGS. 9A-9H show examples of structures at various stages of the processing sequence of FIG. 8.
[0020] FIG. 10 shows an example shows an example sequence of land grid array packaging of singulated GaAs integrated circuit dies, according to one embodiment.
[0021] FIGS. 11A-11G show examples of structures at various stages of the processing sequence of FIG. 10.
[0022] FIG. 12 shows an example shows an example sequence of leadframe packaging of singulated GaAs integrated circuit dies, according to one embodiment.
[0023] FIGS. 13A-13D show examples of structures at various stages of the processing sequence of FIG. 12, according to one embodiment.
[0024] FIGS. 14A-14E show examples of structures at various stages of the processing sequence of FIG. 12, according to another embodiment.
[0025] FIG. 15 illustrates a GaAs integrated circuit device made according to various methods of the present invention, mounted onto a printed circuit board.
[0026] FIG. 16 illustrates an electronic device incorporating a GaAs integrated circuit device made according to various methods of the present invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

[0027] The headings provided herein, if any, are for convenience only and do not necessarily affect the scope or meaning of the claimed invention.

GaAs Wafer Processing and through via Formation

[0028] Provided herein are various methodologies and devices for processing wafers such as GaAs wafers. FIG. 1 shows an example of a process 10 where a functional GaAs wafer is further processed to form through-wafer features such as vias and back-side metal layers.
[0029] In the description herein, various examples are described in the context of GaAs substrate wafers. It will be understood, however, that some or all of the features of the present disclosure can be implemented in processing of other types of semiconductor wafers. Further, some of the features can also be applied to situations involving non-semiconductor wafers.
[0030] In the description herein, various examples are described in the context of back-side processing of wafers. It will be understood, however, that some or all of the features of the present disclosure can be implemented in front-side processing of wafers.
[0031] In the process 10 of FIG. 1, a functional wafer can be provided (block 11). FIG. 2A depicts a side view of such a wafer 30 having first and second sides. The first side can be a front side, and the second side a back side.
[0032] FIG. 2B depicts an enlarged view of a portion 31 of the wafer 30. The wafer 30 can include a substrate layer 32 (e.g., a GaAs substrate layer). The wafer 30 can further include a number of features formed on or in its front side. In the example shown, a transistor 33 and a metal pad 35 are depicted as being formed the front side. The example transistor 33 is depicted as having an emitter 34*b*, bases 34*a*, 34*c*, and a collector 34*d*. Although not shown, the circuitry can also include formed passive components such as inductors, capacitors, and source, gate and drain for incorporation of planar field effect transistors (FETs) with heterojunction bipolar transistors (HBTs). Such structures can be formed by various processes performed on epitaxial layers that have been deposited on the substrate layer.
[0033] Referring to the process 10 of FIG. 1, the functional wafer of block 11 can be tested (block 12) in a number of ways prior to bonding. Such a pre-bonding test can include, for example, DC and RF tests associated with process control parameters.
[0034] Upon such testing, the wafer can be bonded to a carrier (block 13). In certain implementations, such a bonding can be achieved with the carrier above the wafer. Thus, FIG. 2C shows an example assembly of the wafer 30 and a carrier 40 (above the wafer) that can result from the bonding step 13. In certain implementations, the wafer and carrier can be bonded using temporary mounting adhesives such as wax or commercially available Crystalbond™. In FIG. 2C, such an adhesive is depicted as an adhesive layer 38.
[0035] In certain implementations, the carrier 40 can be a plate having a shape (e.g., circular) similar to the wafer it is supporting. Preferably, the carrier plate 40 has certain physical properties. For example, the carrier plate 40 can be relatively rigid for providing structural support for the wafer. In another example, the carrier plate 40 can be resistant to a number of chemicals and environments associated with various wafer processes. In another example, the carrier plate 40 can have certain desirable optical properties to facilitate a number of processes (e.g., transparency to accommodate optical alignment and inspections)
[0036] Materials having some or all of the foregoing properties can include sapphire, borosilicate (also referred to as Pyrex), quartz, and glass (e.g., SCG72).
[0037] In certain implementations, the carrier plate 40 can be dimensioned to be larger than the wafer 30. Thus, for circular wafers, a carrier plate can also have a circular shape with a diameter that is greater than the diameter of a wafer it supports. Such a larger dimension of the carrier plate can facilitate easier handling of the mounted wafer, and thus can allow more efficient processing of areas at or near the periphery of the wafer.
[0038] Tables 1A and 1B list various example ranges of dimensions and example dimensions of some example circular-shaped carrier plates that can be utilized in the process 10 of FIG. 1.

TABLE 1A

Carrier plate diameter range	Carrier plate thickness range	Wafer size
Approx. 100 to 120 mm	Approx. 500 to 1500 um	Approx. 100 mm
Approx. 150 to 170 mm	Approx. 500 to 1500 um	Approx. 150 mm
Approx. 200 to 220 mm	Approx. 500 to 2000 um	Approx. 200 mm
Approx. 300 to 320 mm	Approx. 500 to 3000 um	Approx. 300 mm

TABLE 1B

Carrier plate diameter	Carrier plate thickness	Wafer size
Approx. 110 mm	Approx. 1000 um	Approx. 100 mm
Approx. 160 mm	Approx. 1300 um	Approx. 150 mm
Approx. 210 mm	Approx. 1600 um	Approx. 200 mm
Approx. 310 mm	Approx. 1900 um	Approx. 300 mm

[0039] An enlarged portion 39 of the bonded assembly in FIG. 2C is depicted in FIG. 2D. The bonded assembly can include the GaAs substrate layer 32 on which are a number of devices such as the transistor (33) and metal pad (35) as described in reference to FIG. 2B. The wafer (30) having such

substrate (**32**) and devices (e.g., **33**, **35**) is depicted as being bonded to the carrier plate **40** via the adhesive layer **38**.

[0040] As shown in FIG. **2**D, the substrate layer **32** at this stage has a thickness of d**1**, and the carrier plate **40** has a generally fixed thickness (e.g., one of the thicknesses in Table 1). Thus, the overall thickness (Tassembly) of the bonded assembly can be determined by the amount of adhesive in the layer **38**.

[0041] In a number of processing situations, it is preferable to provide sufficient amount of adhesive to cover the tallest feature(s) so as to yield a more uniform adhesion between the wafer and the carrier plate, and also so that such a tall feature does not directly engage the carrier plate. Thus, in the example shown in FIG. **2**D, the emitter feature (**34***b* in FIG. **2**B) is the tallest among the example features; and the adhesive layer **38** is sufficiently thick to cover such a feature and provide a relatively uninterrupted adhesion between the wafer **30** and the carrier plate **40**.

[0042] Referring to the process **10** of FIG. **1**, the wafer—now mounted to the carrier plate—can be thinned so as to yield a desired substrate thickness in blocks **14** and **15**. In block **14**, the back side of the substrate **32** can be ground away (e.g., via two-step grind with coarse and fine diamond-embedded grinding wheels) so as to yield an intermediate thickness-substrate (with thickness d2 as shown in FIG. **2**E) with a relatively rough surface. In certain implementations, such a grinding process can be performed with the bottom surface of the substrate facing downward.

[0043] In block **15**, the relatively rough surface can be removed so as to yield a smoother back surface for the substrate **32**. In certain implementations, such removal of the rough substrate surface can be achieved by an O_2 plasma ash process, followed by a wet etch process utilizing acid or base chemistry. Such an acid or base chemistry can include HCl, H_2SO_4, HNO_3, H_3PO_4, H_3COOH, NH_4OH, H_2O_2, etc., mixed with H_2O_2 and/or H_2O. Such an etching process can provide relief from possible stress on the wafer due to the rough ground surface.

[0044] In certain implementations, the foregoing plasma ash and wet etch processes can be performed with the back side of the substrate **32** facing upward. Accordingly, the bonded assembly in FIG. **2**F depicts the wafer **30** above the carrier plate **40**. FIG. **2**G shows the substrate layer **32** with a thinned and smoothed surface, and a corresponding thickness of d**3**.

[0045] By way of an example, the pre-grinding thickness (d**1** in FIG. **2**D) of a 150 mm (also referred to as "6-inch") GaAs substrate can be approximately 675 μm. The thickness d2 (FIG. **2**E) resulting from the grinding process can be in a range of approximately 102 μm to 120 μm. The ash and etching processes can remove approximately 2 μm to 20 μm of the rough surface so as to yield a thickness of approximately 100 μm. (d**3** in FIG. **2**G). Other thicknesses are possible.

[0046] In certain situations, a desired thickness of the back-side-surface-smoothed substrate layer can be an important design parameter. Accordingly, it is desirable to be able to monitor the thinning (block **14**) and stress relief (block **15**) processes. Since it can be difficult to measure the substrate layer while the wafer is bonded to the carrier plate and being worked on, the thickness of the bonded assembly can be measured so as to allow extrapolation of the substrate layer thickness. Such a measurement can be achieved by, for example, a gas (e.g., air) back pressure measurement system that allows detection of surfaces (e.g., back side of the substrate and the "front" surface of the carrier plate) without contact.

[0047] As described in reference to FIG. **2**D, the thickness ($T_{assembly}$) of the bonded assembly can be measured; and the thicknesses of the carrier plate **40** and the un-thinned substrate **32** can have known values. Thus, subsequent thinning of the bonded assembly can be attributed to the thinning of the substrate **32**; and the thickness of the substrate **32** can be estimated.

[0048] Referring to the process **10** of FIG. **1**, the thinned and stress-relieved wafer can undergo a through-wafer via formation process (block **16**). FIGS. **2**H-**2**J show different stages during the formation of a via **44**. Such a via is described herein as being formed from the back side of the substrate **32** and extending through the substrate **32** so as to end at the example metal pad **35**. It will be understood that one or more features described herein can also be implemented for other deep features that may not necessarily extend all the way through the substrate. Moreover, other features (whether or not they extend through the wafer) can be formed for purposes other than providing a pathway to a metal feature on the front side.

[0049] To form an etch resist layer **42** that defines an etching opening **43** (FIG. **2**H), photolithography can be utilized. Coating of a resist material on the back surface of the substrate, exposure of a mask pattern, and developing of the exposed resist coat can be achieved in known manners. In the example configuration of FIG. **2**H, the resist layer **42** can have a thickness in a range of about 15 μm to 20 μm.

[0050] To form a through-wafer via **44** (FIG. **2**I) from the back surface of the substrate to the metal pad **35**, techniques such as dry inductively coupled plasma (ICP) etching (with chemistry such as BCl_3/Cl_2) can be utilized. In various implementations, a desired shaped via can be an important design parameter for facilitating proper metal coverage therein in subsequent processes.

[0051] FIG. **2**J shows the formed via **44**, with the resist layer **42** removed. To remove the resist layer **42**, photoresist strip solvents such as NMP (N-methyl-2-pyrrolidone) and EKC can be applied using, for example, a batch spray tool. In various implementations, proper removal of the resist material **42** from the substrate surface can be an important consideration for subsequent metal adhesion. To remove residue of the resist material that may remain after the solvent strip process, a plasma ash (e.g., O_2) process can be applied to the back side of the wafer.

[0052] Referring to the process **10** of FIG. **1**, a metal layer can be formed on the back surface of the substrate **32** in block **17**. FIGS. **2**K and **2**L show examples of adhesion/seed layers and a thicker metal layer.

[0053] FIG. **2**K shows that in certain implementations, an adhesion layer **45** such as a nickel vanadium (NiV) layer can be formed on surfaces of the substrate's back side and the via **44** by, for example, sputtering. Preferably, the surfaces are cleaned (e.g., with HCl) prior to the application of NiV. FIG. **2**K also shows that a seed layer **46** such as a thin gold layer can be formed on the adhesion layer **45** by, for example, sputtering. Such a seed layer facilitates formation of a thick metal layer **47** such as a thick gold layer shown in FIG. **2**L. In certain implementations, the thick gold layer can be formed by a plating technique.

[0054] In certain implementations, the gold plating process can be performed after a pre-plating cleaning process (e.g.,

O_2 plasma ash and HCl cleaning). The plating can be performed to form a gold layer of about 3 μm to 6 μm to facilitate the foregoing electrical connectivity and heat transfer functionalities. The plated surface can undergo a post-plating cleaning process (e.g., O_2 plasma ash).

[0055] The metal layer formed in the foregoing manner forms a back side metal plane that is electrically connected to the metal pad **35** on the front side. Such a connection can provide a robust electrical reference (e.g., ground potential) for the metal pad **35**. Such a connection can also provide an efficient pathway for conduction of heat between the back side metal plane and the metal pad **35**.

[0056] Thus, one can see that the integrity of the metal layer in the via **44** and how it is connected to the metal pad **35** and the back side metal plane can be important factors for the performance of various devices on the wafer. Accordingly, it is desirable to have the metal layer formation be implemented in an effective manner. More particularly, it is desirable to provide an effective metal layer formation in features such as vias that may be less accessible.

[0057] Referring to the process **10** of FIG. **1**, the wafer having a metal layer formed on its back side can undergo a street formation process (block **18**). FIGS. **2M-2O** show different stages during the formation of a street **50**. Such a street is described herein as being formed from the back side of the wafer and extending through the metal layer **52** to facilitate subsequent singulation of dies. It will be understood that one or more features described herein can also be implemented for other street-like features on or near the back surface of the wafer. Moreover, other street-like features can be formed for purposes other than to facilitate the singulation process.

[0058] To form an etch resist layer **48** that defines an etching opening **49** (FIG. **2M**), photolithography can be utilized. Coating of a resist material on the back surface of the substrate, exposure of a mask pattern, and developing of the exposed resist coat can be achieved in known manners.

[0059] To form a street **50** (FIG. **2N**) through the metal layer **52**, techniques such as wet etching (with chemistry such as potassium iodide) can be utilized. A pre-etching cleaning process (e.g., O_2 plasma ash) can be performed prior to the etching process. In various implementations, the thickness of the resist **48** and how such a resist is applied to the back side of the wafer can be important considerations to prevent certain undesirable effects, such as via rings and undesired etching of via rim during the etch process.

[0060] FIG. **2O** shows the formed street **50**, with the resist layer **48** removed. To remove the resist layer **48**, photoresist strip solvents such as NMP (N-methyl-2-pyrrolidone) can be applied using, for example, a batch spray tool. To remove residue of the resist material that may remain after the solvent strip process, a plasma ash (e.g., O_2) process can be applied to the back side of the wafer.

[0061] In the example back-side wafer process described in reference to FIGS. **1** and **2**, the street (**50**) formation and removal of the resist (**48**) yields a wafer that no longer needs to be mounted to a carrier plate. Thus, referring to the process **10** of FIG. **1**, the wafer is debonded or separated from the carrier plate in block **19**. FIGS. **2P-2R** show different stages of the separation and cleaning of the wafer **30**.

[0062] In certain implementations, separation of the wafer **30** from the carrier plate **40** can be performed with the wafer **30** below the carrier plate **40** (FIG. **2P**). To separate the wafer **30** from the carrier plate **40**, the adhesive layer **38** can be heated to reduce the bonding property of the adhesive. For the example Crystalbond™ adhesive, an elevated temperature to a range of about 130° C. to 170° C. can melt the adhesive to facilitate an easier separation of the wafer **30** from the carrier plate **40**. Some form of mechanical force can be applied to the wafer **30**, the carrier plate **40**, or some combination thereof, to achieve such separation (arrow **53** in FIG. **2P**). In various implementations, achieving such a separation of the wafer with reduced likelihood of scratches and cracks on the wafer can be an important process parameter for facilitating a high yield of good dies.

[0063] In FIGS. **2P** and **2Q**, the adhesive layer **38** is depicted as remaining with the wafer **30** instead of the carrier plate **40**. It will be understood that some adhesive may remain with the carrier plate **40**.

[0064] FIG. **2R** shows the adhesive **38** removed from the front side of the wafer **30**. The adhesive can be removed by a cleaning solution (e.g., acetone), and remaining residues can be further removed by, for example, a plasma ash (e.g., O_2) process.

[0065] Referring to the process **10** of FIG. **1**, the debonded wafer of block **19** can be tested (block **20**) in a number of ways prior to singulation. Such a post-debonding test can include, for example, resistance of the metal interconnect formed on the through-wafer via using process control parameters on the front side of the wafer. Other tests can address quality control associated with various processes, such as quality of the through-wafer via etch, seed layer deposition, and gold plating.

[0066] Referring to the process **10** of FIG. **1**, the tested wafer can be cut to yield a number of dies (block **21**). In certain implementations, at least some of the streets (**50**) formed in block **18** can facilitate the cutting process. FIG. **2S** shows cuts **61** being made along the streets **50** so as to separate an array of dies **60** into individual dies. Such a cutting process can be achieved by, for example, a diamond scribe and roller break, saw or a laser.

[0067] In the context of laser cutting, FIG. **2T** shows an effect on the edges of adjacent dies **60** cut by a laser. As the laser makes the cut **61**, a rough edge feature **62** (commonly referred to as recast) typically forms. Presence of such a recast can increase the likelihood of formation of a crack therein and propagating into the functional part of the corresponding die.

[0068] Thus, referring to the process **10** in FIG. **1**, a recast etch process using acid and/or base chemistry (e.g., similar to the examples described in reference to block **15**) can be performed in block **22**. Such etching of the recast feature **62** and defects formed by the recast, increases the die strength and reduces the likelihood of die crack failures (FIG. **2U**).

[0069] Referring to the process **10** of FIG. **1**, the recast etched dies (FIG. **2V**) can be further inspected and subsequently be packaged.

[0070] It will be understood that the processing steps described above can be implemented in the example through-wafer via process described in reference to FIGS. **1** and **2**, as well as in other processing situations. It will also be understood that one or more processing steps can be implemented in different types of semiconductor-based wafers, including but not limited to those formed from semiconductor materials such as groups IV, III-V, II-VI, I-VII, IV-VI, V-VI, II-V; oxides; layered semiconductors; magnetic semiconductors; organic semiconductors; charge-transfer complexes; and other semiconductors.

Copper Metallization

[0071] While metallization of vias and backside contact of GaAs integrated circuits is typically performed using gold, other integrated circuit technologies, such as silicon-based technologies, use copper (Cu) for a contact layer. Cu has superior conductivity, may be applied more uniformly, and is less costly than gold. Further, Cu has a sufficiently low dissolution rate in solder, so allows the integrated circuit device to be soldered to its printed circuit board pad. Cu, however, readily oxidizes, which degrades electrical and mechanical characteristics. Accordingly, when used in silicon processes, the Cu is typically applied in thick layers, polished, and then capped with dielectric materials such as silicon nitride to avoid these oxidation effects.

[0072] Although Cu has been used successfully in silicon wafer technology, to the best of the inventors' knowledge, Cu has not been successfully used in GaAs integrated circuit devices. A number of obstacles have hindered the effective use of copper in metallization of GaAs devices. For example, Cu is an unintentional source of impurity, and is often proven to be the leading cause of GaAs device failures. Cu rapidly diffuses into GaAs substrates, at a rate faster than the diffusion of gold into GaAs substrates, and faster than the diffusion of Cu into silicon substrates. Once Cu diffuses into source/gate/drain region of a field effect transistor (FET) or active areas of a heterojunction bipolar transistor (HBT), the device will degrade, and eventually fail electrically. Unlike gold, Cu can diffuse into GaAs and create deep energy levels in the GaAs band gap region. These deep levels will trap charges, which lead to degradation and failure of the GaAs devices.

[0073] Without wishing to be bound by theory, the inventors have determined that there are three mechanisms of Cu diffusion in GaAs. The first is bulk or lattice diffusion, which involves vacancies in the GaAs lattice and the exchange of Cu atoms between layers in the GaAs lattice. Bulk diffusion is highly temperature dependent. The second mechanism is the intermetallic compound formation between Cu and GaAs. The third mechanism is interstitial diffusion, in which Cu atoms move along defects, dislocations, or grain boundaries in GaAs. This third mechanism is of particular importance because during processing, the GaAs surface is often damaged. Consequently, there are voids, dislocations, and other defects present on the GaAs surface, which facilitate the movement of Cu atoms within the GaAs lattice structure.

[0074] Accordingly, the use of Cu typically results in the destruction or nonoperation of GaAs integrated circuits. Further, Cu readily oxidizes, and so is difficult to use as a contact material in GaAs integrated circuits without any protection. It is therefore necessary to modify the process outlined above in order to permit the use of Cu to form the metal layer lining the back side of the wafer and the surface of the vias. Certain aspects of the present invention are directed to novel process modifications and techniques which the inventors have developed to overcome at least some of the obstacles in using copper for via and backside metallization of GaAs integrated circuits.

[0075] To overcome the obstacles associated with effectively substituting copper for at least some of the gold in vias and back-side metal layers of GaAs integrated circuits, the inventors have developed modified processes, particularly for forming through-wafer features. The inventors have found that the quality of through wafer via (TWV) copper plating is affected not only by plating parameters but also by surface treatment techniques. The inventors have also found that Cu plating parameter optimization through plating solution flow, wafer rotation, temperature, and current density alone could not achieve satisfactory bottom up fill. An undesirable conformal coating often results. Changing process parameters could also incur other problems such as wafer stress and warpage.

[0076] To address these challenges associated with Cu TWV plating, the inventors have developed innovative precleaning and surface treatment processes for copper plating TWVs to achieve correct copper thickness and improved step coverage in TWV. The processes generally involve modifying surface treatment and plating seed layer to achieve more favorable results without negatively affecting other properties of the wafer.

[0077] FIG. **3** shows one embodiment of such a modified via metallization process represented in Block **17** of FIG. **1**, which is developed for copper metallization of a GaAs TWV. In the process **10** of FIG. **3**, the via metallization process (block **17**) begins with a pre-clean step (block **17***a*). FIG. **2**J depicts the formed via **44** processed through the pre-clean step **17***a*. In various implementations, the pre-clean step removes residues and other contamination from the via **44** and back surface of the substrate **32** and activates the surfaces for subsequent metal adhesion.

[0078] Referring to the process **10** of FIG. **3**, a metal barrier and seed layer can be subsequently formed in the via **44** and on the back surface of the substrate **32** in block **17***b*. FIG. **2**K shows an example of a seed layer **45** and a metal barrier layer **46** that can be formed in the via **44** and on the back surface of the substrate **32**.

[0079] Referring to the process **10** of FIG. **3**, a copper layer is formed in the via **44** and on the back surface of the substrate **32** in block **17***c*. FIG. **2**L shows an example of a copper layer **47** that can be formed in the via **44** and on the back surface of the substrate **32**. The copper layer **47** can replace some or all of the gold contact layer that is typically deposited in the via **44** and on the back surface. As FIG. **3** further shows, a heat treatment step in block **17***d* can follow the copper deposition process of block **17***c*.

[0080] In some implementations of the embodiment shown in FIG. **3**, the via metallization process (blocks **17***a*-**17***d*) is followed by street formation (block **18**), and deposition of a protective layer deposition (block **18***a*) before debonding wafer from carrier.

[0081] FIGS. **4**A-**4**D show examples of cross sectional diagrams of a section **100** of a GaAs wafer with a TWV formed in accordance with some embodiments of the process **10** depicted in FIG. **3**. As illustrated, the GaAs section **100** has via **113** extending through a GaAs substrate **32**. Referring to the process **10** of FIG. **3**, the via **113** may be pre-cleaned (block **17***a*) using, for example HCl and/or an O_2 plasma ash process.

[0082] Following cleaning, a barrier layer followed by a seed layer may be deposited (block **17***b*) in the via **113**. As shown in FIG. **4**B, first a barrier layer **104** is deposited on the contact side **105** of the GaAs substrate **102**. In one example, the barrier layer **104** is a nickel vanadium (NiV) layer disposed at about **800** angstroms thickness. The NiV may be deposited using a physical vapor deposition process (commonly known as sputtering), or other known deposition process. The NiV provides an effective diffusion barrier between the GaAs substrate and a Cu contact layer, which will be applied later. Since Cu is known to have an undesirable diffusion effect on GaAs, the NiV is deposited in a relatively

thick layer. It will be appreciated that the thickness of the layer may be adjusted according to the needs of the particular application. For example, devices subjected to long-term use may require thicker layers, and the layer may be adjusted according to other material used, for example, in the seed layer to be subsequently deposited.

[0083] As FIG. **4**B further shows, a seed layer **109** may be deposited on the barrier layer **104**. Although the seed layer **109** may not always be necessary, it has been found that a seed layer facilitates better mechanical and electrical connection of the Cu contact layer. The metal seed layer may be, for example, either a Cu layer or a gold layer, and may be deposited at a thickness of about 700 angstroms using a physical vapor deposition process. If Cu is used as the seed layer, then an activation process may need to be performed at a later time if the Cu has been allowed to oxidize.

[0084] The via **113** may then be plated with a Cu contact layer **106** (block **17***c*). The Cu contact layer **106** is deposited on the seed layer **109**, if present. The Cu contact layer **106** is preferably deposited using an electroplating process. The Cu contact layer **106** can be deposited at a relatively uniform thickness, such as about 6 μm. It will be appreciated that other types of processes and thicknesses may be used. Depending on the size of the via **113**, the Cu contact layer **106** may simply coat the walls, or may nearly fill the via. To facilitate faster production, a 6 μm coating of the Cu contact layer **106** typically provides sufficient electrical conduction, while leaving a central opening in via **113**.

[0085] One typical electroplating process involves the use of a copper sulfate ($CuSO_4$) bath. Typical $CuSO_4$ based electroplating chemistry contains a small amount of chloride ions, a suppressor component such as polyethylene glycol (PEG), an accelerator component such as bis(sodiumsulfopropyl) disulfide (SPS), and in most cases a nitrogen based leveling agent such as thiourea.

[0086] As depicted in FIG. **3**, following the Cu plating, the GaAs substrate **102** can be subjected to heat treatment (block **17***d*). The metallization process can continue for 48 hours or more. Heat treatment is advantageous because Cu metallization could be a long process that disadvantageously extends production time of GaAs integrated circuit devices. Additionally, this slow process can result in Cu structure with significant defects, cracks, etc caused by the slow growth. The inventors have found that adding heat to the process both significantly accelerates the metallization process and increase the quality and uniformity of the Cu grain structure. In typical PECVD processes, the heat treatment involves application of temperatures between 200 to 300° C. These temperatures may exceed the melting point for the adhesive used to bond the wafer to the carrier. Subjecting GaAs wafers mounted onto carriers to such high temperatures may therefore disadvantageously decrease the bonding strength of the carrier and wafer. Accordingly, in certain embodiments the GaAs device is subjected to a temperature of approximately 100° C. Once the GaAs has been subjected to heat treatment, the metallization (block **17**) of via **113** is complete. In other embodiments, the heat treatment (block **17***d*) step can be removed from the process.

[0087] Referring to the process **70** of FIG. **3**, the GaAs wafer having a Cu contact layer **106** formed on its back side can undergo a street formation process (block **18**). Such a street is described herein as being formed from the back side of the wafer and extending through the Cu contact layer **106** to facilitate subsequent singulation of dies. It will be understood that one or more features described herein can also be implemented for other street-like features on or near the back surface of the wafer. Moreover, other street-like features can be formed for purposes other than to facilitate the singulation process.

[0088] The street can be formed as described above with respect to FIG. **1** and FIGS. **2**M-**2**O. An etch resist layer defining a street opening can be formed using standard photolithography. Next, the exposed street opening in the Cu contact layer **106** may be etched using wet etching, although other etching processes are also possible. A pre-etching cleaning process (e.g., O_2 plasma ash) can be performed prior to the etching process. In various implementations, the thickness of the resist and how such a resist is applied to the back side of the wafer can be important considerations to prevent certain undesirable effects, such as via rings and undesired etching of via rim during the etch process.

[0089] After etching the street into Cu contact layer **106**, the resist layer may be removed, using photoresist strip solvents such as NMP (N-methyl-2-pyrrolidone), applied using, for example, a batch spray tool. To remove residue of the resist material that may remain after the solvent strip process, a plasma ash (e.g., O_2) and/or aqueous wash process can be applied to the back side of the wafer.

[0090] Following street formation (block **18**), a protective layer **108** may be deposited over the back side of the GaAs wafer (block **18***a*). Since Cu is highly reactive with oxygen, a protective layer **108** is deposited over the Cu contact layer **106**. In one example, the protective layer **108** is an organic solder preservative (OSP). The OSP may be applied using a bath process, or other known processes may be used. The OSP may be deposited at a thickness of about 700 angstroms. It will be appreciated that other thicknesses may be used depending upon application specific requirements and the particular materials used. For example, thicknesses in the range of about 100 angstroms to about 900 angstroms have been found to be effective, although other thicknesses may be alternatively used.

[0091] As described in more detail above, street formation (block **18**) may be followed by debonding the wafer from the carrier (block **19**), and testing the wafer following debonding (block **20**). The resulting structure is shown in FIG. **4**D.

Seed Layer Modification

[0092] Plating the via **113** with a Cu layer is a sensitive and difficult process. It is particularly difficult to achieve a bottom-up fill profile. The optimized via fill process not only relies on plating parameters but also upon variations in precleaning and any surface treatment prior to plating. Standard attempts to optimize Cu plating include monitoring and adjusting solution flow, wafer rotation, temperature, and/or current density. Such modifications have been unable to achieve satisfactory bottom-up fill of the through-wafer via **113**, and often results in conformal plating. Meanwhile, changing process parameters could also incur other problems such as wafer stress and warpage. Accordingly, achieving the correct thickness of Cu within the via **113** presents a complex challenge.

[0093] In order to optimize the Cu plating process of a through wafer via, a variation of the process described above can be employed. In particular, the barrier/seed deposition step (block **17***b*) of FIG. **3** is modified to achieve improved Cu plating of the through wafer via **113**, without sacrificing other mechanical or electrical properties of the wafer. FIG. **5** shows

one embodiment of a modified barrier/seed deposition process represented in block **17***b* of FIG. **3**.

[0094] The process **10** of FIG. **5** begins with depositing a barrier/seed layer (block **71**). FIG. **6**A depicts the formed via **113** with a barrier layer **104** deposited over the surface of the substrate **102**. As described above, the barrier layer **104** can be a nickel vanadium (NiV) layer disposed at about 800 angstroms thickness. The NiV provides an effective diffusion barrier between the GaAs substrate and the Cu contact layer **106**, which will be applied later. Since Cu is known to have an undesirable diffusion effect on GaAs, the NiV is deposited in a relatively thick layer. It will be appreciated that the thickness of the layer may be adjusted according to the needs of the particular application. For example, devices subjected to long-term use may require thicker layers, and the layer may be adjusted according to other material used, for example, in the seed layer **109**.

[0095] As further shown in FIG. **6**B, a seed layer **109** is then deposited on the barrier layer **104**. It has been found that a seed layer facilitates better mechanical and electrical connection of the Cu contact layer. The metal seed layer may be, for example, a Cu layer, a gold layer, or a palladium layer. As illustrated in FIG. **6**B, the seed layer **109** can be formed by depositing small particles **110** using a physical vapor deposition process, to a thickness of about 700 angstroms.

[0096] Following deposition, an a portion of the seed layer **109** can oxidize, thereby giving rise to oxide layer **111** over the top surface of seed layer **109** as shown in FIG. **6**C. As noted above, oxidation can degrade electrical and mechanical characteristics of the device. Accordingly, it is often desirable to remove the oxide layer **111**.

[0097] In the process **10** of FIG. **5**, a plasma treatment (block **72**) can be used to remove the oxide layer **111**, as shown in FIG. **6**D. The plasma **112** can be, for example, an oxygen plasma. Following the plasma treatment, an acid rinse can be applied (block **73**). As shown in FIG. **6**E, an acid rinse **114** is applied over the surface of the device. The acid rinse **114** can be a dilute hydrochloric acid, for example. Together, the plasma treatment (block **72**) and acid rinse (block **73**) remove the oxide layer **111**, as shown in FIG. **6**F. Additionally, the surface of the barrier layer **109** is modified by the plasma treatment, such that the surface transitions from being hydrophobic to hydrophilic. Rendering the barrier layer **109** hydrophilic improves the ability of the Cu plating solution to wet to the surface of the barrier layer **109**, and accordingly can improve Cu plating performance.

[0098] In the process **10** of FIG. **5**, surface activation (block **74**) follows the acid rinse step (block **73**). As shown in FIG. **6**G, the substrate **102** is rinsed in a diluted accelerator solution **115**. In some embodiments, no DI rinse is used after the diluted accelerator solution **115**. Thus, the accelerator solution coats a monolayer **116** accelerator molecules over the surface of the barrier layer **109**, as shown in FIG. **6**H. The accelerator can be, for example, bis(sodiumsulfopropyl) disulfide (SPS). The presence of the accelerator monolayer **116** prior to the Cu plating step (block **17***c*) can improve the plating performance. As shown in FIG. **6**I, a Cu plating solution **117** can then be applied over the surface of the barrier layer **109** and monolayer **111**.

[0099] As noted above, a typical Cu plating solution **117** contains a small amount of chloride ions, a suppressor component such as polyethylene glycol (PEG), an accelerator component such as bis(sodiumsulfopropyl) disulfide (SPS), and in most cases a nitrogen based leveling agent such as thiourea. A competition model has been understood to explain the mechanism of via fill during the Cu plating process. According to this model, chloride is complexed with the suppressor. Due to the long chain polymer nature of the suppressor, it is unable to diffuse rapidly into a via formed on a semiconductor wafer. The accelerator, on the other hand, is often a relatively small molecule, which can diffuse much more rapidly than the suppressor into the via. As a result, the suppressor will primarily accumulate on the surface of the semiconductor wafer, whereas the accelerator will primarily accumulate inside the via. The higher concentration of the accelerator increases the plating rate of Cu deposition within the via. On the surface of the wafer, however, the suppressor functions as a diffusion barrier to prevent Cu ions from diffusing onto the surface, and consequently preventing reduction of the Cu ions to Cu metal. The accelerator-copper complex will gradually replace the suppressor-chloride complex on the wafer surface, such that a Cu layer **106** will then be plated on the surface of the wafer, albeit at a rate slower than the plating inside the via **113**. As shown in FIG. **6**J, a Cu layer **106** is formed over the surface of the wafer. This difference in diffusion mechanism between the suppressor and accelerator complexes, combined with the competitive interaction between them, contribute to the bottom-up fill of Cu metallization inside the via **113**.

[0100] The Cu layer **106** is deposited at a relatively uniform thickness, such as about 6 μm. It will be appreciated that other types of processes and thicknesses may be used. Depending on the size of the via **113**, the Cu may simply coat the walls, or may nearly fill the via. To facilitate faster production, a 6 μm coating of the Cu contact layer **106** typically provides sufficient electrical conduction, while leaving a central opening in via **113**.

[0101] Following the Cu plating (block **17***c*), the process **10** may continue as described above with respect to FIGS. **1**-**4**.

Integrated Circuit Singulation and Packaging

[0102] FIG. **7**A illustrates a GaAs wafer **200** with a plurality of individual integrated circuits **201** formed in accordance with embodiments of the invention in which copper is used as a contact metal for the vias and back-side plane. As shown in FIG. **7**A, streets **202** have been formed in the regions between each integrated circuit **201** on the wafer **200**. As described above, street formation involves removing Cu in the regions between the integrated circuits.

[0103] Following street formation, the wafer **200** is placed onto cutting tape **203**, with the backside of the GaAs wafer **200** adhering to the cutting tape **203** and frame **204** in the manner shown in FIGS. **7**B and **7**C. Next, the integrated circuit dies are singulated by cutting through the GaAs wafer along the pre-formed streets. A scribe may be applied to the streets in order to mechanically singulate the integrated circuit dies. Alternatively, a laser may be used to burn through the streets. Mechanical scribing is inexpensive, but typically less accurate than laser singulation, and may cause damage to the die. Laser singulation is more accurate and reduces damage, but at increased expense.

[0104] Once the integrated circuit dies have been singulated, the cutting tape is stretched apart. This stretching ensures that the dies have been singulated, as it results in widening the separation between each of the dies. The cutting tape may be stretched until the tape is visible between each of the dies. FIG. **7**C illustrates stretched cutting tape in which some of the singulated dies have been removed. The dies may

be removed from the cutting tape manually or by automated robotics. For example, an automated die-picking machine may select and remove individual dies through the use of vacuum pressure. FIG. 7D illustrates a singulated GaAs integrated circuit die, according to an embodiment of the present invention.

[0105] Once individual GaAs integrated circuit dies have been formed, they may be packaged for incorporation into larger electronic devices. Various types of packaging exist, some of which are described in more detail below. It will be understood that there exist myriad different types of packaging beyond those listed and described herein. Depending on the desired application, virtually any type of packaging may be used in accordance with the present invention. Four different packages are described in more detail below: ball grid array (BGA), land grid array (LGA), molded leadframe, and quad-flat no-leads (QFN).

[0106] FIG. **8** shows an example shows an example sequence of BGA packaging of singulated GaAs integrated circuit dies, according to one embodiment, with FIGS. **9**A-**9**H showing examples of structures at various stages of the processing sequence of FIG. **8**. With reference to FIG. **9**A, individual dies **201** are arranged (block **501**), typically in an array, onto a laminate packaging substrate **205**. A single packaging substrate **205** such as that shown in FIG. **9**A can include between 200 to 400 dies **201**, although the specific number may vary depending on the application. The packaging substrate **205** includes pre-formed lower contact pads **206** on its lower surface. On the top surface the packaging substrate has die attach pads **207**, onto which singulated dies **201** are mounted, and a plurality upper contact pads **208**. The packaging substrate includes internal interconnections to electrically connect the upper contact pads **208** on the top surface to the lower contact pads **206** on the bottom surface.

[0107] The die attach pad **207** is typically flat and made of tin-lead, silver, or gold-plated copper. With reference to FIGS. **9**B and **9**C, the individual dies **201** are attached to the die attach pads **207** (block **502**) by applying solder paste to all die attach pads **207**. Solder paste is an adhesive mixture of flux and tiny solder particles. The solder paste may be deposited by the use of a screen printing process, or by jet-printing. After the solder paste has been applied, individual dies are placed onto the packaging substrate **205** by robotic pick-and-place machines. Individual dies **201** may be removed from the cutting tape and transferred directly to the packaging substrate, where they are positioned to align the die attach pads with the contacts of the individual dies. The solder paste connects the die attach pads **207** to the contacts of the individual dies **201**. To provide a more robust connection, the dies are subjected to heat treatment for solder reflow. The precise temperatures and times for this process will vary depending on the composition of the solder paste. Typical temperatures range from 100° to 260° C., with dwell times at peak temperatures ranging from 50 seconds to two minutes. This heat treatment causes the solder particles within the solder paste to melt. The solder is then allowed to cool, resulting in a robust electrical and mechanical connection between the packaging substrate and the individual dies.

[0108] With reference to FIG. **9**D, following attachment of the individual dies **201** to the packaging substrate **205**, electrical interconnection is formed between bonding pads on the integrated circuit and the upper contact pads **208** on the top surface of the packaging substrate **205** (block **503**). This connection may be formed by wire bonding or flip-chip methods. Wire bonding involves arranging wires **209**, often made of copper, gold, or aluminum, between an upper contact pad **208** at one end, and a bonding pad on the integrated circuit die **201** at the other. The wire **209** is attached using some combination of heat, pressure, and ultrasonic energy to weld the wire **209** in place. Flip chip interconnection involves applying solder bumps to the bonding pads on the top surface of the integrated circuit. The integrated circuit is then inverted, and arranged such that the solder bumps align with contact pads. With the application of heat, the solder bumps melt and, following a cooling process, an electrical and mechanical connection may be formed between the bonding pads on the integrated circuit die and the contact pads on the packaging substrate.

[0109] With reference to FIG. **9**E, after electrical interconnection has been formed between the die and the packaging substrate, the entire packaging substrate is covered with a molding compound **210** (block **504**). There are a wide variety of commercially available molding compounds. Typically, these are epoxy-based compounds. The packaging substrate **205** covered with the molding compound **210** is then cured in an oven. The temperature and duration of curing depends on the particular molding compound selected. As shown in FIG. **9**F, after the molding compound **210** has cured, the each die **201** on the packaging substrate **210** is totally encapsulated, including the electrical interconnections **209**, with only the bottom surface of the packaging substrate **205**, with its lower contact pads, exposed. At this stage, the packaging substrate **205** covered with cured molding compound **210** can be sawed (block **505**), thereby singulating the packaged devices. Singulation may be performed mechanically, such as with a wafer saw.

[0110] Each packaged device is inverted at this stage, and then on top of each lower contact pad on the packaging substrate, a small ball of solder paste is deposited, creating a grid of solder paste balls **206** (block **506**). The BGA package may then be placed over solder pads on a PCB, with each solder paste ball **206** aligned to a solder pad. The solder pads are flat, and typically made of tin-lead, silver, or gold-plated copper. FIG. **9**E illustrates a schematic cross-section of a singulated BGA packaged die, with FIGS. **9**G and **9**H illustrating the top and bottom perspective views of the same.

[0111] FIG. **10** shows an example shows an example sequence of LGA packaging of singulated GaAs integrated circuit dies, with FIGS. **11**A-**11**G showing examples of structures at various stages of the processing sequence of FIG. **10**. In many respects, LGA packaging is similar to BGA packaging. As shown in FIG. **11**A, individual dies **201** are arranged (block **401**), typically in an array, onto a laminate packaging substrate **205**. The packaging substrate **205** includes pre-formed lower contact pads **206** on its lower surface. On the top surface the packaging substrate has die attach pads **207**, onto which singulated dies **201** are mounted, and a plurality upper contact pads **208**. The packaging substrate includes internal interconnections to electrically connect the upper contact pads **208** on the top surface to the lower contact pads **206** on the bottom surface.

[0112] The die attach pad **207** is typically flat and made of tin-lead, silver, or gold-plated copper. With reference to FIGS. **11**B and **11**C, the individual dies **201** are attached to the die attach pads **207** (block **402**) by applying solder paste to all die attach pads **207**, similar to BGA packaging. After the solder paste has been applied, individual dies are placed onto the packaging substrate **205** by robotic pick-and-place

machines. The solder paste connects the die attach pads **207** to the contacts of the individual dies **201**. To provide a more robust connection, the dies are subjected to heat treatment for solder reflow, as described in more detail above.

[0113] With reference to FIG. **11**D, following attachment of the individual dies **201** to the packaging substrate **205**, electrical interconnection is formed between bonding pads on the integrated circuit and the upper contact pads **208** on the top surface of the packaging substrate **205** (block **403**). This connection may be formed by wire bonding or flip-chip methods, as described with respect to BGA packaging above.

[0114] With reference to FIG. **11**E, after electrical interconnection has been formed between the die and the packaging substrate, the entire packaging substrate is covered with a molding compound **210** (block **404**). The packaging substrate **205** covered with the molding compound **210** is then cured in an oven. As shown in FIG. **11**F, after the molding compound **210** has cured, the each die **201** on the packaging substrate **210** is totally encapsulated, including the electrical interconnections **209**, with only the bottom surface of the packaging substrate **205**, with its lower contact pads, exposed. At this stage, the packaging substrate **205** covered with cured molding compound **210** can be sawed (block **405**), thereby singulating the packaged devices.

[0115] It is at this stage that LGA packaging deviates from BGA packaging described above. In contrast to BGA, LGA does not involve placing small balls of solder paste onto the packaging substrate. Rather, the solder paste, or alternatively molten solder, is placed onto the PCB over the solder pads, and then the LGA packaged device is arranged such that the contact pads **206** are aligned over the solder pads (block **406**). For mounting onto a PCB, the package may be placed over corresponding solder pads on the PCB, followed by heat treatment to induce solder reflow. The PCB is outfitted with pre-formed conductive solder pads, also known as PCB pads, arranged to correspond to contact pads **206** of the packaging substrate. In short, BGA involves applying solder paste to the packaging substrate **205**, whereas LGA involves applying solder paste to the PCB. FIG. **11**E illustrates a schematic cross-section of a singulated BGA packaged die, with FIG. **11**G illustrating a bottom perspective view of the same

[0116] After placement of the packaged device on the packaging substrate, BGA and LGA proceed similarly. The packaged device mounted onto a PCB is subjected to a heat treatment for solder reflow, followed by a cool down period.

[0117] FIG. **12** shows an example shows an example sequence of leadframe packaging of singulated GaAs integrated circuit dies, with FIGS. **13**A-**13**D showing examples of structures at various stages of the processing sequence of FIG. **12**. With reference to FIG. **13**A, individual singulated integrated circuit dies **201** are mounted onto a metallic leadframe **301** (block **601**). The leadframe **301** includes a plurality of die attach regions **302**, and a plurality of leads **303**. The leadframe **301** is typically made of a thin sheet of copper or copper alloy. In some instances, the copper is plated with another metal, such as pure tin, silver, nickel, gold, or palladium. For high-throughput, the processing may be performed in batches, in which an array or strip of connected leadframes is provided.

[0118] The singulated dies **201** can be mounted onto the die attach regions **302** of the leadframe **301** by an adhesive or soldering process (block **601**). The bond is typically formed between the backside metallization of the die and the metal surface of the leadframe. The bond can be formed using solder paste followed by a reflow process, as described above. Alternatively, molten solder can be placed directly onto the die attach pad, followed by placement of the die. Conductive epoxy adhesives may also be used in place of solder.

[0119] With reference to FIG. **13**B, After the die has been attached to the leadframe, wire bonding is then used to form electrical connections **306** between the die attach pads to the package leads (block **602**). Next, a mechanical trimming operation separates the leads **303** from the die bonding platform on the lead frame **301** (block **603**). Plastic or other molding compound **305** is then injection molded around the die **201** and leadframe **301** to form the typical black plastic body (block **604**), similar to the molding processes described above with respect to LGA and BGA packaging. In typical leadframe packaging, however, the frame for injection molding is designed such that a portion of the leads **303** remains uncovered by the molding compound **305**. Following curing, the packaged device is presented with a portion of the leads **303** extending out from the cured molding compound, typically a black plastic. FIG. **13**C illustrates a schematic cross-section of a singulated leadframe packaged die, with FIG. **13**D illustrating a top perspective view of the same

[0120] The sequence illustrated in FIG. **12** can also be applied to quad-flat no lead packaging of singulated GaAs integrated circuit dies. FIGS. **14**A-**14**D show examples of structures at various stages of the processing sequence. QFN packaging is similar to leadframe packaging, with some important distinctions. With reference to FIG. **14**A, QFN packaging also begins with a leadframe **301** comprising die attach regions **302** and a plurality of leads **303**. Singulated dies **201** are attached to the leadframe **301** in a manner similar to that described above with respect to standard leadframe packaging (block **701**). As shown in FIG. **14**B, Wire bonding then follows, as described above, to connect the die **201** to the leadframe leads **303** with wires **306** (block **702**). With QFN packaging, however, the leads **303** are not designed to extend out beyond the cured molding materials after singulation. Accordingly, there is no need for singulation prior to injection molding of the molding compound over the leadframe and die. Instead, a batch of connected mounted dies **201** can be covered with a molding compound, followed by a curing process (block **703**).

[0121] Once the molding compound **305** has cured, the leadframes with mounted dies are singulated (block **704**). Typically a diamond saw is used to cut through the hardened cured molding compound **305**. As the diamond saw cuts through the leads **303**, each side of the QFN package has exposed portions of the leadframe **301**. Unlike traditional leadframe packaging, however, the exposed portions are flush with the molding compound **305**. The leads **303** are also typically exposed on the lower surface of the QFN package. FIG. **14**C illustrates a schematic cross-section of a singulated QFN packaged die, with FIG. **14**D illustrating a bottom and top perspective views of the same.

Mounted GaAs Integrated Circuit Device

[0122] FIG. **15** illustrates one embodiment of a GaAs integrated circuit device **200**. The device **200** generally comprises a printed circuit board **212** connected to a GaAs integrated circuit **211**. The GaAs integrated circuit **211** has a backside **105** and a frontside **103**. The GaAs integrated circuit **211** includes a GaAs substrate **102**, a barrier layer **104**, a protective layer **108**, and a Cu contact layer **106**. In some embodiments, the GaAs integrated circuit **211** may also include a

seed layer **109** between the Cu contact layer **106** and the barrier **104**. The seed layer **109** may serve to facilitate mechanical and electrical connection to the Cu contact layer **106**, but is not always necessary. The printed circuit board includes a pad which is adapted to couple with the GaAs integrated circuit **211** at the backside **105**. The GaAs integrated circuit **211** is configured to be mounted on the printed circuit board **212** by the pad **216**. In one embodiment, the GaAs integrated circuit **211** is mounted to the pad **216** by a layer of solder **218** interposed between the backside **105** and the pad **216**.

[0123] The barrier layer **104** is formed on the lower surface **105** of the GaAs substrate **102** and serves to isolate the Cu contact layer **106** from the GaAs substrate **102** to prevent Cu diffusion. The Cu contact layer **106** is formed on the backside **105** of the GaAs integrated circuit **211**. The Cu contact layer **106** provides an electrical ground contact between the GaAs substrate **102** and the pad **216** on the printed circuit board **212**. In one embodiment, the layer of solder **218** is formed between the Cu contact layer **106** and the pad **216** to securely mechanically attach the backside **105** of the GaAs integrated circuit **211** to the printed circuit board **212**. In one embodiment, the protective layer **108** is formed between the Cu contact layer **106** and the solder **218** to prevent oxidation of the copper. The GaAs substrate **102** comprises a plurality of vias **25** which have been etched through the GaAs substrate **102** to form electrical connections between various integrated circuits disposed thereon. The vias **25** have sidewalls which will comprise the layers previously deposited on the GaAs substrate, as described in more detail above.

[0124] FIG. **16** illustrates a portion of an electronic device incorporating a GaAs integrated circuit device made according to various methods of the present invention. In some embodiments, the device can be a portable wireless device, such as a cellular phone. The device can include a battery configured to supply power to the device, a circuit board configured to provide support for and to interconnect various electronic components, and an antenna configured to receive and transmit wireless signals. The electronic device can include a number of additional components, such as a display processor, central processor, user interface processor, memory, etc. In other embodiments, the electronic device may be a component of a tablet computer, PDA, or other wireless device.

Terminology

[0125] Unless the context clearly requires otherwise, throughout the description and the claims, the words "comprise," "comprising," and the like are to be construed in an inclusive sense, as opposed to an exclusive or exhaustive sense; that is to say, in the sense of "including, but not limited to." The word "coupled", as generally used herein, refers to two or more elements that may be either directly connected, or connected by way of one or more intermediate elements. Additionally, the words "herein," "above," "below," and words of similar import, when used in this application, shall refer to this application as a whole and not to any particular portions of this application. Where the context permits, words in the above Detailed Description using the singular or plural number may also include the plural or singular number respectively. The word "or" in reference to a list of two or more items, that word covers all of the following interpretations of the word: any of the items in the list, all of the items in the list, and any combination of the items in the list.

[0126] The above detailed description of embodiments of the invention is not intended to be exhaustive or to limit the invention to the precise form disclosed above. While specific embodiments of, and examples for, the invention are described above for illustrative purposes, various equivalent modifications are possible within the scope of the invention, as those skilled in the relevant art will recognize. For example, while processes or blocks are presented in a given order, alternative embodiments may perform routines having steps, or employ systems having blocks, in a different order, and some processes or blocks may be deleted, moved, added, subdivided, combined, and/or modified. Each of these processes or blocks may be implemented in a variety of different ways. Also, while processes or blocks are at times shown as being performed in series, these processes or blocks may instead be performed in parallel, or may be performed at different times.

[0127] The teachings of the invention provided herein can be applied to other systems, not necessarily the system described above. The elements and acts of the various embodiments described above can be combined to provide further embodiments.

[0128] While certain embodiments of the inventions have been described, these embodiments have been presented by way of example only, and are not intended to limit the scope of the disclosure. Indeed, the novel methods and systems described herein may be embodied in a variety of other forms; furthermore, various omissions, substitutions and changes in the form of the methods and systems described herein may be made without departing from the spirit of the disclosure. The accompanying claims and their equivalents are intended to cover such forms or modifications as would fall within the scope and spirit of the disclosure.

What is claimed is:

1. A method for surface treatment of through wafer vias in GaAs integrated circuits prior to copper metallization, said method comprising:

modifying a surface of a seed layer formed in said through wafer vias to increase the water affinity of said surface;

rinsing said surface to remove contaminants from the surface; and

activating said surface to facilitate copper deposition onto said surface.

2. The method of claim **1** wherein said seed layer is gold.

3. The method of claim **1** wherein said seed layer is copper.

4. The method of claim **1** wherein said seed layer is palladium.

5. The method of claim **1** wherein modifying said surface comprises treating said surface with plasma.

6. The method of claim **5** wherein said plasma is oxygen plasma.

7. The method of claim **1** wherein rinsing said surface comprises rinsing said surface with dilute hydrochloric acid.

8. The method of claim **1** wherein activating said surface comprises depositing a monolayer of accelerator molecules over said surface.

9. The method of claim **8** wherein the accelerator molecules comprise bis(sodiumsulfopropyl) disulfide (SPS).

10. The method of claim **8** wherein depositing the monolayer comprises rinsing said surface with a diluted accelerator solution.

11. A GaAs integrated circuit formed in accordance with the method of claim **1**.

12. The GaAs integrated circuit of claim **11** wherein said GaAs integrated circuit is incorporated in a wireless telecommunication device.

13. A GaAs integrated circuit formed in accordance with the method of claim **1** wherein said GaAs integrated circuit comprises a copper filled through wafer via.

14. A GaAs integrated circuit formed in accordance with the method of claim **1** wherein said integrated circuit comprises a copper contact pad.

15. A method for metalizing a through wafer via in GaAs integrated circuits, said method comprising:

pre-cleaning said through wafer via;
depositing a barrier layer on a surface of said through wafer via;
depositing a seed layer on said barrier layer;
treating said seed and barrier layers with plasma;
rinsing said seed and barrier layers with an acid;
activating said seed and barrier layers; and
depositing copper in said through wafer via.

16. The method of claim **15** wherein activating said seed and barrier layers comprises coating said seed and barrier layers with a monolayer of accelerator molecules.

17. The method of claim **15** wherein activating said seed and barrier layers comprises rinsing said seed and barrier layers with an accelerator, where said accelerator is not removed from said seed and barrier layers before depositing copper in said through wafer via.

18. A GaAs integrated circuit formed in accordance with the method of claim **15**.

19. A GaAs integrated circuit formed in accordance with the method of claim **15** wherein said GaAs integrated circuit comprises a copper filled through wafer via.

20. A GaAs integrated circuit formed in accordance with the method of claim **15** wherein said integrated circuit comprises a copper contact pad.

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