Gate Oxide Reliability of Poly-Si and Poly-SiGe CMOS devices

Vincent E. Houtsma

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GATE OXIDE RELIABILITY OF POLY-SI AND POLY-SIGE CMOS DEVICES

PROEFSCHRIFT

ter verkrijging van
de graad van doctor aan de Universiteit Twente,
op gezag van de rector magnificus,
Prof.dr. F.A. van Vught,
volgens besluit van het College voor Promoties
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door

Vincent Etienne Houtsma

geboren op 12 september 1970
te Sneek

Dit proefschrift is goedgekeurd door:

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de assistent promotor: Dr. J. Holleman

'There's Plenty of Room at the Bottom'
Richard P. Feynman (1918-1988)

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Voorwoord

De kwaliteit van een proefschrift hangt voor een groot gedeelte af van de beschikbare middelen en de aanwezigheid van stimulerende mensen. De afgelopen vier jaar wist ik mij omringd door mensen die ieder op hun eigen manier tot de kwaliteit van dit proefschrift hebben bijgedragen. Velen hebben bovendien een actief aandeel gehad in het onderzoek en de totstandkoming van dit proefschrift.

Een aantal van hen wil ik hier graag speciaal noemen :

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Vincent Houtsma

Enschede,
December 1999.

Samenvatting

Dit proefschrift behandelt de betrouwbaarheid van silicium-oxide lagen in moderne CMOS transistoren met polykristallijn silicium (poly-Si) en polykristallijn silicium-germanium (poly-SiGe) als gate materiaal. De lekstromen en degradatie van deze oxide lagen met zowel p-type als n-type gate materiaal is onderzocht. Poly-SiGe is gebruikt vanwege de mogelijkheid om de werkfunctie van de gate te kunnen varieëren. De invloed van de werkfunctie op de lekstromen en degradatie van de oxide lagen kan hierdoor onderzocht worden. Belangrijk hierbij te noemen is dat poly-SiGe verenigbaar is met de reeds bestaande Si technologie.

Hoofdstuk 2 laat zien dat de lekstromen voor p-type gates significant anders zijn dan voor n-type gates. Een nieuw model is ontwikkeld dat is gebaseerd op tunneling van minderheidsladingsdragers uit de geleidingsband van de gate om de gemeten stroom-spannings karakteristieken (I-V) van p-type gates te kunnen verklaren.

In hoofdstuk 3 wordt de stress-geïnduceerde lekstroom (SILC) van deze componenten onderzocht. Het verschil in lekstroom tussen p-type en n-type gates heeft ook invloed op de SILC karakteristieken. Voor p-type gates is gevonden dat de SILC asymmetrisch van aard is. Verder is een lagere stress-geïnduceerde lekstroom voor p-type poly-SiGe gevonden in vergelijking met de poly-Si gates. Voor silicium-oxide lagen met een dikte kleiner dan 4 nm is een nieuw geleidingsmechanisme vastgesteld. Voor kleine negatieve gate spanningen wordt de SILC stroom in deze dunne oxides zeer waarschijnlijk bepaald door trap geassisteerd tunnelen van gaten (HTAT). Een inelastisch trap geassisteerd tunnel model is ontwikkeld voor zowel p-type als n-type gates. Dit model kan de gemeten karakteristieken na SILC goed beschrijven.

De doorslag van de silicium-oxide lagen is onderzocht in hoofdstuk 4. Het is vastgesteld dat voor zeer dunne oxides (2.5 nm) de tijd tot doorslag significant afneemt (4 ordes van grootte) als de omgevings-temperatuur toeneemt van 25°C naar 200°C. Dit heeft een grote invloed op de betrouwbaarheid van dunne silicium-oxide lagen. Verder is gevonden dat voor n-type gates de aangelegde gate spanning zich goed verhoudt met de tijd tot doorslag van dunne oxide lagen. Voor p-type gates is een toename van de tijd tot doorslag met toenemende gate temperatuurbudget gevonden. Dit wordt waarschijnlijk veroorzaakt door de afname van de lekstroom met toenemende gate temperatuurbudget voor een constante gate spanning. Dit geeft aan dat zowel de energie van de elektronen als de elektronen stroom van belang zijn voor de tijd tot doorslag van zeer dunne oxide lagen.

In hoofdstuk 5 worden de stroom-spannings karakteristieken (I-V) van n-type poly-Si capaciteiten na doorslag onderzocht. Het is vastgesteld dat na harde-doorslag de I-V karakteristieken volledig bepaald worden door de afmetingen van de verbinding die gevormd wordt tussen de gate en het substraat tijdens doorslag. De totale hoeveelheid vrijgekomen energie tijdens doorslag is hiervoor bepalend. Een elektrisch-thermisch model is ontwikkeld welke de gemeten I-V karakteristieken na doorslag goed kan verklaren. Voor zeer lage vermogens dissipatie kan zachte-doorslag optreden. De I-V karakteristieken na zachte-doorslag duiden erop dat het geleidingsmechanisme na zachte-doorslag asymmetrisch van aard is. Echter het geleidingsmechanisme na zachte doorslag is nog niet volledig begrepen.

Tenslotte zijn in hoofdstuk 6 lichtemissie metingen gedaan aan n-type poly-Si gate capaciteiten na doorslag. Deze licht emissie metingen geven belangrijke informatie over de verbinding die gevormd is tussen de gate en het substraat na doorslag.

Abstract

This thesis focuses on the gate oxide reliability of poly silicon (poly-Si) and poly Silicon-Germanium(poly-$Si_{0.7}Ge_{0.3}$) dual gate CMOS devices. The conduction mechanism (I-V), Stress-Induced Leakage Current (SILC) and time-to-breakdown (t_{bd}) of these devices on (ultra-)thin gate oxides is studied. P^+ and n^+-gates with poly-Si and poly-SiGe are used to study the influence of gate work-function on gate current and SILC current. Poly-SiGe is chosen since its allows modification of the workfunction of the gate for p^+-poly gate devices. Moreover, it is fully compatible with (poly-)Si technology.

In chapter 2 it is observed that for p^+ gate devices the conduction mechanism is significantly different than for n^+ gate devices. A new model based on Minority Carrier Tunneling(MCT) from the conduction band of the gate is proposed for p^+-poly gate devices under gate injection conditions (-V_g). This model describes the observed I-V curves and gate bias asymmetry for p^+-poly gate devices.

Next in chapter 3 the Stress-Induced Leakage Current of these devices is studied. The difference in conduction mechanism for n^+ and p^+ gate devices influences the SILC characteristics. For p^+-poly gate devices, asymmetric SILC (gate bias polarity) and reduced SILC for p^+ poly-SiGe compared to the p^+ poly-Si reference devices is observed. For very thin oxides (t_{ox} <4 nm) the SILC current at low -V_g voltages is most likely caused by trap assisted hole tunneling (HTAT) from the substrate to the gate. An inelastic trap assisted tunneling model is developed to evaluate the SILC current for both n^+ and p^+ gate devices under substrate as well as gate injection conditions. This model is successful in describing the experimental I-V characteristics after SILC.

The time-to-breakdown of both n^+ and p^+ poly-Si gate devices on ultra-thin gate oxides is studied in chapter 4. A decrease in t_{bd} of nearly 4 orders of magnitude is observed when the ambient temperature is increased from 25°C to 200°C for n^+ poly-Si gate devices on 2.5 nm oxides. It is observed that for n^+ gate devices the applied gate voltage V_g correlates well with t_{bd} under substrate as well as gate injection conditions. For p^+-poly Si gate devices an increase of t_{bd} with increasing active gate doping is observed. This is most likely related to a decrease in tunneling current during stress at a fixed gate voltage. This indicates that both the total energy release at the anode and the electron fluence are important parameters for t_{bd} of ultra-thin oxides.

In chapter 5 the post-breakdown I-V characteristics of n^+ poly-Si NMOS gate devices are studied. It is observed that the I-V characteristics after hard-breakdown are determined by the filament cross-section formed through the emission of en-

ergy stored in the MOS capacitor before breakdown. An electro-thermal model is developed which is successful in explaining the measured post hard-breakdown I-V characteristics. The dependence on the physical parameters involved in the breakdown process is also examined. At very low power dissipation soft-breakdown may occur. The I-V characteristics after low power breakdown suggest that the conduction mechanism is asymmetric with respect to gate bias polarity. However the conduction mechanism after low power breakdown is still poorly understood.

Finally, in chapter 6 light emission measurements are performed on n^+ poly-Si NMOS gate devices after breakdown. These light emission measurements reveal important information about the physical properties of the link formed after breakdown.

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Nomenclature

symbol	description	unit
A	capacitor area	[cm^{-2}]
A	pre-exponential factor in the FN-tunneling expression	[A/MV^2]
A'	pre-exponential factor in the direct tunneling expression	[A/MV^2]
a	pre-power law factor in the soft-breakdown	
	I-V characteristics expression	[A/V]
B	exponential factor in the FN-tunneling expression	[cm/MV]
B'	exponential factor in the direct tunneling expression	[cm/MV]
b	power law factor in the soft-breakdown	
	I-V characteristics expression	[-]
C	capacitance per unit area	[F/cm]
C_{gate}	gate surface capacitance per unit area	[F/cm]
C_{MOS}	total capacitance of the MOS structure,	
	C_{MOS}=C_{ox}+C_{par} per unit area	[F/cm]
C_{ox}	oxide layer capacitance per unit area	[F/cm]
C_{par}	parasitic capacitance of the MOS structure per unit area	[F/cm]
C_{it}	interface trap capacitance	[$cm^{-2}eV^{-1}$]
C_{sub}	substrate surface capacitance per unit area	[F/cm]
C_t	heat capacity per unit volume	[$J/K{\cdot}cm^3$]
D_{it}	density of oxide interface traps	[$cm^{-2}eV^{-1}$]
D_{ot}	volume density of neutral electron traps in the oxide	[cm^{-3}]
$D_{ot,crit}$	critical volume density of neutral electron traps	
	in the oxide	[cm^{-3}]
D_{th}	thermal diffusivity of silicon	[cm^2s^{-1}]
E_c	electric field strength across the gate-substrate link	[V/cm]
E_{bd}	breakdown electric field	[MV/cm]
E_{ox}	electric field strength across the dielectric layer	[MV/cm]
f	occupation probability of the neutral traps in the oxide	[-]
H	heat generation per unit volume	[W/cm^3]
I_p	programming current	[mA]
I_s	stress current	[mA]
I_{bd}	current during breakdown of the gate oxide	[mA]
I_{cap}	capacitor discharge current during breakdown	
	of the gate oxide	[mA]
$I_{\mathcal{E}}$	optical intensity of the spectrum	[W/eV]
J_c	electron current density inside the gate-substrate link	[A/cm^2]
J_{DT}	Direct Tunneling current density	[A/cm^2]
J_{et}	Esaki-Tsu formula for tunneling current density	[A/cm^2]
J_{FN}	Fowler-Nordheim tunneling current density	[A/cm^2]

J_g	gate current density	[A/cm^2]
J_{in}	electron current density per unit film thickness flowing into a neutral trap in the oxide	[A/cm^3]
J_{IST}	Interface State Tunneling current density	[A/cm^2]
J_{MCT}	Minority Carrier Tunneling current density	[A/cm^2]
J_{out}	electron current density per unit film thickness flowing out of a neutral trap in the oxide	[A/cm^3]
J_{silc}^{ac}	transient component of the Stress-Induced Leakage Current density	[A/cm^2]
J_{silc}^{dc}	steady-state component of the Stress-Induced Leakage Current density	[A/cm^2]
J_{silc}	Stress-Induced Leakage Current density	[A/cm^2]
J_{stress}	electrical stress current density	[A/cm^2]
J_{VBT}	Valence Band Tunneling current density	[A/cm^2]
k	Boltzmann's constant (k=8.62$\cdot$ 10^{-5} eV/K)	[eV/K]
k_2	extinction coefficient (absorption) of the poly-silicon layer	[-]
L_{th}	dimension of the volume being heated during breakdown	[nm]
m	electron rest mass (m=9.11 $\cdot$ 10^{-31} kg)	[kg]
m_d	density-of-state mass in the gate material	[kg]
m^*	electron effective mass in SiO_2 (m^*=0.34 $\cdot$ m)	[kg]
n	the p-n junction quality factor	[-]
n_v	valley degeneracy in the gate material	[-]
$n_{1,2,3}$	refractive index of resp. air, poly-silicon and oxide layer	[-]
N_{poly}	electrically active doping concentration of gate	[cm^{-3}]
N_{sub}	substrate doping concentration	[cm^{-3}]
P	total electrical power	[W]
P_g	defect generation rate of neutral oxide traps	[cm^{-1}/C]
P_g(silc)	Stress Induced Leakage Current generation rate	[cm^2/C]
q	elementary charge (q=1.60 $\cdot$ 10^{-19} C)	[C]
Q	total charge stored on the capacitor	[C]
Q_{bd}	total injected electron fluence at breakdown	[C/cm^2]
Q_f	fixed oxide trapped charge	[cm^{-2}]
Q_g	gate charge per unit area	[C/cm^2]
Q_{inj}	total injected electron fluence during stress	[C/cm^2]
r_c	core radius of the breakdown site	[nm]
R_{bd}	total post breakdown resistance	[Ω]
R_c	resistance of the core of the breakdown site	[Ω]
R_l	total resistance of the gate-substrate link	[Ω]
$R_{s,tot}$	total spreading resistance of the gate-substrate link	[Ω]
$\vec{S}$	heat flux per unit area	[W/cm^2]
T_{amb}	ambient temperature	[°C]

T_e	effective electron temperature of the electrons	[°C]
T_{inj}	temperature during electrical stress	[°C]
T_L	lattice temperature of silicon	[°C]
T_{meas}	temperature during measurement	[°C]
T_{Si}	melting temperature of silicon	[°C]
T_{SiO_2}	melting temperature of silicon dioxide	[°C]
$T^*\cdot T_{in}$	transmission probability for tunneling into a neutral trap in the oxide	[-]
$T^*\cdot T_{out}$	transmission probability for tunneling out of a neutral trap in the oxide	[-]
$T^*\cdot T_{WKB}$	tunneling probability under the WKB approximation	[-]
t_{bd}	time to breakdown	[s]
t_{eff}	effective thickness over which the TAT tunneling current flows mainly	[nm]
t_{ox}	thickness of the dielectric oxide layer	[nm]
t_{poly}	thickness of the poly-silicon layer	[nm]
V_b	reverse breakdown voltage of the diode-antifuses	[V]
V_{bd}	voltage during breakdown of the gate oxide	[V]
V_c	voltage across the gate-substrate link	[V]
V_{fb}	flatband voltage	[V]
V_g	gate voltage	[V]
V_{gate}	voltage drop in the gate due to gate depletion	[V]
V_{ox}	voltage across the oxide	[V]
V_s	voltage at stress current I_s	[V]
V_{sub}	voltage drop in the Si-substrate due to band bending	[V]
V_t	threshold voltage	[V]
X_T	most favourable trap position in the oxide	[nm]
α	oxide quality parameter, $\alpha = \partial ln(D_{ot})/\partial ln(Q_{inj})$	[-]
β	oxide quality parameter, $\beta = \partial ln(D_{ot})/\partial ln(J_{stress})$	[-]
ϵ_{ox}	permitivity of SiO_2 (ϵ_{ox}=3.45 $\cdot$ 10^{-13} F/cm)	[F/cm]
ϵ_{si}	permitivity of Si (ϵ_{si}=1.05 $\cdot$ 10^{-12} F/cm)	[F/cm]
ϵ_r	relative permitivity	[-]
γ	quantum yield of electron impact ionization in Si	[-]
κ	thermal conductivity coefficient of silicon	[W/K·cm]
λ	wavelength of the light	[nm]
E_{th}	energy threshold marking the boundary between soft-breakdown and hard-breakdown	[J]
$\mathcal{E}_a$	effective anode barrier height, defined as $\mathcal{E}_a = \mathcal{E}_b + \mathcal{E}_{relax} - qE_{ox}\cdot t_{ox}$	[eV]
$\mathcal{E}_{act}$	temperature activation energy	[eV]
$\mathcal{E}_b$	energy barrier height at the Si/SiO_2 interface or *effective* barrier height to describe SILC as FN tunneling	[eV]

$\mathcal{E}_c$	conduction band edge of Si, SiGe or SiO_2	[eV]
E_{dis}	total energy released during breakdown of the MOS capacitor	[J]
$\mathcal{E}_f$	fermi level	[eV]
$\mathcal{E}_g$	band gap of Si, SiGe or SiO_2	[eV]
$\mathcal{E}_p$	photon energy	[eV]
$\mathcal{E}_{tr}$	trap energy level with respect to the conduction band of the SiO_2	[eV]
$\mathcal{E}_{tr}^*$	effective trap barrier height, defined as $\mathcal{E}_{tr}^*$=$\mathcal{E}_b$ - $qE_{ox}{\cdot}X_T$	[eV]
$\mathcal{E}_v$	valence band edge of Si, SiGe or SiO_2	[eV]
$\hbar$	reduced Planck constant ($\hbar$=6.58 $\cdot$ 10^{-16} eV·s)	[eV·s]
ϕ_{ms}	metal-to-semiconductor workfunction difference	[eV]
$\rho_{c,g,s}$	electrical resistivity of resp. the core material of the breakdown site, the polysilicon layer and the substrate	[Ω·cm]
σ_{in}	neutral trap capture cross section	[cm^2]
σ_{out}	neutral trap emission cross section	[cm^2]
τ_{bd}	discharging time of the capacitor during breakdown	[s]
τ_{th}	time necessity to reach thermal equilibrium during breakdown	[s]
$\mathcal{T}(\lambda)$	transmission factor for normal incidence light in a three layer system	[-]
χ	electron affinity	[eV]

List of acronyms

AC-SILC	transient component of Stress-Induced Leakage Current
AHI	Anode Hole Injection
BBT	Band to Band Tunneling
BGN	Band Gap Narrowing
CCD	Charged Coupled Device
CCS	Constant Current Stress
CMOS	Complementary Metal-Oxide-Semiconductor
C-V	Capacitance - Voltage
CVS	Constant Voltage Stress
DC-SILC	steady-state component of Stress-Induced Leakage Current
DHT	Direct Hole Tunneling
DOS	Density of States
DPROM	Diode Programmable Read Only Memory
DT	Direct Tunneling
EEPROM	Electrically-Erasable Programmable Read-Only Memory
EL	Electroluminescence
FN	Fowler-Nordheim
FOM	Figure Of Merit
HB	(Hard) Breakdown
HT	Hole Tunneling
HTAT	Trap Assisted Hole Tunneling
IC	Integrated Circuit
IR	Infrared
IST	Interface State Tunneling
ITAT	Inelastic Trap Assisted Tunneling
ITRS	International Technology Roadmap for Semiconductors
I-V	Current - Voltage
J-E	Current density - Electric field strength
J-V	Current density - Voltage
LPCVD	Low Pressure Chemical Vapor Deposition
MCT	Minority Carrier Tunneling
MOS	Metal-Oxide-Semiconductor
MOSFET	Metal-Oxide-Semiconductor Field Effect Transistor
NA	Numerical Aperture
NMOS	n-channel Metal-Oxide-Semiconductor
NVM	Non-Volatile Memory
OTP	One Time Programmable
PE	external Power Efficiency
P/E	Program/Erase
PL	Photoluminescence

PMOS	p-channel Metal-Oxide-Semiconductor
RTA	Rapid Thermal Anneal
RTN	Random Telegraph Noise
SB	Soft Breakdown
SIA	Semiconductor Industry Association
SILC	Stress-Induced Leakage Current
SRH	Shockley-Read-Hall
TAT	Trap Assisted Tunneling
TEM	Transmission Electron Microscopy
UV	Ultraviolet
VBT	Valence Band Tunneling
VRH	Variable Range Hopping
WKB	Wentzel-Kramers-Brillouin

Chapter 1

Introduction

"The complexity for minimum component costs has increased at a rate of roughly a factor of two per year. Certainly over the short term this rate can be expected to continue, if not increase. Over the longer term, the rate of increase is a bit more uncertain, although there is no reason to believe it will not remain nearly constant for at least 10 years. That means by 1975, the number of components per integrated circuit for minimum cost will be 65,000.

I believe that such a large circuit can be built on a single wafer."

Gordon E. Moore (1965) [1]

1.1 Introduction

The down-scaling of CMOS device dimensions has been the main stimulation for the continuing growth of the microelectronics industry over the past two decades. This trend of steady down-scaling was first formulated by Gordon E. Moore and is better known as Moore's law [1]. In 1965 G. Moore published a semi-log plot of the number of components on a silicon chip versus the date of first availability. The result was a straight line representing almost a doubling per year. In the later years, the rate relaxed somewhat to a doubling every 18 months. This is still the rate of today and it is expected to prevail for some time.

Metal-Oxide-Semiconductor Field Effect Transistors (MOSFETs) have been around quite some time now. The main success of these silicon based devices is, apart from the possibility to reduce their dimensions down to almost nanometer scale dimensions, the stable high quality silicon-silicon dioxide interface and their ability to interconnect millions to billions of devices on a single chip to form an integrated circuit (IC). The basic concept of the MOSFET and its operation was already formulated almost seventy years ago [2], even before the experimental discovery of the bipolar junction transistor on December 16, 1947 by J. Bardeen, W. H. Brattain and W. Shockley [3, 4] for which they later received the Nobel

Price. However, it was not until 1960 that the first silicon MOSFET was actually realized by Kahng and Atalla [5]. Ironically enough, the main reason for the rather late realization of a functioning MOSFET was that at those days it was very hard to realize an interface between a dielectric layer and a semiconductor which was of very high quality, a requirement for proper MOSFET action.

Today, after many generations of scaling the smallest feature in CMOS devices, that is the gate oxide thickness, is approaching atomic dimensions and fundamental limits imposed by quantum mechanics as off-state leakage current close in on technology. Tunneling currents larger than 1 A/cm^2 are predicted for SiO_2 dielectric layers of 1.5-2 nm thickness. Also the reliability of the gate oxide is becoming a major problem. If the scaling trend continues as predicted by the International Technology Roadmap for Semiconductors (ITRS) [6](see Table 1.1), SiO_2 may not be able to meet future reliability requirements under (normal) operation conditions [7].

Year of First Shipment Technology Node	**1997** 250 nm	**1999** 180 nm	**2002** 130 nm	**2005** 100 nm	**2008** 70 nm	**2011** 50 nm
Eq. Oxide thickness [nm]	4-5	3-4	2-3	1.5-2	<1.5	<1.0
Maximum Field [MV/cm]	4-5	5	5	>5	>5	>5
Supply (gate) voltage [V]	1.8-2.5	1.5-1.8	1.2-1.5	0.9-1.2	0.6-0.9	0.5-0.6

Table 1.1: Equivalent gate oxide thickness, electrical field and largest allowable gate voltage corresponding to the indicated year of first manufacture and technology generation. Data taken from the International Technology Roadmap for Semiconductors (1998 Update version) [6].

A fundamental understanding of the degradation mechanism of ultra-thin SiO_2 layers is therefore of great importance to allow accurate predictions of the reliability for future MOS devices under device operation conditions. Early in the next century state-of the-art MOSFETs will have 1-2 nm gate oxide thickness and will work at supply voltages of 1 V. The reliability of these devices is becoming a major issue. This creates some interesting research challenges to be solved in the near future. Some of them will be addressed in this thesis.

"Fortunately there is still some margin left in today's devices for perhaps a few generations, but how much longer can CMOS scaling continue ?"

1.2 Oxide degradation, reliability and lifetime

SiO_2 is still beyond any doubt one of the key factors in the success of CMOS-technology. The main reason for this is that for the reliable production of large-scale integrated circuits(ICs) it is necessarily to produce by compatible tech-

nologies both a semiconductor and an insulator that have superb electrical and mechanical properties. In fact, SiO_2 is a very good insulator with a very large bandgap of around $\mathcal{E}_g$=8-9 eV [8, 9] and it can be grown very easily and well-controlled on a Si-substrate.

The properties of the oxide-silicon system are fundamental to the performance of integrated-circuit devices and knowledge about these properties has been around for quite a long time know. At present, SiO_2 layers as thin as 1.5 nm can already be made and are used as a gate dielectric in a fully functioning MOSFET with a gate length of 0.1 μm [10, 11]. This also displays some of the most powerful properties of SiO_2, namely its scalebility and process integration capabilities. Nevertheless SiO_2 is not perfect and still suffers from some degradation. Aggressive down-scaling of the gate oxide thickness for future MOS devices however requires that, among other concerns, the gate oxide can still meet requirements for reliability. A fundamental understanding of the degradation mechanism of SiO_2 is therefore of great importance to allow accurate predictions of the reliability for future MOS devices at device operation conditions.

Gate oxide reliability has always been a major issue in determining the feasibility of MOS devices. Especially the reliability of ultra-thin gate dielectrics (t_{ox} <5 nm) is of increasing concern because of the significant direct tunneling currents flowing during normal device operation. The exponentially increase in tunnel current with decreasing oxide thickness will increase the standby power and seriously degrade the gate oxide reliability at operation conditions if the gate voltage is not simultaneously reduced sufficiently. This direct tunneling(DT) current poses a serious problem onto the further down-scaling of the gate oxide thickness for sub-100 nm feature-size technologies. If the scaling trend continues, SiO_2 may not be able to meet future reliability requirements [7, 6]. This means that another material with higher reliability and lower standby tunneling current will be needed [1].

Ultra-thin gate oxide reliability is therefore a major research topic, but in spite of the large amount of knowledge already gathered on this subject a number of issues are still not resolved. Gate oxide reliability was studied mainly for n-doped polycrystalline silicon (poly-Si) gate material up till now. With the down-scaling of the gate oxide thickness below 10 nm, p^+ poly-Si gate electrodes have been proposed for deep sub-micron gates to replace n^+ poly-Si gates. The main reason for this is that n^+ gate p-channel devices need an additional p-type implantation in the Si-substrate for threshold voltage adjustment. When a voltage is applied between the source and drain it is observed that the minimum in potential barrier is no longer at the surface indicating a buried channel operation [12]. However, p^+ gate p-channel devices do not require an additional implant for threshold

[1] To overcome this problem, the Semiconductor Industry Association (SIA) mentions high-ϵ dielectrics like Ta_2O_5 as a possible candidate to replace SiO_2 in sub-100nm feature-size technologies, which should enter production around the year 2006 (1997 version) [6].

voltage adjustment and thus remains a surface channel device.

Surface channel pMOSFETs with p^+ poly-Si gate have several advantages over conventional n^+ poly-Si gate buried-channel pMOSFETs, such as reduced short-channel effects and improved turn-off characteristics [12]. Therefore, for CMOS devices with ultra-thin gate oxides, p^+ gates have been proposed for p-channel MOSFETs to convert the buried channel operation to surface channel operation.

The degradation of p^+ gate devices with ultra-thin gate oxides is therefore also a major concern. However, before studying the degradation of p^+ gate devices it may be instructive to recall the most important models for explanation of oxide degradation as reported in literature and to review the different stages in the breakdown process.

1.3 Physical mechanisms of oxide degradation

In literature, many models have been suggested in order to explain the physical mechanism of oxide degradation under electrical stress conditions. A common assumption in all these models is that if some parameter reaches a critical value it triggers the breakdown of the oxide. The three most prevailing models reported in literature are :

1. *Electric Oxide Field model*

   According to this thermodynamic model [13, 14, 15, 16], the electric field itself induces sufficient damage in the oxide due to local field enhancement to cause electron trap generation. Since this model is solely based on the applied electrical field, it means that the electron flux does not influence the oxide degradation at all. This model is therefore commonly referred to as the E_{ox}*-model*. It has however been observed by Degraeve *et al.* [17] that both the electron fluence and the electric field determines the oxide breakdown. It was shown that electron trap generation is identical for all stress fields and that the electric field merely acts as an acceleration factor for the degradation process. This strongly suggests that the breakdown process is current driven, which means that the time-to-failure data should show a $1/E_{ox}$ dependence due to Fowler-Nordheim (FN) current conduction. This is known as the *1/*E_{ox} *model* and will be explained next. However it should be noted that there are also reports which indicate that the E_{ox}*-model* gives a better fit to long-term and low-field data than the *1/*E_{ox} *model* [18, 19]. These data suggests strongly that it is field, not current, which causes the time-dependent degradation of the oxide.

Figure 1.1: Schematic representation of Anode Hole Injection (AHI) model.

2. *Anode Hole Injection model (AHI)*

   In the Anode Hole Injection model(AHI) [20, 21, 22, 23, 24] the injected electrons gain kinetic energy as they travel through the conduction band of the SiO_2 layer. Upon reaching the anode these high-energetic electrons release part of their energy as they fall back to the conduction band in the anode. Thereby having a probability of creating a *hot-hole* which can tunnel back into the oxide (see Fig. 1.1). These holes are suspected to damage the oxide layer, i.e. creating electron traps and will eventually trigger the breakdown process as soon as a critical hole fluence is reached. This model is commonly referred to as the *$1/E_{ox}$ model*, since the time-to-failure data should show a $1/E_{ox}$ dependence due to Fowler-Nordheim (FN) current conduction. This model assumes that trap generation is directly linked to hole generation, since holes are needed to create traps in the oxide. Indeed, a unique relationship between hole fluence and electron trap generation is found, independent of stress field and oxide thickness [17]. Furthermore, it was demonstrated that breakdown in thin oxide layers occurs as soon as a critical density of (neutral) electron traps in the oxide is reached.

   According to Schuegraf *et al.* [22] the AHI model proves to be valid for a large thickness range varying between 2.5 nm and at least 13 nm and can predict Q_{bd} and t_{bd} behavior for low oxide voltages down to 2.4 V.

However, DiMaria *et al.* [25, 26, 27] observed that anode hole injection is important, but only for gate voltages larger than $V_g \approx 7.6$ V. They observed a threshold energy for trap creation of about 2.3 eV with respect to the bottom of the oxide conduction band, while they stated that for anode hole injection a threshold energy of at least 5 eV is needed. So they concluded that degradation of the gate oxide is not related to *hot-holes* but to hydrogen-induced defects, as will be explained in the next model.

3. *Hydrogen-release model*

   This model is very similar to the AHI injection model. According to the hydrogen release model oxide degradation is due to H^+ instead of holes [28, 29, 26]. A large amount of hydrogen is present at the interface, since passivation of the Si/SiO_2 interface defects with hydrogen is performed in standard CMOS-processing. In this model the energy of the high-energetic electrons is released by releasing hydrogen from the Si/SiO_2 interface. When the H^+ enters the oxide it is believed to create damage. This is supported by experimental evidence. DiMaria *et al.* [26, 30, 31] demonstrated that SiO_2 degrades in a similar manner when exposed to H^+. From these studies it was also concluded that the generation of neutral oxide traps in thin oxides is the dominant cause of oxide degradation and will eventually lead to oxide breakdown. So electron trap creation can be observed as soon as the electron energy exceeds 2 eV with respect to the bottom of the oxide conduction band. However, it has been observed that in the direct tunneling(DT) regime, where the electrons do not enter the oxide conduction band, defect generation still occurs.

The E_{ox} versus $1/E_{ox}$ controversy has continued for many years now, since both models can fit the time-to-failure data rather well over the measured (limited) field ranges. Although the latter two models are the most prevailing ones in explaining the degradation of the oxide, no model has been proven to be unambiguously correct up until now.

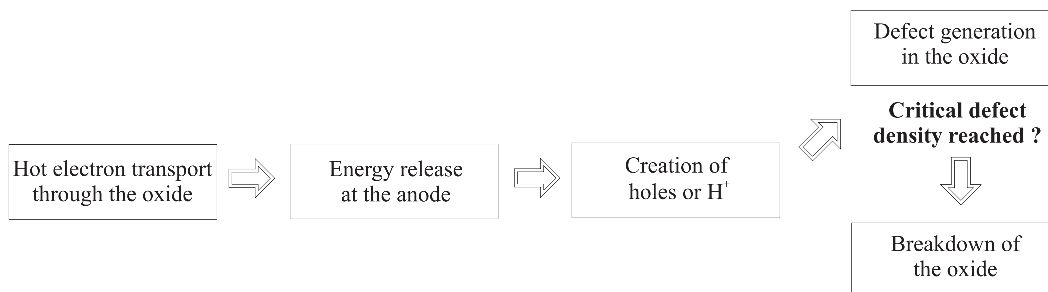

Figure 1.2: Schematic illustration of gate oxide breakdown due to positive species (holes or H^+).

Nevertheless, from the models above it can be concluded that the degradation mechanism of the oxide is most likely related to positive species as is illustrated in Fig. 1.2 and that breakdown occurs as soon as a critical neutral electron trap density $D_{ot,crit}$ is reached.

1.4 Problem definition: Basic principles

In the previous section it was stated that oxide degradation proceeds with the generation of neutral electron traps in the bulk of the oxide. In this section the different stages of oxide degradation as a function of the density of generated electron traps in (ultra-)thin gate oxides is briefly evaluated. Up until a few years ago the focus was mostly on the occurrence of defect-related i.e. *extrinsic* breakdown, while *intrinsic* breakdown never posed any real reliability problem. However, with the further down-scaling of the oxide thickness to only a few nanometers, intrinsic related breakdown has become a major reliability problem. Since this intrinsic related breakdown eventually limits the scaling of the gate oxide thickness for future generation MOS devices it seems natural to investigate its properties in more detail. First however a brief overview of the different stages of oxide degradation is given.

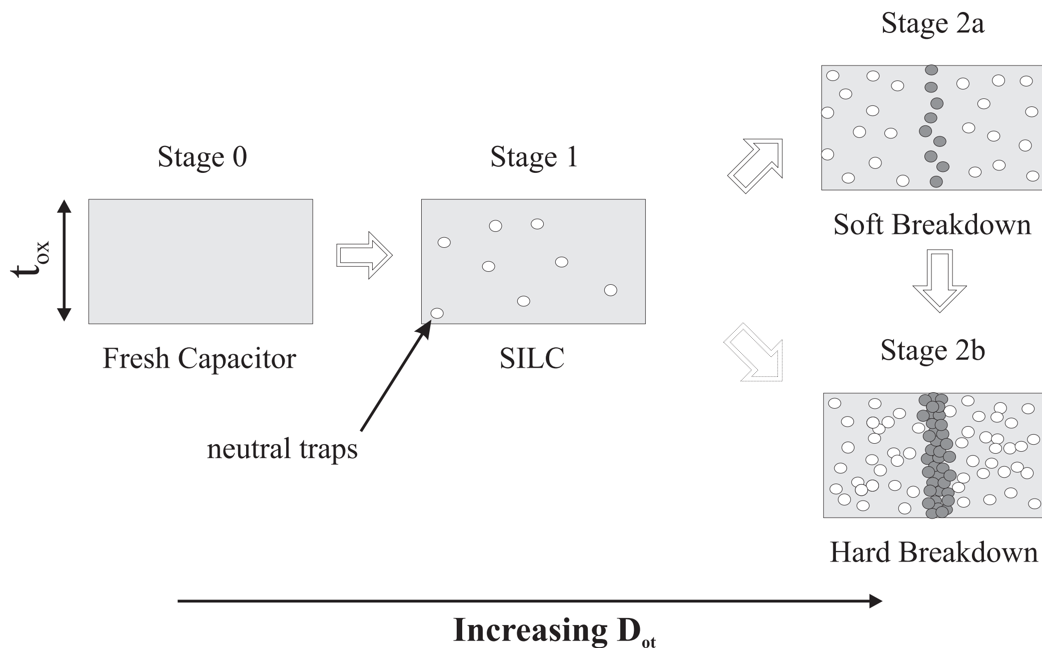

Figure 1.3: Schematic illustration of oxide degradation. Roughly 3 stages can be distinguished, which are 1) SILC, 2a) soft breakdown and 2b) (hard) breakdown.

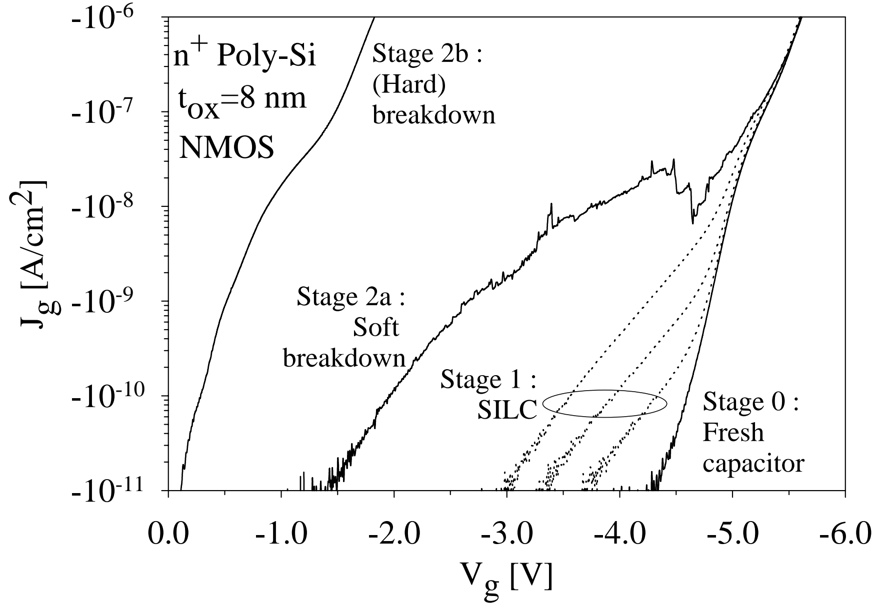

Figure 1.4: J_g-V_g measurements of n^+ poly-Si NMOS capacitors on 8 nm gate oxide thickness showing the different stages of oxide degradation, which are 1) SILC, 2a) soft breakdown and 2b) (hard) breakdown.

Electrical stressing the oxide leads to continuous degradation of its insulating properties. Roughly 3 different stages of oxide degradation can be distinguished, which are depicted in Fig. 1.3.

The occurrence of these stages depend on the density of (neutral) electron traps present in the bulk of the oxide D_{ot}. The current-voltage(I-V) characteristics which belong to each of these stages are displayed in Fig. 1.4.

- **Stage 1: Stress-Induced Leakage Current(SILC)**

  In sub-10 nm oxides high field stressing of the oxide generates a low field leakage current, which is referred to as Stress-Induced Leakage Current(SILC). Stress-Induced Leakage Current or SILC is the increase in low-level leakage through thin silicon dioxide(SiO_2) layers after the oxide has been subject to high electrical-field stressing. This phenomenon was first observed in the early eighties by Maserjian *et al.* [32] and will be treated in more detail in chapter 3.

- **Stage 2a: Soft breakdown(SB)**

  At a higher amount of neutral traps in the oxide, Soft-Breakdown(SB) may occur. Soft, quasi, early, non-destructive breakdown or B-mode SILC is the sudden increase in gate current density at low fields on top of the SILC current to extremely high current levels. It was first observed by Lee *et al.* [33]. This sudden increase in gate current is accompanied by an increase in gate signal noise. Soft breakdown is (only) observed when the power dissipation after breakdown is limited as happens for instance in ultra-thin oxides and small area MOS capacitors [34, 35]. An important difference between SILC and soft breakdown(SB) is that the conduction mechanism of SILC is uniform, i.e. it occurs over the whole capacitor area, while SB conduction occurs at a localized area.

  The question however whether soft breakdown corresponds to a real oxide failure is still to be resolved [36]. For ultra-thin oxides it has been reported that the (soft)breakdown of such oxides is difficult to detect, since the post breakdown I-V characteristics are not significantly different from the initial I-V characteristics. The conduction mechanism after breakdown is therefore an important issue and will be treated in more detail in chapter 5.

- **Stage 2b: (Hard) breakdown(HB)**

  Further stressing of the gate oxide will eventually lead to termination of the oxide degradation by the occurrence of breakdown of the oxide. This is the final stage of oxide breakdown, where thermal run-away effects lead to a complete loss of insulating properties of the oxide. Hard breakdown occurs if the power dissipation during breakdown is high enough to locally melt the oxide over a small volume centered around the point of breakdown. So hard breakdown is often observed in large area MOS capacitors and thick oxides. It is believed that breakdown is characterized by a maximum amount of electron traps in the gate oxide $D_{ot,crit}$, which is known as the critical defect density at breakdown [17, 7].

  Oxide breakdown can be characterized by two parameters, the amount of time which is stressed before the device breaks down and the amount of charge fluence which passed through it. The first is the time-to-breakdown t_{db} and the second the charge-to-breakdown Q_{bd}.

  The definition of time-to-breakdown is straightforward, while the charge-

to-breakdown is defined by Eq. 1.1 as [37, 38] :

$$Q_{bd} = \int_0^{t_{bd}} J_g(t)\mathrm{d}t \tag{1.1}$$

The charge-to-breakdown is a well-known and widely-used tool to evaluate the gate oxide reliability of MOS structures and study the influence of processing conditions on the Q_{bd}, such as anneal temperature, gate materials and gate implants. The Q_{bd} can be related to the electron trap density D_{ot}, where Q_{bd} is reached as soon as D_{ot}=$D_{ot,crit}$. This implies that the density of neutral traps present in the bulk of the oxide D_{ot} and the generation rate of them (P_g=$\Delta D_{ot}/\Delta Q_{inj}$) are important parameters for gate oxide reliability.

After breakdown a link of electron traps is formed in the gate oxide which connects the gate with the substrate. The post (hard) breakdown I-V characteristics of carefully designed MOS capacitors are studied in chapter 5 as well.

1.5 Research objectives

In this thesis the conduction mechanism, oxide degradation and breakdown of (ultra-)thin gate oxides with n^+ and p^+ gates, which are subject to electrical stress are studied. The aim is to obtain a better fundamental knowledge about oxide degradation and breakdown in both p^+ and n^+ gate devices, which can eventually be used to accurately predict the reliability of CMOS devices with ultra-thin gate oxides at operation conditions.

Recently a larger tunnel barrier height and a different conduction mechanism for gate injection (-V_g) have been proposed for p^+-poly gate devices [39, 40, 41]. This might have a large impact on the reliability of future CMOS devices with p^+ gates. However a complete understanding is still not available. The research objectives of this thesis can essentially be split up into four parts.

First the conduction (I-V), degradation mechanism (SILC) and time-to-breakdown t_{bd} of (ultra-)thin gate oxides is investigated. P^+ and n^+-gates with poly silicon (poly-Si) and poly Silicon-Germanium(poly-$Si_{0.7}Ge_{0.3}$) are used to study the influence of gate workfunction on gate current and SILC current. Poly-SiGe is chosen since its allows modification of the workfunction of the gate for p^+ gate devices. Moreover, it is fully compatible with (poly-)Si technology.

Fig. 1.5 displays the energy band diagram of Si, SiGe and Ge. From Fig. 1.5 it can be observed that Si(χ=4.05 eV) and Ge(χ=4.00 eV) have comparable electron affinity χ. However, the bandgap of Ge($\mathcal{E}_g$=0.66 eV) is much smaller

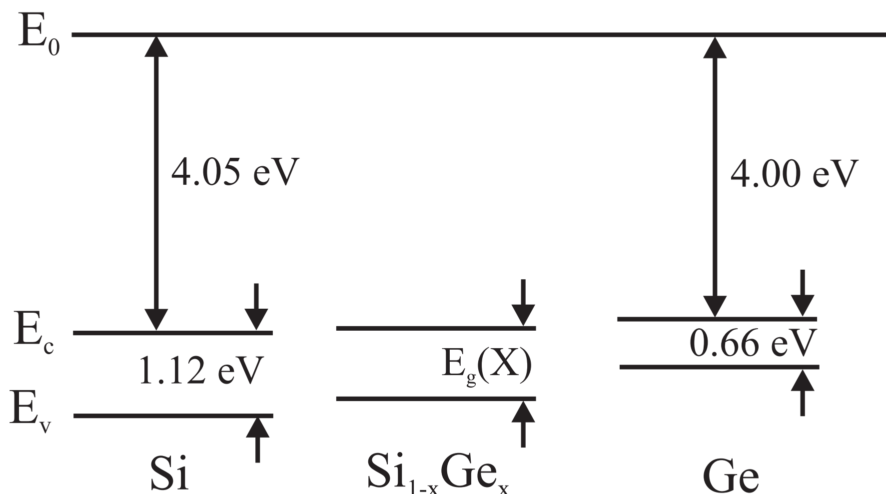

Figure 1.5: Energy band diagram of Si, SiGe and Ge. It can be observed that the bandgap of SiGe can be tuned by changing the Ge fraction.

than Si($\mathcal{E}_g$=1.12 eV). This allows modification of the valence band edge position of the gate by varying the Ge fraction x in poly-$Si_{1-x}Ge_x$ gate devices and therefore influence the gate workfunction for p^+ gate devices. This workfunction engineering by exploiting the difference in valence band edge can in principle be applied for all Ge contents. Moreover, poly-$Si_{1-x}Ge_x$ is a promising alternative to poly-Si as a gate material due to its process compatibility and favorable electrical properties, such as higher dopant activation, lower sheet resistance, superior hole mobility and tunable work function [42, 43, 44, 45, 46, 47]. However the gate oxide reliability of poly-SiGe gate devices has not been studied in detail yet.

The impact of gate current and gate workfunction on the reliability of the gate oxide is also briefly investigated. The physical models for oxide degradation presented in the previous section will be critically reviewed based on our findings.

Next, the post-breakdown I-V characteristics of n^+ poly-Si NMOS gate devices are studied. The I-V characteristics after breakdown can give important information of the breakdown process, which will eventually lead to a better understanding of the degradation mechanism leading to (catastrophic) breakdown.

Finally, light emission measurements are performed on the post breakdown I-V characteristics of n^+ poly-Si NMOS gate devices. These light emission measurements may also reveal important information about the physical properties of the link formed after breakdown.

1.6 Outline of this thesis

In this thesis the oxide degradation mechanisms of CMOS devices with (ultra)-thin gate oxides is studied. The conduction mechanism, oxide degradation and breakdown of (ultra-)thin gate oxides with n^+ and p^+ poly-Si and poly-SiGe gates have been studied.

The outline of this thesis and main conclusions of every chapter are given in more detail below.

Chapter 2
In this chapter the C-V and I-V characteristics of NMOS and PMOS capacitors are studied. P^+ and n^+-gates with poly silicon(poly-Si) and poly Silicon-Germanium(poly-$Si_{0.7}Ge_{0.3}$) were used to study the influence of gate workfunction on gate current. C-V_g measurements on p^+ gate devices show a shift of the flatband voltage from V_{fb}=0.82 V(poly-Si) to V_{fb}=0.60 V(poly-SiGe) which is caused by a shift in the valence band position of the gate. For p^+ gate devices the J_g-E_{ox} characteristics depend on gate material and gate bias polarity. The onset of conduction at -V_g occurs at a significantly higher oxide field than for +V_g condition. A new model based on Minority Carrier Tunneling(MCT) from the gate is proposed for the J_g-E_{ox} characteristics of p^+ gate devices under gate injection conditions (-V_g). Furthermore, high frequency (10 kHz) C-V_g curves of p^+ poly-Si gate devices on 4.8 nm oxide thickness show no sharp onset of gate inversion in the p^+ poly-Si gate at -V_g. This is most likely caused by carrier tunneling out of the gate which occurs at a higher rate than that of carrier generation under MCT injection conditions. For very thin oxides (t_{ox} < 4 nm) another contribution to the I-V characteristics at -V_g is observed. Carrier separation measurements indicate that a hole current is flowing from the source/drain to the gate in the low voltage regime. This current is presumably due to holes which can tunnel (via traps) from the hole inversion layer in the substrate to the gate. Furthermore, this hole current increases strongly with decreasing oxide thickness and can be important for the degradation and reliability of ultra-thin oxides.

Chapter 3
In this chapter the Stress-Induced Leakage Current(SILC) characteristics of NMOS and PMOS capacitors are studied. P^+ and n^+-gates with poly silicon(poly-Si) and poly Silicon-Germanium(poly-$Si_{0.7}Ge_{0.3}$) were used to study the influence of gate workfunction on the SILC current. For n^+ gate devices, symmetric SILC with gate bias polarity is observed. No significant difference in SILC characteristics between the n^+ poly-SiGe and poly-Si reference devices is observed. For p^+-poly gate devices, asymmetric SILC (gate bias polarity) and reduced SILC

for p^+ poly-$Si_{0.7}Ge_{0.3}$ is observed. The stress injection bias polarity dependence of p^+ gate devices is also studied. It is found that the amount of traps generated per unit of injected charge is approximately 10 times higher for injection of stress from the gate compared to substrate injection of stress. For very thin oxides (t_{ox} <4 nm) the SILC current at -V_g and at low voltages is dominated by hole tunneling from the substrate to the gate. This current is interpreted as trap assisted hole tunneling (HTAT). The effect of fluorine(F) on the SILC characteristics of n^+ poly-Si gate devices has also been studied. A small amount of F suppresses the generation of new oxide traps under high field electron injection, which leads to reduced SILC. At excessive F doses an increase of SILC is observed. Finally, a two-step tunneling model was developed to evaluate the SILC current under FN, MCT and VBT injection conditions. It is shown that this model successfully describes the experimental I-V characteristics for both n^+ and p^+ poly gate devices under substrate as well as gate injection conditions.

Chapter 4
In this chapter results are presented of the time-to-breakdown (t_{bd}) of both n^+ and p^+ poly-Si gate devices on ultra-thin gate oxides (t_{ox} <5 nm). For the 2.5 nm oxides (n^+ poly-Si gate) a decrease in t_{bd} of nearly 4 orders of magnitude is observed when the ambient temperature is increased from 25°C to 200°C. Also a weak gate bias polarity dependence is observed with respect to time-to-breakdown if t_{bd} is plotted as a function of the gate voltage V_g. For p^+-poly Si gate devices an increase of t_{bd} with increasing gate anneal RTA temperature, i.e. increasing active gate doping, is observed, which is most likely related to a decrease in tunneling current during stress at a fixed gate voltage. This indicates that both the total energy release at the anode and the electron fluence are important parameters for t_{bd} of ultra-thin oxides. It appears that constant voltage stress (CVS) is also preferable for p^+-poly gate devices on sub-5 nm gate oxides.

Chapter 5
In this chapter results are presented of the post-breakdown electrical characteristics of n^+ poly-Si MOS capacitors with 8 nm and 10 nm thick oxides. The dependence of the post breakdown I-V characteristics on capacitor area, substrate doping and breakdown power were evaluated. Depending on gate and substrate doping polarity, different post breakdown characteristics were observed. For n^+-poly/oxide/n^+-substrate MOS capacitors the post breakdown characteristics resemble that of a resistance. The value of the resistance is determined by the filament cross-section formed through the emission of energy stored in the MOS capacitor before breakdown. For n^+-poly/oxide/p-substrate MOS capacitors the I-V characteristics after high power breakdown resemble that of a nanometer size diode with a high I_{on}/I_{off} ratio. The breakdown voltage of these diodes is high due to the gate action. For low power breakdown the diodes become

"non-ideal" and their "non-ideality" depends strongly on stress current. The conduction mechanism after low power breakdown is still not well understood. The I-V characteristics of these devices were also measured at variable temperature to study the dominant conduction processes after breakdown. At very low power dissipation soft-breakdown may occur. This shows that soft-breakdown does not only occur in sub-5 nm oxides, but can also be enforced in 8 nm gate oxide thickness structures if the total energy during breakdown is limited.

Chapter 6

In this chapter results are presented of the spectrally resolved absolute measurements of the electroluminescence of silicon nanometer-scale diode-antifuses. The emission spectrum of the diode-antifuses is measured in the energy range of 1.4 - 2.8 eV at different forward and reverse currents. The dependence of the emission intensity on the current was evaluated to study the dominant emission processes. Previously proposed mechanisms for avalanche emission from conventional silicon p-n junctions are discussed in order to understand the origin of the emission. With the diode-antifuses biased in reverse breakdown, we measured (after correction for absorption and interference in the poly-Si layer) a nearly wavelength-independent emission extending from UV to IR corresponding with an average electron temperature between T_e=5000-6000 K. This agrees with previous data of conventional avalanche p-n junctions. For the forward biased condition the spectrum reflects the silicon band structure due to emission from electron-hole recombinations. A lattice temperature at the emission site of about T_L=400 K was estimated. Finally, the stability of the diode-antifuses has been tested. Results indicate that the diode-antifuse is basically a high quality device. The external power efficiency has been calculated to be PE=$2.0 \cdot 10^{-6}$% in the energy range of 1.4 - 2.8 eV. The optical power per unit area is rather high and can reach values up to 0.1-10 W/cm^2. Furthermore, due to its nanometer-scale dimensions, very high electrical fields and current densities are possible at low power consumption. This makes the diode-antifuse an excellent candidate for emitter elements in Si-based optical interconnect schemes and for optical sensors and actuator systems.

Chapter 2

The poly-Si and poly-SiGe CMOS I-V characteristics

In this chapter the C-V and I-V characteristics of NMOS and PMOS capacitors are studied. P^+ and n^+-gates with poly silicon(poly-Si) and poly Silicon-Germanium(poly-$Si_{0.7}Ge_{0.3}$) were used to study the influence of gate workfunction on gate current. C-V_g measurements on p^+ gate devices show a shift of the flatband voltage from V_{fb}=0.82 V(poly-Si) to V_{fb}=0.60 V(poly-SiGe) which is caused by a shift in the valence band position of the gate. For p^+ gate devices the J_g-E_{ox} characteristics depend on gate material and gate bias polarity. The onset of conduction at -V_g occurs at a significantly higher oxide field than for +V_g condition. A new model based on Minority Carrier Tunneling(MCT) from the gate is proposed for the J_g-E_{ox} characteristics of p^+ gate devices under gate injection conditions (-V_g). Furthermore, high frequency (10 kHz) C-V_g curves of p^+ poly-Si gate devices on 4.8 nm oxide thickness show no sharp onset of gate inversion in the p^+ poly-Si gate at -V_g. This is most likely caused by carrier tunneling out of the gate which occurs at a higher rate than that of carrier generation under MCT injection conditions. For very thin oxides (t_{ox} < 4 nm) another contribution to the I-V characteristics at -V_g is observed. Carrier separation measurements indicate that a hole current is flowing from the source/drain to the gate in the low voltage regime. This current is presumably due to holes which can tunnel (via traps) from the hole inversion layer in the substrate to the gate. Furthermore, this hole current increases strongly with decreasing oxide thickness and can be important for the degradation and reliability of ultra-thin oxides.

2.1 Introduction

The integrity of ultra-thin oxides is a major concern for further down-scaling of the gate oxide thickness. Stress-Induced Leakage Current(SILC), Soft-Breakdown (SB) and the increase of temperature acceleration of time-to-breakdown(t_{bd}) seriously limits the down-scaling of gate oxide thickness [7, 48, 49]. Gate oxide

reliability has been studied mainly for n^+-doped poly-Si gate devices. For CMOS devices with ultra-thin gate oxides, p^+ gates have been proposed for p-channel MOSFETs to convert the buried channel operation to surface channel operation [12]. The degradation of PMOS gate dielectric with p^+ gates is therefore also a major concern.

It should be noted that recently first reports on the conduction(I-V) and degradation mechanisms in p^+ gate devices were presented [50, 39, 40, 41]. However a complete understanding is still not available. It was reported that for p^+ gate devices the J_g-E_{ox} characteristics depend on gate bias polarity. For substrate injection conditions ($+V_g > 0$) the conduction mechanism is simply Fowler-Nordheim(FN) tunneling. However for gate injection conditions ($-V_g < 0$) the onset of conduction occurs at a significantly higher oxide field than for $+V_g$.

Schuegraf *et al.* [50] still assumed that the conduction mechanism in p^+ gate devices at $-V_g$ can be described by Fowler-Nordheim(FN) tunneling. However, if FN tunneling with a barrier height of $\mathcal{E}_b$=3.1 eV is assumed as the conduction mechanism for p^+ gate devices under gate injection conditions, an *unrealistic* voltage drop of $|V_{ox}|=|V_g|-2.2$ V is needed to fit their data. Ogier *et al.* [39] and Salm *et al.* [40] presumed that the conduction mechanism of their p^+ gate devices at $-V_g$ is caused by tunneling of electrons from the valence band of the gate, i.e. Valence Band Tunneling(VBT). They assumed that VBT tunneling can be described by a FN tunneling expression with an increased barrier height of $\mathcal{E}_b=3.1+\mathcal{E}_g=4.2$ eV. The slope of their Fowler-Nordheim plot indeed indicates that the barrier height $\mathcal{E}_b$ is larger ($\approx$4.4 eV) compared to n^+ gate devices. However, they did not account for the much larger pre-exponential factor in the FN-tunneling expression, which can be derived from the intersection point with E_{ox}=0. From this the barrier height $\mathcal{E}_b$ can also be calculated, which results in an *unrealistic* low barrier height of $\mathcal{E}_b \ll 4.2$ eV. This will be explained later on. So one might ask the question which tunneling mechanism dominates at $-V_g$ in p^+ gate devices.

In this chapter the C-V and I-V characteristics of both NMOS and PMOS capacitors are studied. P^+ and n^+-gates with poly silicon(poly-Si) and poly Silicon-Germanium(poly-$Si_{0.7}Ge_{0.3}$) were used to study the influence of gate workfunction on gate current. It will be shown that for p^+ gate devices the J_g-E_{ox} characteristics depend on gate material and gate bias polarity in contrast to n^+ gate devices, which are almost symmetrical with respect to gate bias polarity. The J-E_{ox} characteristics of p^+ poly-Si PMOS capacitors on 4.8 nm gate oxide with different gate RTA anneal temperatures are also studied for $-V_g$ injection conditions. A shift to higher E_{ox} is observed with increasing gate RTA anneal temperature. A new model based on Minority Carrier Tunneling(MCT) from the gate is proposed for the I-V characteristics of p^+ gate devices under gate injection conditions which can explain the observations.

The basic outline of this chapter is as follows. First in section 2.2 the experimental procedures for the fabrication of the CMOS devices is described. After this, in section 2.3 the C-V_g characteristics of these NMOS and PMOS capacitors are evaluated. The C-V_g curves are also used to make the conversion from measured gate voltage V_g to oxide field strength E_{ox}, so the conduction mechanism of the n^+ and p^+ gate devices can be properly evaluated. Next, the charge carrier transport through (ultra-)thin gate oxides will be briefly evaluated in section 2.4. In section 2.4.1 the I-V characteristics of NMOS and PMOS capacitors with p^+ and n^+ poly silicon(poly-Si) and poly Silicon-Germanium(poly-$Si_{0.7}Ge_{0.3}$) gates will be presented and discussed in detail. The impact of different gate RTA anneal temperature on the J-E_{ox} characteristics of PMOS capacitors with p^+ poly-Si gates is studied in this section as well. Finally, in section 2.4.2 a model based on Minority Carrier Tunneling(MCT) from the gate is proposed as the conduction mechanism of our p^+ gate devices under gate injection conditions (-V_g).

2.2 Experimental Procedures

The samples prepared for this study can essentially be split up in two sets. The first set consists of NMOS and PMOS capacitors with n^+ and p^+ poly-Si and poly-$Si_{0.7}Ge_{0.3}$ gates on 5.6 nm oxide thickness. They are used to study the influence of gate workfunction on the gate current.

The second set consists of p^+ poly-Si PMOS transistors with 4.8 nm oxide thickness and various gate RTA anneal temperatures, which were used to investigate the effect of gate RTA anneal temperature on the J-E_{ox} characteristics of p^+ poly-Si gate devices.

- **Set 1**
  n^+ poly-Si/SiGe NMOS capacitors were fabricated on 10 Ω-cm p-type silicon substrates. A high quality gate oxide with 5.6 nm thickness (ellipsometric) was grown in N_2 diluted dry oxygen. Undoped poly-Si and poly-$Si_{0.7}Ge_{0.3}$ layers (200 nm thick) were deposited using a LPCVD system [44]. Gate doping was done by 40 keV, $5.0{\cdot}10^{15}$ cm^{-2} As^+ implant followed by a Rapid Thermal Anneal (RTA) at 1000°C for 20 seconds in N_2 ambient.

  p^+ poly-Si/SiGe PMOS capacitors were fabricated on 10 Ω-cm n-type silicon substrates. A high quality gate oxide with 5.6 nm thickness (ellipsometric) was grown in diluted dry oxygen. Undoped poly-Si and poly-$Si_{0.7}Ge_{0.3}$ layers (200 nm thick) were deposited using a LPCVD system [44]. Gate doping was done by 20 keV, $2.5{\cdot}10^{15}$ cm^{-2} BF_2^+ implant followed by a furnace anneal at 850°C for 30 minutes.

- **Set 2**
  Additionally p^+ poly-Si PMOS transistors were fabricated on 10 Ω-cm n-type silicon substrates. Channel implants were done using P^+, followed by a 50 keV V_t implant with As^+. A high quality gate oxide with 4.8 nm thickness (ellipsometric) was grown in dry oxygen at 850°C. Undoped poly-Si (200 nm thick) was deposited amorphously at 545°C and pre-doped with $1.0 \cdot 10^{14}$ cm^{-2} P^+ before etching. Additional implants in the gate are 1 keV, $3.0 \cdot 10^{14}$ cm^{-2} B^+ tips implant, a 50 keV, $8.0 \cdot 10^{12}$ cm^{-2} P^+ pocket implant and a 20 keV $2.5 \cdot 10^{15}$ cm^{-2} BF_2^+ LDD implant. The gate RTA anneal temperature was done for 20 seconds with increasing temperature of 990°C, 1010°C, 1030°C, 1050°C and 1070°C.

2.3 C-V measurements on poly-Si and poly-SiGe MOS capacitors

In this section quasi-static and high frequency(10 kHz) C-V measurements are performed on both n^+ and p^+ poly-Si and poly-$Si_{0.7}Ge_{0.3}$ MOS capacitors with 4.8 and 5.6 nm gate oxide thickness. The C-V_g curves are used to accurately determine the band bending in the gate (gate depletion) and the oxide field strength over the oxide E_{ox}, as a function of the gate voltage. The conversion from measured gate voltage V_g to oxide field strength E_{ox} is done by integration of the measured quasi-static C-V_g curves, as will be shown below. This procedure will also correct for gate depletion, band bending in the mono-Si substrate, finite thickness of inversion/accumulation layers (including quantum effects) etc., since they all are measured as a function of the gate voltage in the C-V_g curve.

The measured total capacitance C is the series combination of C_{ox}, C_{gate} + $C_{it,gate}$ and C_{sub} + $C_{it,sub}$ and is defined by :

$$C(V_g) = \frac{\partial Q_g}{\partial V_g} \tag{2.1}$$

$$\frac{1}{C} = \frac{1}{C_{gate} + C_{it,gate}} + \frac{1}{C_{ox}} + \frac{1}{C_{sub} + C_{it,sub}} \tag{2.2}$$

Where Q_g is the charge at the gate surface, C is the measured capacitance, C_{gate} is the gate surface capacitance, C_{ox} the oxide layer capacitance and C_{sub} is the Si substrate surface capacitance, all per unit area. $C_{it,gate}$ and $C_{it,sub}$ are respectively the interface trap capacitance at the poly-Si/SiO_2 and the SiO_2/Si interface per unit area.

Furthermore, it is assumed that the density of oxide interface traps at both interfaces $D_{it,gate}$ and $D_{it,sub}$, and the fixed oxide charge Q_f can be neglected [51]. This means that $C_{it,gate} \approx qD_{it,gate}$ and $C_{it,sub} \approx qD_{it,sub}$ in Eq. 2.2 are ignored.

Using Gauss law the oxide field strength can be related to the total capacitance and Eq. 2.1 can be expressed as :

$$C(V_g) = \frac{\partial Q_g}{\partial V_g} = \epsilon_{ox} \frac{\partial E_{ox}}{\partial V_g} \tag{2.3}$$

Eq. 2.3 can be solved explicitly for the oxide field strength E_{ox} as a function of the gate voltage V_g which results in Eq. 2.4 :

$$E_{ox}(V_g) = \frac{1}{\epsilon_{ox}} \int_{V_{fb}}^{V_g} C(V_g')\, \mathrm{d}V_g' \tag{2.4}$$

Where V_{fb} is the flatband voltage. It is assumed that V_{ox}=0 when V_g=V_{fb}.

So the conversion from measured gate voltage V_g to oxide field strength E_{ox} can easily be carried out by integration of the measured C-V_g curve if the flatband voltage V_{fb} is known. Similar, an expression for the total band bending in the gate (gate depletion) and Si-substrate can be obtained, using Eq. 2.2. The result is given by Eq. 2.5 [52], which is also known as the Berglund method [51, 53] :

$$[V_{sub} - V_{gate}](V_g) = \int_{V_{fb}}^{V_g} \left(1 - \frac{C(V_g')}{C_{ox}}\right) \mathrm{d}V_g' \tag{2.5}$$

Where V_{sub} and V_{gate} are respectively, the voltage drop in the Si-substrate and the voltage drop in the gate due to band bending.

Using Eq. 2.5 it is now possible to derive the band bending in the gate as a function of the gate voltage in first order approximation, by calculating the band bending in the Si substrate V_{sub}, assuming no gate depletion and subtracting the result from Eq. 2.5. The oxide capacitance C_{ox} can derived in first order approximation, including the finite thickness of the inversion and accumulation layer, by measuring the capacitance in strong accumulation. Although this capacitance is voltage dependent (see Figs. 2.1 and 2.2), it will still be a reasonable approximation for high V_g values.

Note that gate depletion will result in a decrease of the total capacitance C, measured at high -V_g (p^+-poly) and +V_g (n^+-poly). This is since due to gate depletion, the depletion layer in the gate becomes wider with increasing gate bias (also V_{gate} increases) which results in a decrease of the gate capacitance C_{gate}.

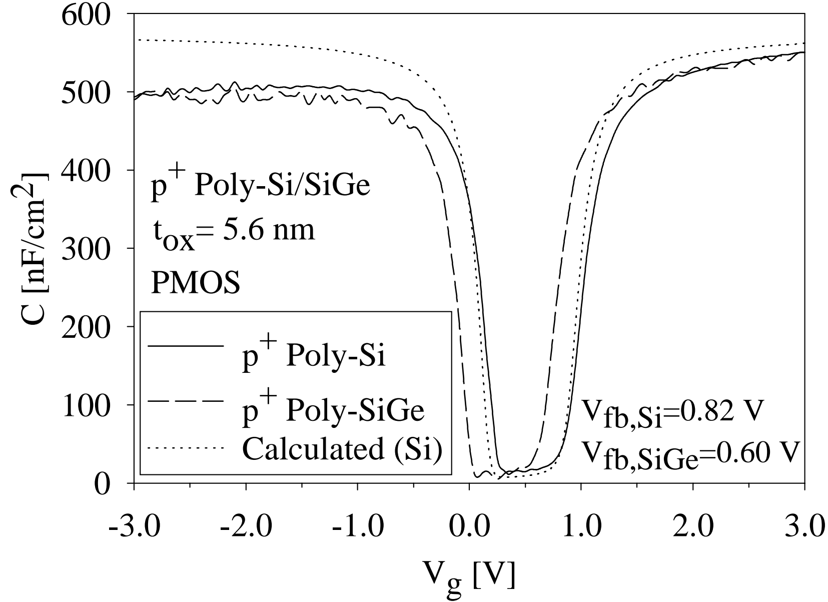

Figure 2.1: Quasi-static C-V_g curves for p^+-poly Si and p^+-poly $Si_{0.7}Ge_{0.3}$ PMOS capacitors with 5.6 nm oxide thickness. Dashed line poly-SiGe, solid line poly-Si and dotted line calculated (poly-Si).

Since C_{gate} is in series with the oxide layer capacitance (Eq. 2.2) this will result in a decrease of the total measured capacitance.

Quasi-static C-V_g curves for PMOS capacitors with p^+-poly Si and p^+-poly $Si_{0.7}Ge_{0.3}$ gate on 5.6 nm gate oxide thickness are shown in Fig. 2.1. Measured C-V_g data were compared with calculated results to determine the flatband voltage V_{fb}, which is defined by the shift in voltage between measured and calculated curve. A one-dimensional (1-D) simulator using Poisson equations and Fermi-Dirac statistics was used to extract the flatband voltage from the measurements. Note that the calculated curves in Figs. 2.1, 2.2 and 2.3 are already shifted over the flatband voltage V_{fb} for poly-Si. From Fig. 2.1 a shift in the flatband voltage from V_{fb}=0.82 V (poly-Si) to V_{fb}=0.60 V (poly-SiGe) is observed, which agrees well with previous data [42, 43, 40]. It is caused by a shift in the valence band edge position of the gate [42, 43]. Note that the gate depletion is acceptable for both devices.

It should however be noted that Boron penetration through the gate oxide can easily cause a positive shift in V_{fb} (and threshold voltage V_t) of several volts [54]. This means that care should be taken while interpreting C-V measurements.

Fig. 2.2 shows the C-V_g curves for NMOS capacitors with n^+-poly Si and n^+-poly $Si_{0.7}Ge_{0.3}$ gate material. Note that for n^+ doped poly-SiGe gate devices

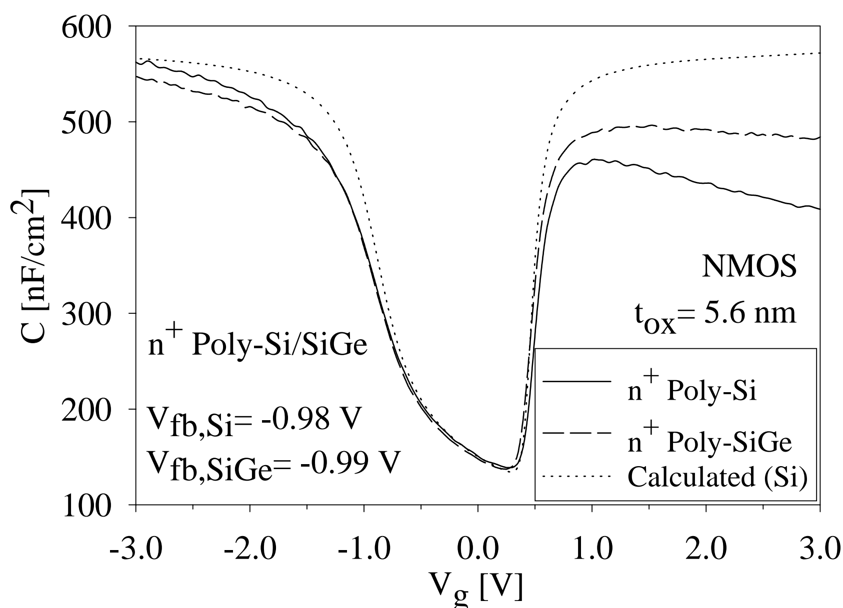

Figure 2.2: Quasi-static C-V_g curves for n^+-poly Si and n^+-poly $Si_{0.7}Ge_{0.3}$ NMOS capacitors with 5.6 nm oxide thickness. Dashed line poly-SiGe, solid line poly-Si and dotted line calculated (poly-Si).

the shift in flatband voltage V_{fb}=-0.98 V (poly-Si) to V_{fb}=-0.99 V (poly-SiGe) is negligible. This is in agreement with results found by others [42, 43, 55] and can be attributed to the small difference in workfunction between n^+-poly Si and n^+-poly SiGe, which is less than $\Delta\phi$= 50 mV (see chapter 1). This 50 mV is the difference in electron affinity between Si(χ=4.05 eV) and Ge(χ=4.00 eV), poly-SiGe having an electron affinity in between Si and Ge. Also it is evident from Fig. 2.2 that the gate depletion of the poly-SiGe devices is significantly reduced compared to the poly-Si reference devices. This result agrees with results found by others [55, 56]. The reduction of gate depletion is most likely due to the enhanced diffusivity of As^+ in poly-SiGe compared to poly-Si, though a decrease in dopant activation for Arsenic and Phosphorus poly-SiGe compared to the poly-Si reference devices was also found by Salm *et al.* [44]. This decrease in dopant activation however is in contradiction with previous findings presented by King *et al.* [43]. They observed for n^+ doped poly-SiGe gates an increase in mobility and dopant activation for Phosphorus implanted poly-SiGe up to a Ge content of x=0.35.

High frequency(10 kHz) C-V_g curves for PMOS transistors with p^+ poly-Si gate on 4.8 nm oxide thickness using various gate RTA anneal temperatures are shown

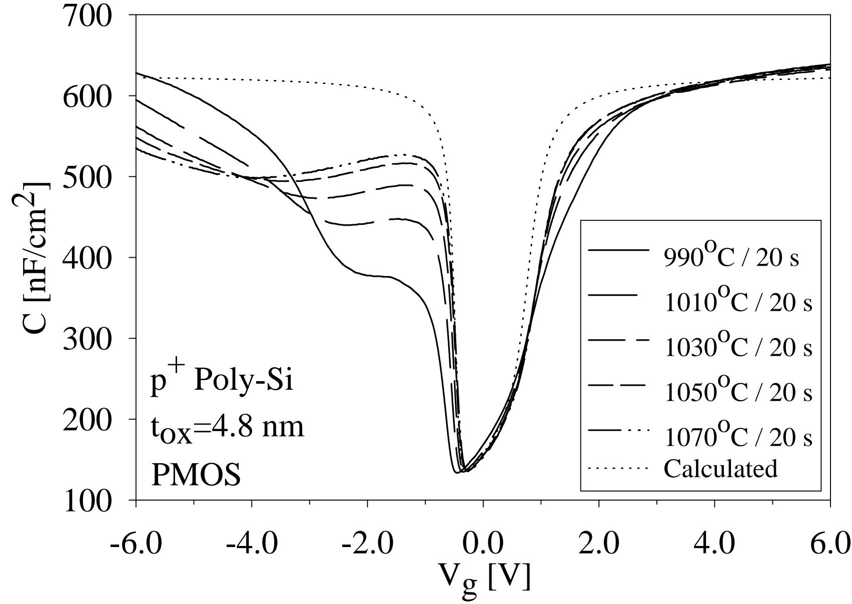

Figure 2.3: High frequency C-V_g curves of PMOS p^+ poly-Si gate devices on 4.8 nm gate oxide, with source/drain and substrate grounded (gated-diode). The gate RTA anneal temperature is varied from 990°C to 1070°C/ 20 sec.

in Fig. 2.3. During measurement the source/drain and substrate were grounded (gated-diode), so minority carriers can be rapidly supplied and extracted by the source/drain regions which results in a quasi-static like C-V curve. From Fig. 2.3 it can be observed that the flatband and threshold voltage of all devices are approximately the same. At -V_g the curves differ from each other because of gate depletion. It can be noted that the gate depletion decreases with increasing gate RTA anneal temperature. Also, the C-V_g curves show no sharp onset of inversion in the p^+ poly-Si gate at -V_g as is normally observed for n^+ gate devices [57]. This is most likely caused by carrier tunneling out of the gate, which occurs at a higher rate than that of carrier generation. Another possible explanation is the stretch-out of the C-V curve due to interface traps $D_{it,gate}$ present at the poly-Si/SiO_2 interface [51]. To bring the poly-Si gate into inversion requires a larger range of gate charge variation for the case with interface traps, than without interface traps. Since gate charge and gate bias are related to each other, see Eq. 2.1, a larger swing of gate bias will be needed if interface states are present at the poly-Si/SiO_2 interface. Because interface traps occupancy varies with gate bias, stretch-out of the C-V curve occurs.

In the next section the current-voltage characteristics of both n^+ and p^+ poly-Si and poly-$Si_{0.7}Ge_{0.3}$ MOS capacitors are investigated and discussed in detail.

2.4 Charge carrier transport through thin oxides

Fowler-Nordheim(FN) tunneling [58] is a *field-assisted* conduction mechanism based on the quantum-mechanical tunneling of carriers through a triangular potential barrier. This mechanism can be used to describe the current flow of carriers through the gate oxide under high field injection conditions (V_{ox}=E_{ox}·t_{ox} >3.1 V). This current in the Si/SiO_2 system primarily originates from electrons rather then holes, since the barrier height is much higher for the latter ($\mathcal{E}_b$=4.5 eV compared to 3.1 eV) [59]. By applying an electric field E_{ox}, the tunneling distance through the oxide can be decreased, so electrons can tunnel from the conduction band of the semiconductor through the potential barrier of the oxide into the conduction band of the oxide as is illustrated in Fig. 2.4 (left Fig.).

An analytical expression for the FN-tunneling current density J_{FN} in the Si/SiO_2 system has been derived in [60, 59] and is given by Eq. 2.6 :

$$J_{FN} = AE_{ox}^2 \cdot \exp\left(\frac{-B}{E_{ox}}\right) \tag{2.6}$$

$$A = \frac{q^3}{16\pi^2\hbar\mathcal{E}_b}\frac{m}{m^*} \qquad B = \frac{4\sqrt{2m^*}\mathcal{E}_b^{\frac{3}{2}}}{3q\hbar} \tag{2.7}$$

Where E_{ox}=V_{ox}/t_{ox} is the electric field strength across the oxide, q the electron charge, $\hbar$ the reduced Planck constant, m is the electron rest mass, m^* the electron effective mass in SiO_2 (m^*=0.34 · m) and $\mathcal{E}_b$ is the energy barrier height at the Si/SiO_2 interface ($\mathcal{E}_b$=3.1 eV).

For ultra-thin gate oxides(t_{ox} <5 nm) Direct-Tunneling(DT) becomes the dominant conduction mechanism. In this conduction mechanism electrons can tunnel *directly* from the cathode to the anode through the oxide, without entering the oxide conduction band, as is illustrated in Fig. 2.4 (right Fig.).

However, the direct-tunneling current density J_{DT} can not be described as easily in a closed analytic form as FN-tunneling. Several approximate equations and computer simulations can be found in literature [61, 50, 62, 63, 52, 64, 65] of which the following is used in the remainder of this study :

$$J_{DT} = A^{'}E_{ox}^2 \cdot \exp\left(\frac{-B^{'}}{E_{ox}}\right) \tag{2.8}$$

$$A^{'} = A \cdot \left(1 - \sqrt{\frac{\mathcal{E}_b + qV_{ox}}{\mathcal{E}_b}}\right)^{-2} \qquad B^{'} = B \cdot \left[1 - \left(\frac{\mathcal{E}_b - qV_{ox}}{\mathcal{E}_b}\right)^{3/2}\right] \tag{2.9}$$

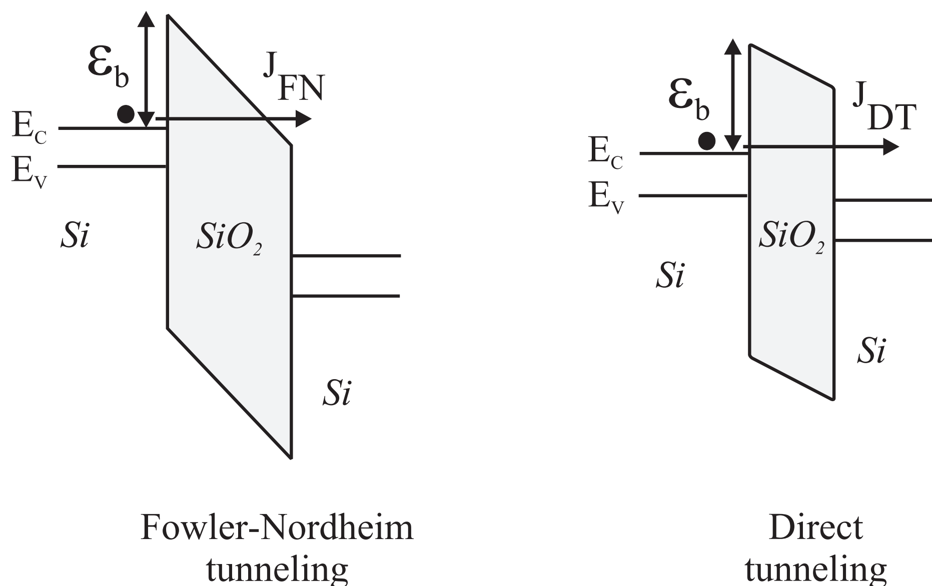

Figure 2.4: Schematic representation of Fowler-Nordheim tunneling (left) and Direct-Tunneling (right) mechanism.

2.4.1 I-V measurements on poly-Si and poly-SiGe MOS capacitors

In this section I-V measurements are performed on both n^+ and p^+ poly-Si and poly-$Si_{0.7}Ge_{0.3}$ MOS capacitors with 5.6 nm gate oxide thickness. All measurements were performed on MOSFETs or gate-controlled diodes [66] with source/drain or diode (minority carrier source) and substrate grounded.

This structure has the advantage that it is suited for both (gate and substrate) injection polarities. The substrate is either in depletion, accumulation or inversion depending on gate bias polarity. For inversion conditions, the minority carriers are supplied by the source/drain (diode) regions to create an inversion layer. This ensures that the devices are always measured under equilibrium conditions, since the substrate is never in deep depletion (non-equilibrium) during measurements.

Figs. 2.5 and 2.6 displays the J-V_g characteristics of unstressed n^+ and p^+ poly-Si and poly-SiGe MOS capacitors for substrate- (+V_g) and gate-injection (-V_g) conditions. These data show that the measured J-V_g characteristics are not symmetric with respect to V_g, which is inconsistent with the notion that tunneling should be independent of bias polarity. This asymmetry in gate bias polarity can be attributed to two effects :

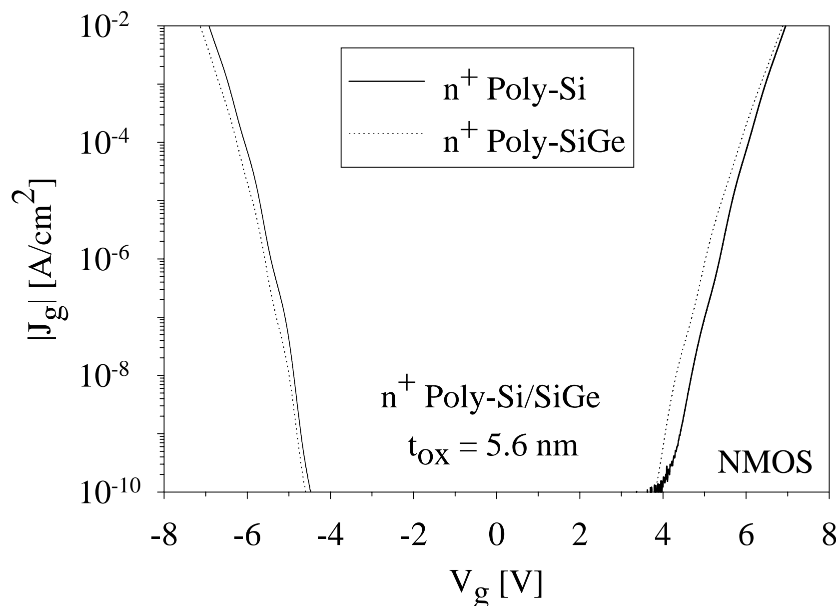

Figure 2.5: I-V measurements of unstressed n^+ poly-Si and poly-$Si_{0.3}Ge_{0.7}$ gate NMOS capacitors with 5.6 nm oxide thickness. Dashed lines poly-SiGe, solid lines poly-Si.

- **Workfunction difference**
  The *metal-to-semiconductor* workfunction difference ϕ_{ms} between the gate and substrate will lead to band bending in the silicon substrate and thus a voltage drop V_{sub} will be present in the mono-Si substrate at V_g=0 V. The voltage necessary to cancel this voltage drop and achieve flat band conditions in the Si/SiO_2 system equals the difference in work functions of the gate and the substrate and is called the flat-band voltage V_{fb}.

- **Gate depletion**
  At low active gate doping band bending may also be present in the gate, which leads to a voltage drop V_{gate} in the gate material. This voltage drop can be expressed in first order approximation, i.e. not taking into account any quantum mechanical effects, by making use of the depletion approximation. The result of this is given by [67, 50, 68] :

$$V_{gate} = \frac{\epsilon_{ox}^2 E_{ox}^2}{2q\epsilon_{si} N_{poly}} \tag{2.10}$$

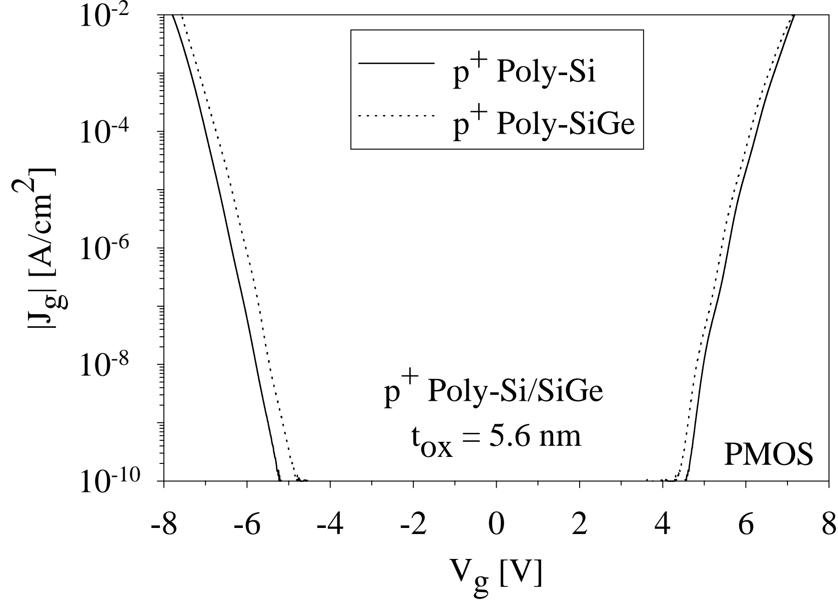

Figure 2.6: I-V measurements of unstressed p^+ poly-Si and poly-$Si_{0.3}Ge_{0.7}$ gate PMOS capacitors with 5.6 nm oxide thickness. Dashed lines poly-SiGe, solid lines poly-Si.

Where ϵ_{ox} and ϵ_{si} are respectively the permitivity of SiO_2 and Si. N_{poly} is the electrically active doping concentration of the gate.

This effect is called gate depletion and becomes important if the dopant in the gate is not fully activated or has not diffused sufficiently to the poly-Si/SiO_2 interface.

In order to investigate and compare the leakage currents of oxides it is thus necessary to compensate for above mentioned effects and relate the oxide voltage V_{ox} and thus oxide field strength E_{ox} to the applied gate voltage V_g. This is achieved by integration of the capacitance-voltage(C-V) curves as is given by Eq. 2.4 [52, 69].

Fig. 2.7 shows the J_g-E_{ox} characteristics of unstressed n^+ and p^+ poly-Si and poly-SiGe capacitors on 5.6 nm gate oxide thickness, under substrate- ($+V_g$) and gate-injection ($-V_g$) conditions. For n^+-gate devices the J_g-E_{ox} characteristics are (almost) symmetric under $-V_g$ and $+V_g$ injection conditions, consistent with the notion that tunneling should be independent with gate bias polarity.

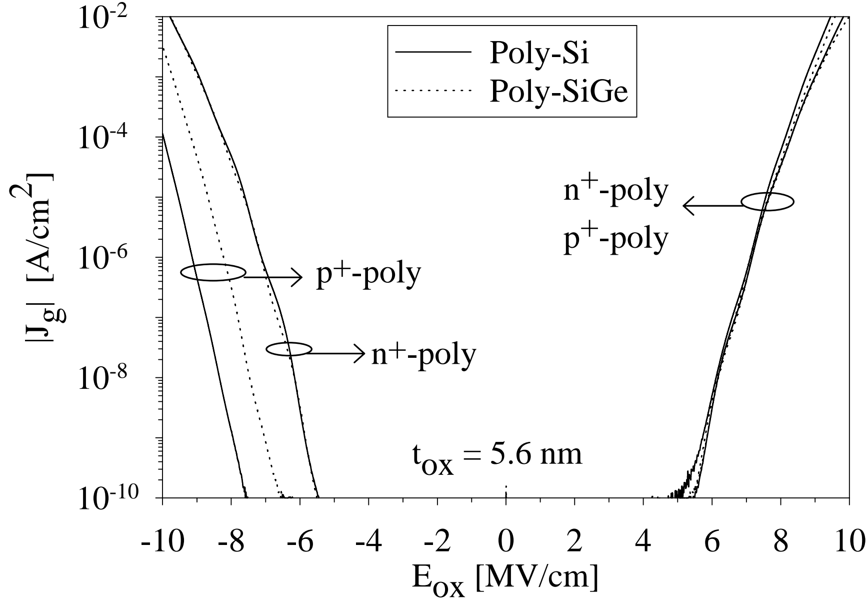

Figure 2.7: J_g-E_{ox} measurements of unstressed n^+ and p^+ poly-Si and poly-$Si_{0.3}Ge_{0.7}$ gate MOS capacitors with 5.6 nm oxide thickness. Dashed lines poly-SiGe, solid lines poly-Si.

However, for p^+-gate devices, the onset of conduction for -V_g occurs at a significantly higher oxide field ($\approx 1.5\times$) than for $+V_g$ condition. Note the difference for p^+-gate devices between poly-Si and poly-SiGe at -V_g.

Fig. 2.8 displays the Fowler-Nordheim plot of our p^+-gate MOS capacitors for $+V_g$ and -V_g injection conditions. At $+V_g$ the J_g-E_{ox} curves of our p^+ gate devices can be fitted with the standard Fowler-Nordheim (FN) expression with barrier height of $\mathcal{E}_b$ =3.1 eV. For -V_g a fit with the standard FN tunneling expression can not be obtained, unless unphysical fit parameters are used.

Ogier *et al.* [39] and Salm *et al.* [40] assumed that the conduction mechanism of their p^+ gate devices at -V_g is caused by tunneling of electrons from the valence band of the gate, i.e. Valence Band Tunneling(VBT). They presumed that VBT tunneling can be described by FN tunneling with an increased barrier height of $\mathcal{E}_b$=3.1+$\mathcal{E}_g$=4.2 eV(poly-Si) and 4.0 eV(poly-SiGe).

The slope of the Fowler-Nordheim plot indeed indicates that the barrier height $\mathcal{E}_b$ is higher ($\approx$4.5 eV(poly-SiGe) and $\approx$5.3 eV(poly-Si)) compared to $+V_g$ injection conditions. However the barrier height is larger than expected if Valence Band Tunneling(VBT) is assumed as the conduction mechanism at -V_g.

Also the pre-exponential factor A in the FN tunneling expression (see Eq. 2.7) is much larger A= $5.4\cdot10^2$ A/V^2(poly-Si) and A=$4.3\cdot10^{-1}$ A/V^2(poly-SiGe) com-

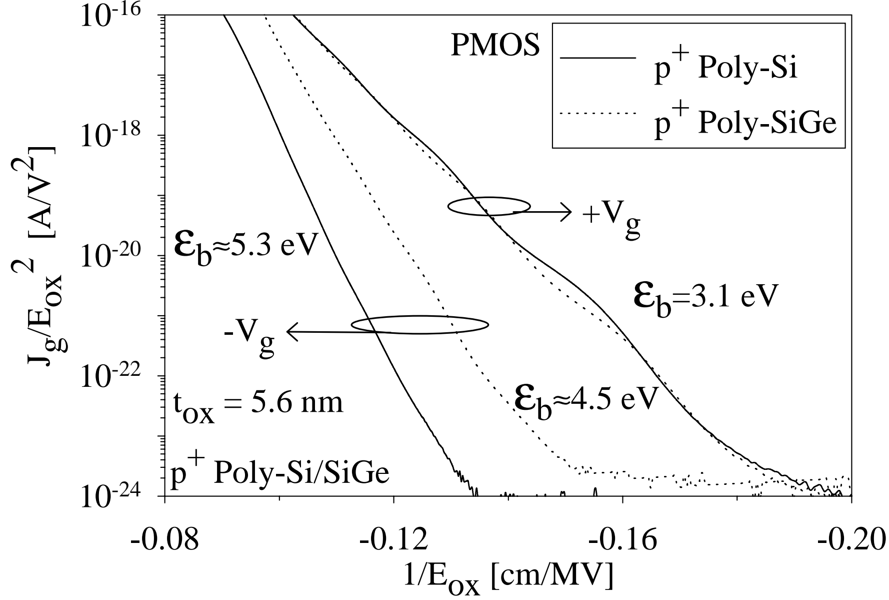

Figure 2.8: Fowler-Nordheim(FN) plot of unstressed p^+ poly-Si and poly-$Si_{0.3}Ge_{0.7}$ gate PMOS capacitors with 5.6 nm oxide thickness. Dashed lines poly-SiGe, solid lines poly-Si.

pared to $+V_g$ injection conditions, $A=1.1\cdot10^{-6}$ A/V^2(poly-Si/SiGe). From this pre-exponential factor the barrier height can also be calculated, resulting in an *unrealistic* barrier height of $\mathcal{E}_b=6.2\cdot10^{-9}$ eV(poly-Si) and $\mathcal{E}_b=7.8\cdot10^{-6}$ eV(poly-SiGe). This indicates that the standard Fowler-Nordheim (FN) expression, even with increased barrier height $\mathcal{E}_b$, can not be used to describe the conduction mechanism at $-V_g$ of our p^+ gate devices [39, 40].

So for our p^+ gate devices tunneling depends on the oxide field bias polarity, which is in contradiction with FN-tunneling, see Eq. 2.6. The reason for this bias polarity dependence is most likely related to the fact that at $-V_g$ the number of electrons available for tunneling in the conduction band of the gate is very different for n^+ and p^+-poly gate devices. For n^+-poly gate devices the tunneling electrons are readily supplied by the accumulated n^+ gate. In p^+-poly gate devices at $-V_g$ electrons can tunnel from the conduction band of the gate, but the number of free electrons is very limited, since the active gate doping is high.

The difference in conduction mechanism between $+V_g$ and $-V_g$ in p^+ gate devices also explains the unrealistic voltage drop $|V_{ox}|=|V_g|-2.2$ V found by Schuegraf *et al.* [50] if FN tunneling with a barrier height of $\mathcal{E}_b=3.1$ eV is assumed as conduction mechanism for p^+ gate devices at $-V_g$.

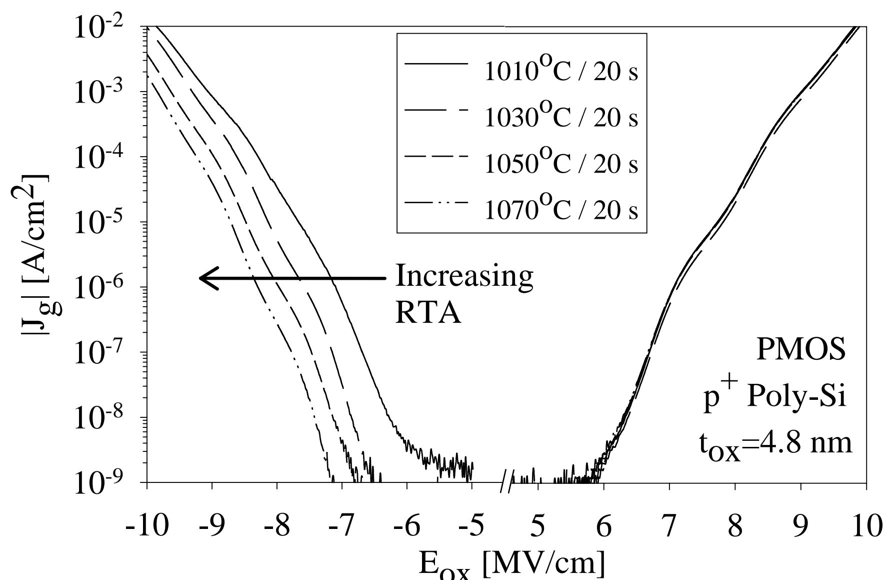

Figure 2.9: J-E_{ox} characteristics of p^+ poly-Si PMOS gate devices on 4.8 nm gate oxide. The gate RTA anneal temperature is varied from 1010°C/20 sec to 1070°C/ 20 sec.

This clearly demonstrates that an accurate method to determine the oxide field strength E_{ox} is essential to properly evaluate the conduction mechanism for p^+ gate devices.

To further investigate the conduction mechanism at -V_g of p^+ gate devices, the J-E_{ox} characteristics of p^+ poly-Si PMOS capacitors on 4.8 nm gate oxide with different gate RTA anneal temperatures are studied. Fig. 2.9 displays the J-E_{ox} characteristics of p^+ poly-Si gate devices on 4.8 nm gate oxide for different gate RTA anneal conditions. In Fig. 2.9 the gate RTA anneal temperature is varied from 1010°C/20 sec to 1070°C/20 sec. It can be seen that for +V_g injection conditions the conduction mechanism is simply Fowler-Nordheim (FN) tunneling and there is no dependence on gate RTA anneal temperature. However, for -V_g injection conditions a shift to higher oxide fields E_{ox} is observed with increasing gate RTA anneal temperature.

So one might ask the question which tunneling mechanism dominates at -V_g for p^+-poly gate devices. Fig. 2.10 displays the possible conduction mechanisms for p^+-poly gate devices at -V_g injection conditions.

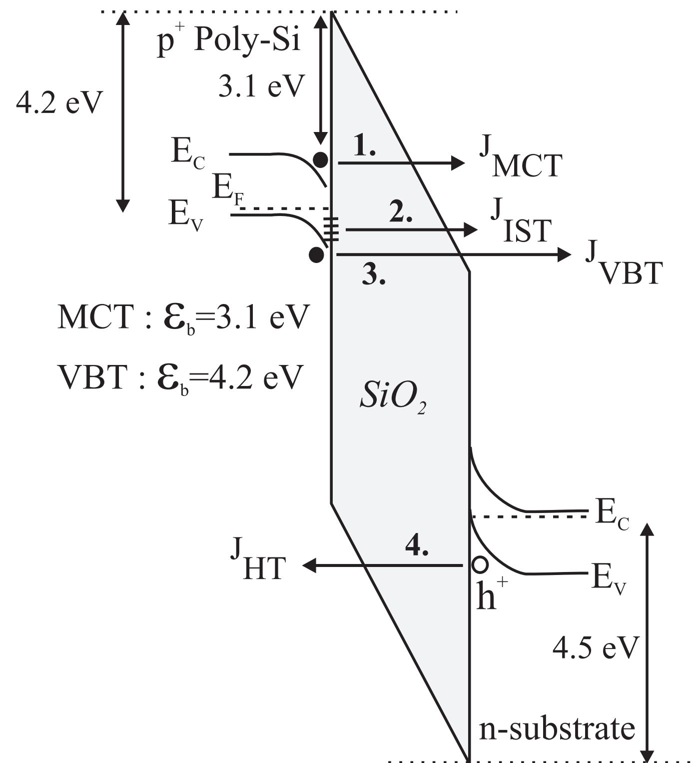

Figure 2.10: Schematic illustration of the four conduction mechanisms possible in p^+-poly gate devices at -V_g bias condition. 1) Minority Carrier Tunneling(MCT) 2) Interface State Tunneling(IST) 3) Valence Band Tunneling(VBT) 4) Hole Tunneling(HT).

Looking more closely at Fig. 2.10 the following tunneling mechanisms can be distinguished for p^+ gate devices at -V_g injection conditions [41] :

1. *electron tunneling from the conduction band of the p^+-poly gate.*

   There are three possible mechanisms for electron injection from the gate. Firstly tunneling of minority carriers(MCT), i.e. electrons tunneling from the conduction band of the gate to the substrate could occur at high negative gate bias when active gate doping is low. The band bending (gate depletion) at the p^+ poly gate-SiO_2 interface for -V_g increases the surface electron concentration. For high active gate doping at the p^+ poly gate-SiO_2 interface this mechanism is less probable since gate depletion is reduced.

2. *electron tunneling from interface states present at the p^+ poly gate-SiO_2 interface.*

   The seconds possible tunneling mechanism is interface state tunneling(IST)

of electrons tunneling from interface states in the p^+ poly gate. There is a high density of interface traps present at the p^+ poly gate-SiO_2 interface from which electrons can tunnel into the oxide. This conduction mechanism might be important in our devices, however it will be neglected in order to investigate the other tunneling mechanisms.

3. *electron tunneling from the valence band of the p^+-poly gate.*

   A third possibility is valence band tunneling(VBT) [39, 40]. In the case of valence band tunneling, electrons tunnel from the valence band of the p^+ poly gate through the potential barrier of the oxide into the conduction band of the oxide as is illustrated in Fig. 2.10. The tunneling probability is much lower than for electrons tunneling from the conduction band of the p^+-poly gate, since now electrons see a higher barrier ($\mathcal{E}_b$=4.2 eV instead of $\mathcal{E}_b$=3.1 eV). However there is a high density of electrons present in the valence band of the gate, so the number of electrons available for tunneling is much higher than for electron tunneling from the conduction band of the p^+-poly gate.

4. *hole tunneling from the valence band of the inverted n-type Si substrate.*

   The last possible conduction mechanism is tunneling of holes(HT) from the valence band of the inverted n-type Si substrate. The barrier heights for both valence band electron tunneling from the gate ($\mathcal{E}_b$=4.2 eV) and valence band hole tunneling from the inverted substrate ($\mathcal{E}_b$=4.5 eV) are comparable. This indicates that the conduction mechanism in p^+-gate devices at -V_g could also be caused by hole tunneling(HT) from the valence band of the inverted n-type Si substrate.

It can thus be concluded that for p^+-gate devices at -V_g, neglecting IST, there are three competing tunneling mechanisms. The magnitude of these different tunneling mechanisms depend only on the barrier height $\mathcal{E}_b$ and on the number of carriers available for tunneling (and thus on the active gate doping of the p^+-gate).

To further investigate the conduction mechanism for p^+-poly gate devices under -V_g injection conditions, the gate, diode and substrate currents were measured by means of carrier separation technique [70, 71] applied to gate-controlled diodes with p^+-diode and n-type Si substrate grounded, see Fig. 2.11. By employing this technique the electron and hole tunneling currents can be measured independently of each other, so a clear distinction between electron and hole tunneling can be made.

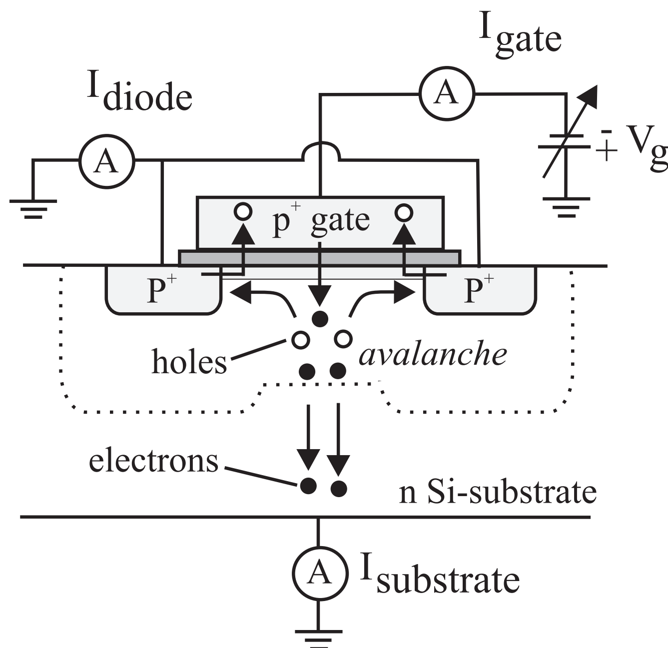

Figure 2.11: Carrier separation technique applied to p^+ poly-Si PMOS gate-controlled diodes under -V_g bias conditions.

The gate, substrate and diode currents measured on p^+-poly Si PMOS gate-controlled diodes with 8 nm oxide thickness are shown in Fig. 2.12. For $+V_g$ conditions the substrate current equals the gate current. This reveals that at $+V_g$ the gate current is most likely due to electron tunneling from the conduction band of the accumulated Si substrate. In addition to this electron current, there is a second (hole) current component (I_{diode}) which appears at higher $+V_g$.

The possible conduction mechanisms for this hole current has already been extensively studied in n-MOSFETs [72, 70, 73]. In n-MOSFETs under $+V_g$ injection conditions electrons are injected from the substrate inversion layer under Fowler-Nordheim injection conditions. At higher $+V_g$ a substrate hole current is measured of which possible conduction mechanism are given below [72, 70, 73]. For thick oxides ($t_{ox} > 10$ nm) it has been considered that impact ionization in the oxide band gap is important in which electrons require an energy of at least $\mathcal{E}_g \approx 9$ eV to create electron hole pairs in SiO_2 [29]. However, for thinner oxides the physical origin for hole generation is still controversial [29, 27]. The most commonly accepted explanation is that this second tunnel-component is due to the tunneling back of hot-holes which are created in the anode (gate) by high-energetic electrons [73, 21, 71]. A fraction of these hot-holes is measured as I_{diode} current in our PMOS gate-controlled diodes under $+V_g$ bias conditions. This tunneling current is also the basic oxide degradation monitor for the Anode Hole Injection model(AHI) as was already explained in chapter 1. Other

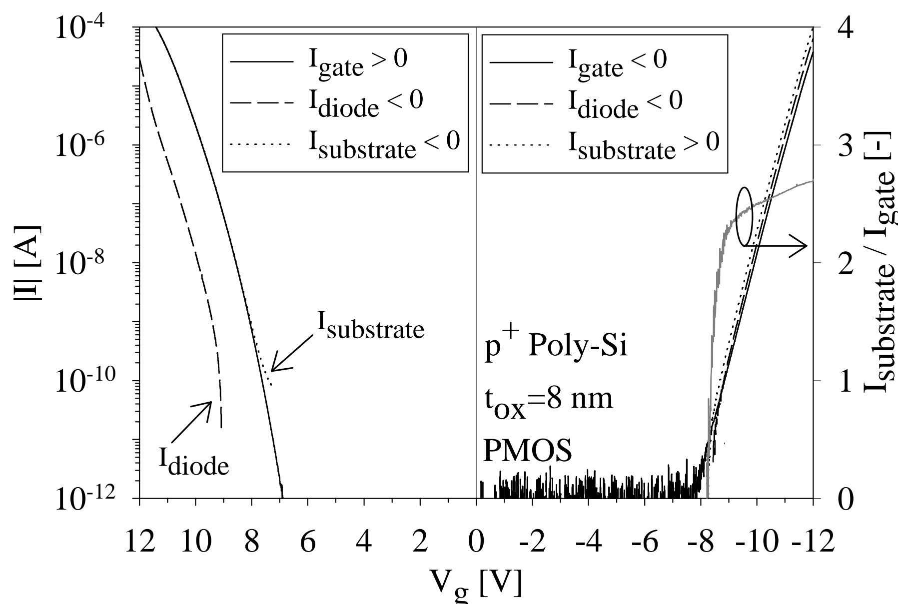

Figure 2.12: Gate, substrate, and diode currents measured as a function of the gate voltage on p^+-poly Si PMOS gate-controlled diodes with 8 nm oxide thickness. The right axis shows the ratio between the substrate and gate current.

explanations for the origin of the current include ion conduction, the creating of electron-hole pairs by high energetic photons ($\mathcal{E}_p$ >1.12 eV) which are created in the gate during hot-electron stressing, or due to the release of hydrogen H^+ from the Si/SiO_2 interface (see also chapter 1).

For -V_g conditions both the substrate and diode current are larger than the gate current (right axis Fig. 2.12, $I_{substrate} > 2\times\ I_{gate}$). The larger substrate current indicates that an avalanche process is taking place [70]. This is not expected when hole tunneling from the substrate dominates the gate current. This can only be explained when the gate current at -V_g for our p^+ gate devices is caused by electron injection from the gate. Hole Tunneling(HT) from the substrate is negligible at least in our devices, with $t_{ox} > 4$ nm.

For very thin oxides (t_{ox} <4 nm) another contribution to the I-V curve at -V_g can be observed, see Fig. 2.13. Carrier separation measurements on p^+ poly-Si PMOS gate devices with 3.1 nm gate oxide thickness are performed to discriminate between electron and hole currents. For -V_g bias condition a hole current flowing from the source/drain to the gate is observed in the low voltage

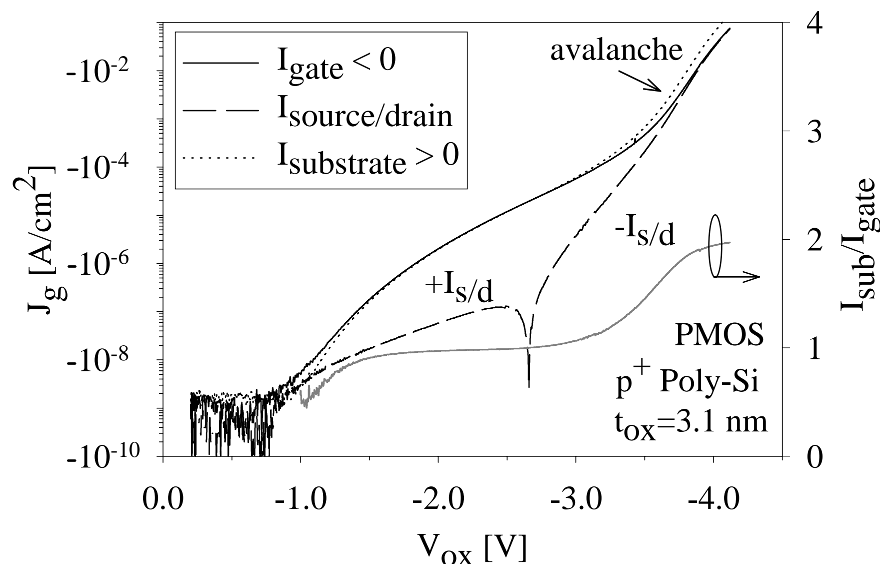

Figure 2.13: Carrier separation technique applied to p^+-poly Si PMOS gate-controlled diodes with 3.1 nm gate oxide thickness. Below V_{ox}=-2.8 V a hole current flowing from the source/drain to the gate is observed.

regime (V_{ox} <-2.8 V). This result agrees with recent findings by others [41, 46].

A possible explanation for this current might be holes tunneling from the substrate hole inversion layer to the gate. This will result in a positive source/drain current $+I_{s/d}$. Another possibility is the recombination of holes with electrons in the hole inversion layer. The electrons are injected from the gate and recombine with holes in the hole inversion layer which are supplied by the source/drain regions. This also results in a positive source/drain current $+I_{s/d}$. However, since the inversion layer is very thin (< 1 nm) the recombination rate has to be very high ($\approx 10^{19}$ cm^{-3}/s) to account for the current. Moreover the electrons also have kinetic energy upon reaching the hole inversion layer and are even further accelerated by the electrical field in the substrate. This makes the recombination of electrons with holes in the hole inversion layer even more improbable. This indicates that it is very unlikely that the hole current originates from the recombination of holes with electrons in the hole inversion layer. Moreover, recently Takagi *et al.* [74] showed that by changing the substrate bias, and thus the threshold voltage of the holes in the hole inversion layer, that the recombination of electrons with holes in the inversion layer is negligible.

It can thus be concluded that this hole current is most likely due to holes which can tunnel from the hole inversion layer in the substrate to the gate. This hole

current increases strongly with decreasing oxide thickness and might be important for the degradation of ultra-thin oxides, since hot holes are no longer needed to trigger the breakdown process as is required according to the Anode Hole Injection model(AHI) [22, 23, 24][1]. This can also be of importance for very thin oxide n^+ poly-gate devices at -V_g condition and as MCT for +V_g.

Also from Fig. 2.13 it can be observed that at V_{ox}=-2.8 V impact ionization occurs. This can be noted from the change in sign of the source/drain current $I_{s/d}$. Above this voltage the electrons, which are injected from the gate, have enough kinetic energy to generate electron/hole pairs in the substrate. The generated holes diffuse to the source/drain regions, resulting in the change in sign of $I_{s/d}$. Also observe that in this voltage region the substrate current becomes larger than the gate current (right axis Fig. 2.13, $I_{substrate} > I_{gate}$).

In conclusion, for p^+-poly gate devices gate currents are either influenced by the workfunction for valence band tunneling or by the bandgap of the gate material for the MCT mechanism. It appears that the carrier injection mechanism in p^+-poly gate devices is different for gate and substrate injection conditions. The +V_g mechanism is similar to that for n^+-poly gate devices, i.e. FN electron tunneling from the substrate conduction band. For gate injection, a significantly larger oxide field is required to obtain the same tunneling current as for substrate injection conditions. This will also influence the Stress-Induced Leakage Current(SILC)characteristics[2], results of this will be discussed in chapter 3.

2.4.2 Minority Carrier Conduction Model for p^+ gate devices

The conduction mechanism for p^+ poly gate devices under gate injection conditions in our samples is thus caused by electron tunneling from the gate. However there are still two mechanisms which compete with each other, namely electron tunneling from the valence band of the p^+-poly gate and electron tunneling from the conduction band of the gate. So we have to derive an expression for both MCT and VBT in order to be able to evaluate the possible conduction mechanism in our p^+-poly gate devices at -V_g injection conditions. As stated before, the tunneling probability is much lower for electrons tunneling from the valence band of the gate than for electrons tunneling from the conduction band of the p^+-poly gate, since these electrons see a higher barrier ($\mathcal{E}_b$=4.2 eV instead of

[1] Moreover, this hole current increases strongly with increasing electrical stress. Hence this current is interpreted as trap assisted hole tunneling (HTAT). This is even more critical for gate oxide reliability as will be shown in chapter 3 in section 3.4.6 on page 62.

[2] SILC is the increase in low-level leakage through thin silicon dioxide (SiO_2) layers after the oxide has been subject to high electrical-field stressing. See chapter 3, where SILC will be explained in more detail.

$\mathcal{E}_b$=3.1 eV). However there is a high density of electrons present in the valence band of the gate, so the number of electrons available for tunneling is much higher than for electron tunneling from the conduction band of the p^+-poly gate. Nevertheless, the amount of electrons available for tunneling in the conduction band of the gate also increases with increasing oxide field strength E_{ox}. This is since due to gate depletion (band bending) the conduction band edge of the gate is bend towards the Fermi level $\mathcal{E}_f$ and thus increasing the electron concentration in the conduction band of the gate. This means that for MCT we can not use the FN tunneling equation as given by Eq. 2.6, because this equation is derived under the assumption that the anode consists of degenerated silicon (i.e. n^+-poly gate or inverted p-type Si-substrate) or is a metal gate.

We thus have to derive a different expression for the tunneling current of p^+ gate devices at $-V_g$, taking into account the number of electrons available for tunneling. This is achieved by making use of the Esaki-Tsu tunneling equation [75] which is given by Eq. 2.11 :

$$J_{et} = \frac{n_v m_d kT}{2\pi^2\hbar^3} \int_0^\infty T^* \cdot T_{WKB}(\mathcal{E}_b - \mathcal{E}) \cdot \ln\left[1 + \exp\left(\frac{\mathcal{E}_f - \mathcal{E}}{kT}\right)\right] d\mathcal{E} \tag{2.11}$$

Where $\mathcal{E}_b$ is the energy barrier height at the poly-Si/SiO_2 interface, measured from the conduction band $\mathcal{E}_c$ of the gate. n_v and m_d are respectively the valley degeneracy and the density-of state mass for electrons in the gate material.

The tunneling probability under the Wentzel-Kramers-Brillouin(WKB) approximation $T^* \cdot T_{WKB}$ is given by Eq. 2.12:

$$T^* \cdot T_{WKB}(\mathcal{E}', E_{ox}) = \exp\left[\frac{2\sqrt{2m^*}}{3qE_{ox}\hbar}\mathcal{E}'^{\frac{3}{2}}\right] \tag{2.12}$$

Next, the number of electrons in the conduction band of the gate available for tunneling as a function of the applied oxide field strength E_{ox} has to be evaluated. The free electron concentration in the conduction band of the polysilicon gate can be calculated from its band bending. The difference in energy between the Fermi level in the gate and the conduction band edge at the SiO_2 interface is gate voltage dependent due to gate depletion, i.e. $\mathcal{E}_c$-$\mathcal{E}_f$=$f(V_g)$. Fig. 2.14 displays schematic the band bending and free electron concentration in the conduction band of a p^+ gate for two different gate voltages V_g=$-V_{g1}$ and V_g=$-V_{g2}$ with $|V_{g1}| < |V_{g2}|$. Furthermore it is assumed that the contribution of interface traps on the tunnel current (J_{IST}) can be neglected, i.e. it is assumed that $D_{it,gate}$=0. From Fig. 2.14 it can be seen that the increase in minority carriers in the conduction band of the p^+-poly gate can *effectively* be modeled as an increase of the Fermi level in the gate.

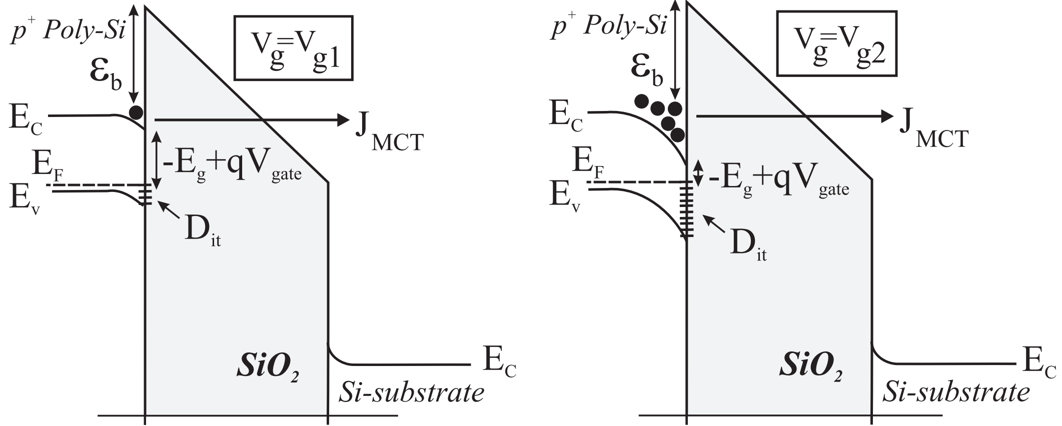

Figure 2.14: Schematic representation of Minority Carrier Tunneling(MCT) in p^+ poly gate devices for two different gate voltages -V_g. $|V_{g1}| < |V_{g2}|$.

The Fermi level, which is assumed to be located in the valence band of the p^+-poly gate, can thus *effectively* be expressed as :

$$\mathcal{E}_f(V_g) = \mathcal{E}_v + qV_{gate} = \mathcal{E}_c - \mathcal{E}_g + qV_{gate} \tag{2.13}$$

Where V_{gate} is the potential drop over the gate depletion layer. $\mathcal{E}_v$, $\mathcal{E}_c$ and $\mathcal{E}_g$ are respectively the valence band edge, the conduction band edge and the bandgap of the gate material.

A first order model of MCT can now be developed based on the Esaki-Tsu tunneling equation and the result is given by Eq. 2.14 :

$$J_{MCT} = \frac{n_v m_d kT}{2\pi^2\hbar^3} \int_{\mathcal{E}=\mathcal{E}_c}^{\infty} T^* \cdot T_{WKB}(\mathcal{E}_b - \mathcal{E}) \cdot \ln\left[1 + \exp\left(\frac{\mathcal{E}_f(V_g) - \mathcal{E}}{kT}\right)\right] d\mathcal{E} \tag{2.14}$$

Note that for $\mathcal{E}_f$=$\mathcal{E}_c$, i.e. the Fermi level is located in the conduction band of the gate (degenerated n^+ poly-Si), Eq. 2.11 simply reduces to Eq. 2.6 which is simply FN tunneling.

Next we have to calculate the band bending in the p^+-poly gate as a function of the oxide field strength E_{ox} in order to be able to evaluate the MCT conduction mechanism in our p^+ gate devices.

Fig. 2.15 displays the potential drop over the gate depletion layer V_{gate} for different p^+ poly-Si doping levels. The voltage drop over the gate depletion layer

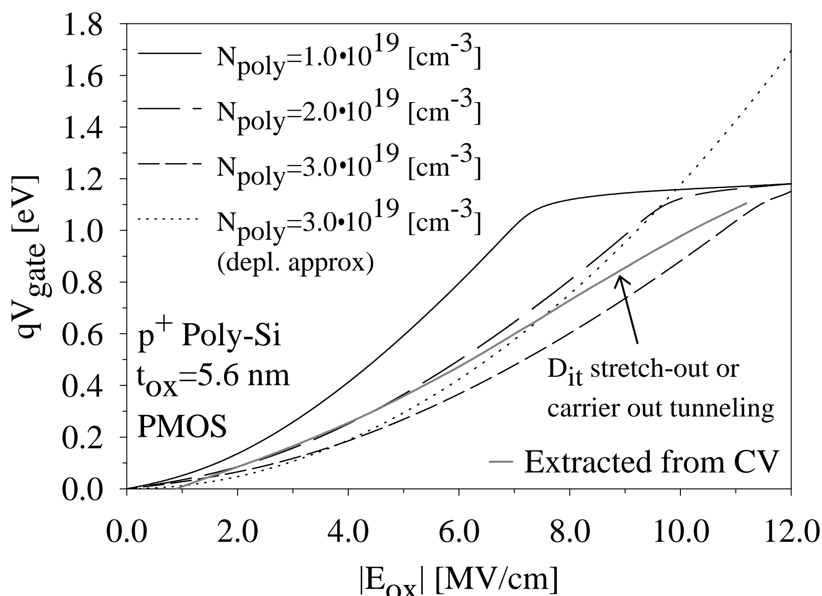

Figure 2.15: Calculated band bending in p^+-poly gate devices at -V_g as a function of applied oxide field strength. Different active gate doping levels and two methods (Fermi-Dirac and depletion approximation) are shown.

was calculated using Fermi-Dirac statistics. This is done by assuming an ideal MOS structure and calculate the band bending in the Si substrate as a function of E_{ox} by solving Poisson's equation [8, 51]. The voltage drop over the gate depletion layer is then taken to be equal to the Si surface potential. For a doping level of N_{poly}=3·10^{19} cm^{-3} the poly-Si band bending was also calculated using the depletion approximation, see Eq. 2.10.

From Fig. 2.15 it can be observed that by using Fermi-Dirac statistics the band bending saturates at qV_{gate}=1.12 eV. This is when the p^+ poly-Si gate is going into inversion. Furthermore, it can be noted that the depletion approximation overestimates the band bending in the p^+ poly-Si gate. This clearly shows the necessity of Fermi-Dirac statistics to calculate the band bending in the poly-Si gate. The band bending in the gate as a function of E_{ox} derived from C-V measurements (using Eq. 2.5) is also depicted in Fig. 2.15. From this it can be observed that for high oxide field strength, V_{gate} starts to deviate from the calculated curves. This is most likely caused by carriers tunneling out of the gate, which occurs at a higher rate than that of carrier generation during MCT tunneling from the gate (-V_g). This will tend to decrease the band bending in the gate, since the charge at the gate surface Q_g is effectively reduced due to tunneling out of the gate.

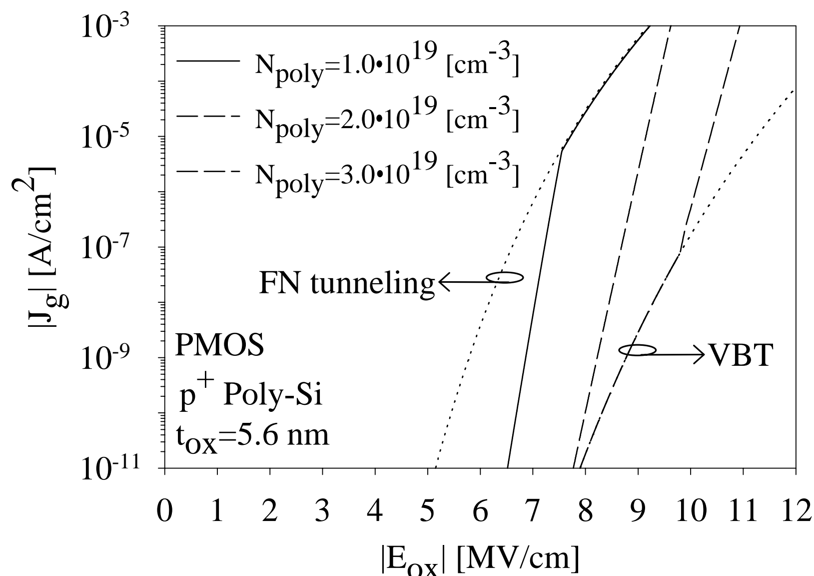

Figure 2.16: Calculated carrier conduction in p^+ poly-Si gate devices at $-V_g$ for different active gate doping.

So a larger gate bias will be needed for the same surface potential in the poly-Si gate. It should however be noted that another possible explanation is the stretch-out of the C-V curve due to interface traps $D_{it,gate}$, present at the poly-Si/SiO_2 interface. This was already mentioned in section 2.3. If interface traps are present at the poly-Si/SiO_2 interface, more gate charge Q_g on the poly-Si gate is needed to create a given surface potential. So to bring the poly-Si gate into inversion requires a larger swing of gate bias variation for the case with interface traps, than without interface traps.

We also have to derive an expression for tunneling of electrons from the valence band of the gate, i.e. VBT. This is done using the same tunneling equation as Eq. 2.11.

An expression for the tunneling current of electrons from the valance band of the gate(VBT) can now be derived and is given by Eq. 2.15 :

$$J_{VBT} = \frac{n_v m_d kT}{2\pi^2 \hbar^3} \int_{\mathcal{E}=\mathcal{E}_v}^{-\infty} T^* \cdot T_{WKB}(\mathcal{E}_b - \mathcal{E}) \cdot \ln\left[1 + \exp\left(\frac{\mathcal{E}_f - \mathcal{E}}{kT}\right)\right] d\mathcal{E} \tag{2.15}$$

Where $\mathcal{E}_f$=$\mathcal{E}_v$ is the Fermi level in the gate, which is assumed to be located at the valence band edge of the gate.

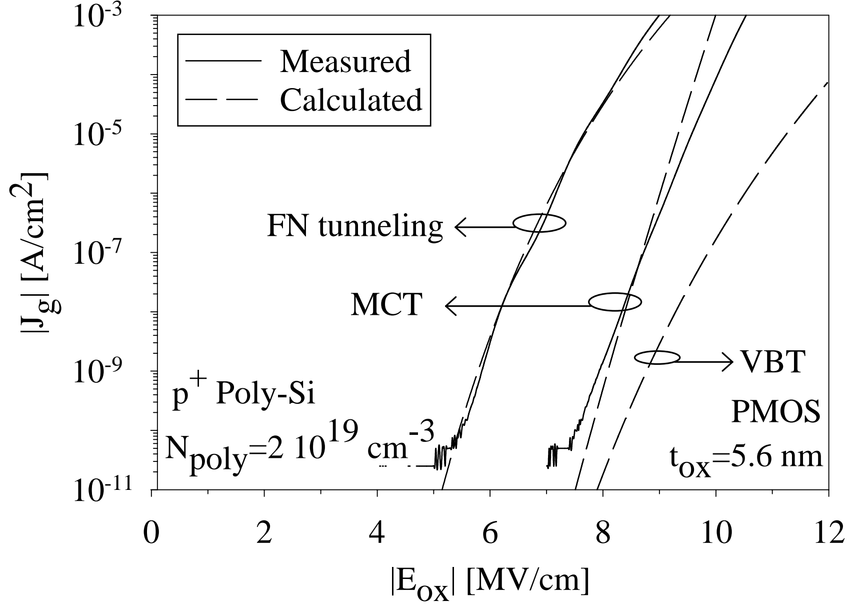

Figure 2.17: Minority Carrier Tunneling(MCT) in our p^+ poly-Si gate devices at $-V_g$. The poly-Si gate doping is estimated to be $N_{poly} \approx 2.0 \cdot 10^{19}$ cm^{-3}.

Recall that the barrier height $\mathcal{E}_b$ is now measured from the valence band of the gate ($\mathcal{E}_b$=4.2(poly-Si) 4.0(poly-SiGe) instead of 3.1 eV). Also note that we have to integrate from $\mathcal{E}=\mathcal{E}_v$ to $-\infty$, since the electrons are located in the valence band of the gate.

Fig. 2.16 displays the calculated J-E_{ox} characteristics for p^+ poly-Si gate devices at $-V_g$ for different active gate doping. The physical parameters used for tunneling are : m_d=0.33·m, m^*=0.35·m, n_v=6, $\mathcal{E}_b$=3.1(MCT) and 4.2(VBT) eV. The voltage drop over the gate depletion layer V_{gate} was calculated using Fermi-Dirac statistics. From Fig. 2.16 it can be observed that for (low) active gate doping $N_{poly} < 1 \cdot 10^{19}$ cm^{-3} the conduction mechanism is simply FN tunneling from the inverted p^+ poly-Si gate, while for an active gate doping of $1 \cdot 10^{19}$ cm^{-3} $< N_{poly} < 3 \cdot 10^{19}$ cm^{-3} the tunneling current density at $-V_g$ is due to MCT of electrons from the conduction band of the gate. For higher active gate doping the band bending in the gate is not sufficient to have a measurable current due to MCT. In this case, the conduction mechanism in p^+ poly-Si gate devices at $-V_g$ is caused by tunneling of electrons from the valence band of the gate, i.e. VBT. It is now possible to evaluate the conduction mechanism at $-V_g$ of our p^+ poly-Si and p^+ poly-SiGe gate devices.

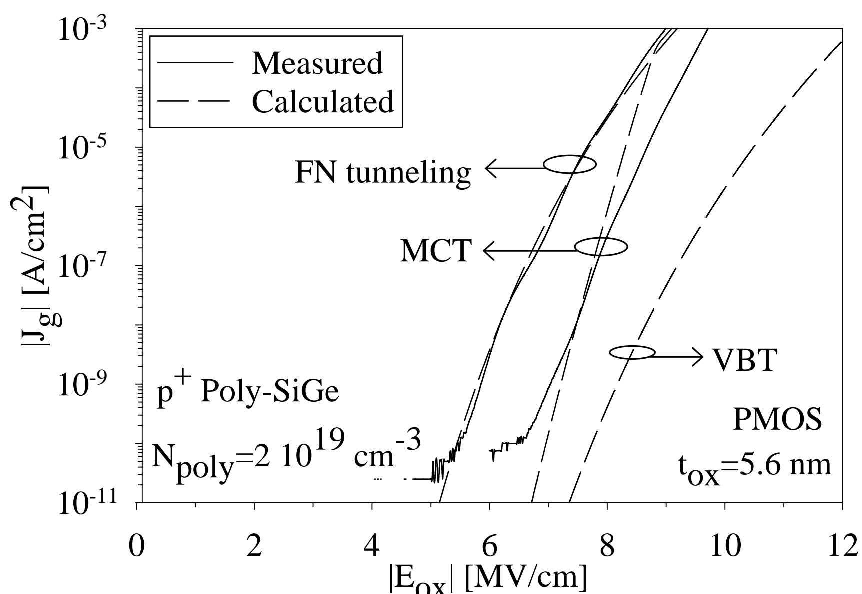

Figure 2.18: Minority Carrier Tunneling(MCT) in our p^+ poly-SiGe gate devices at -V_g. The poly-SiGe gate doping is estimated to be $N_{poly} \approx 2.0 \cdot 10^{19}$ cm^{-3}.

This is done by comparing the measured J-E_{ox} characteristics with the calculated curves for MCT and VBT. Figs. 2.17 and 2.18 displays the measured and calculated J-E_{ox} characteristics of our p^+ poly-Si and p^+ poly-SiGe PMOS gate devices. The actual voltage drop over the gate depletion layer V_{gate} is obtained in first order approximation from C-V measurements as was explained in section 2.3.

From Figs. 2.17 and 2.18 it can be observed that a reasonable fit with measurements is obtained, indicating that MCT might be the dominant conduction mechanism in our p^+ gate devices. For higher E_{ox} the fit is less accurate due to the limited generation of carriers available for tunneling. The difference in the MCT mechanism between p^+ poly-Si and p^+ poly-SiGe is related to the difference in bandgap $\mathcal{E}_g$ of the gate material (1.12 eV(poly-Si) and 0.9 eV(poly-SiGe)). At the same active gate doping concentration, the smaller bandgap of p^+ poly-SiGe reduces the amount of bandbending, and thus E_{ox}, needed to obtain the same tunneling current as for p^+ poly-Si (see Eq. 2.13). This means that the onset of conduction occurs sooner in p^+ poly-SiGe gate devices.

The dependence of the conduction mechanism at -V_g on gate RTA anneal temperature as observed in Fig. 2.9 is also explained using MCT. Gate doping at the poly-Si/SiO_2 interface increases with increasing gate RTA anneal temperature and a higher oxide field is needed for the same current.

It can thus be concluded that MCT might be important for the gate doping used in our p^+ gate devices. Refining the MCT model also requires inclusion of non-uniform injection (doping level varies over grain), band gap narrowing (BGN) at high active gate doping, quantization effects (at large band bending the first energy level does not coincide with the bottom of the conduction band, hence $\mathcal{E}_b$ effectively decreases) [76] and the limited generation of carriers available for tunneling. Also the interface states present at the poly/SiO_2 interface $D_{it,gate}$ have to be taken into account (J_{IST}).

This indicates that V_{gate}, which is an important parameter for MCT, can be determined with limited accuracy only.

2.5 Conclusions

In this chapter the C-V and I-V characteristics of MOS capacitors with p^+ and n^+ poly-Si and poly-SiGe gates are studied. For n^+-poly gate devices the J_g-E_{ox} characteristics are symmetric under -V_g and +V_g injection conditions and can be fitted well using the FN tunneling equation. For p^+-poly gate devices the J_g-E_{ox} characteristics depend on gate material and gate bias polarity. For -V_g a fit with the standard FN expression can not be obtained, unless *unphysical* fit parameters are used. A new model based on Minority Carrier Tunneling(MCT) from the gate is proposed for the I-V characteristics of p^+-poly gate devices under gate injection conditions (-V_g).

For very thin oxides (t_{ox} <4 nm) another contribution to the I-V curve at -V_g was observed. Hole tunneling from the substrate to the gate at -V_g is shown to take place in the low voltage regime. This hole current increases strongly with decreasing oxide thickness and might be important for the degradation of ultra-thin oxides with p^+ as well as n^+ gates.

Chapter 3

SILC in poly-Si and poly-SiGe CMOS capacitors

In this chapter the Stress-Induced Leakage Current(SILC) characteristics of NMOS and PMOS capacitors are studied. P^+ *and* n^+*-gates with poly silicon(poly-Si) and poly Silicon-Germanium(poly-*$Si_{0.7}Ge_{0.3}$*) were used to study the influence of gate workfunction on the SILC current. For* n^+ *gate devices, symmetric SILC with gate bias polarity is observed. No significant difference in SILC characteristics between the* n^+ *poly-SiGe and poly-Si reference devices is observed. For* p^+*-poly gate devices, asymmetric SILC (gate bias polarity) and reduced SILC for* p^+ *poly-*$Si_{0.7}Ge_{0.3}$ *is observed. The stress injection bias polarity dependence of* p^+ *gate devices is also studied. It is found that the amount of traps generated per unit of injected charge is approximately 10 times higher for injection of stress from the gate compared to substrate injection of stress. For very thin oxides (*t_{ox} *<4 nm) the SILC current at -*V_g *and at low voltages is dominated by hole tunneling from the substrate to the gate. This current is interpreted as trap assisted hole tunneling (HTAT). The effect of fluorine(F) on the SILC characteristics of* n^+ *poly-Si gate devices has also been studied. A small amount of F suppresses the generation of new oxide traps under high field electron injection, which leads to reduced SILC. At excessive F doses an increase of SILC is observed. Finally, a two-step tunneling model was developed to evaluate the SILC current under FN, MCT and VBT injection conditions. It is shown that this model successfully describes the experimental I-V characteristics for both* n^+ *and* p^+ *poly gate devices under substrate as well as gate injection conditions.*

3.1 Introduction

Stress-Induced Leakage Current(SILC) is the increase in low-level leakage through thin silicon dioxide(SiO_2) layers after the oxide has been subject to high electrical-field stressing. In the early eighties Maserjian *et al.* [32] reported on the degradation of thin SiO_2 layers which has been subject to electrical stress. They observed

that this leakage current at low and medium oxide fields (E_{ox} <7 MV/cm) increased with increasing electrical stress. This phenomenon is now commonly known as Stress-Induced Leakage Current or SILC [77, 78, 79, 80, 81].

Stress-Induced Leakage Current is defined as the increase in gate current density at low and medium oxide fields after electrical stress. The gate current density after stress $J_{g(stressed)}$ for n^+ poly gate devices can be expressed as :

$$J_{g(stressed)} = J_{g(fresh)} + J_{silc} = J_{DT} + J_{FN} + J_{silc} \tag{3.1}$$

From Eq. 3.1 it can be observed that stressing a thin oxide layer reduces its insulating capabilities, so SILC can become a major reliability problem. Whether this is the case depends on two necessary conditions which have to be fulfilled.

- *SILC is introduced*, i.e. the dielectric has to be subject to stress during device operation.
- *SILC is effective*, i.e. it degrades the functionality of the devices.

Both conditions are met in floating-gate Non-Volatile Memories (NVMs) as EEPROMs [82, 83, 84, 85] where *SILC is introduced* during program/erase(P/E) operations and *SILC is effective*, since repeated P/E-cycling enhances floating-gate charge loss which degrades the data retention times of the NVM devices. Thus in this case, SILC poses a major reliability problem and seriously limits the scaling of the gate oxide thickness for NVM [78].

In this chapter the Stress-Induced Leakage Current(SILC) characteristics of NMOS and PMOS capacitors are studied. P^+ and n^+-gates with poly silicon(poly-Si) and poly Silicon-Germanium(poly-$Si_{0.7}Ge_{0.3}$) were used to study the influence of gate workfunction on gate current and SILC currents.

First in section 3.2 a brief overview of the underlying conduction mechanism of SILC is given. The dependence of SILC on the electrical-stress conditions (injected charge, stress-current density, stress-temperature), measurement conditions (oxide field strength, measurement-temperature), dielectric layer thickness, etc. is reviewed in section 3.2.1. Most of it however is treated in more detail by other researchers, but in order to establish a complete picture it is included in this chapter as well.

Next, in section 3.3 experiments are done on n^+ poly-Si and n^+ poly-SiGe gate devices. Simple test structures, i.e. gate-controlled diodes and MOSFETs are used throughout this study. SILC in n^+ poly-Si gate devices has already been extensively studied [77, 86, 80, 81, 87, 88], so our results can be compared with results found by others. These measurements also provide us with a reference to enable a good comparison with p^+-poly gate devices.

In the next section of this chapter (section 3.4) the SILC characteristics of p^+ poly-Si and p^+ poly-SiGe gate devices are studied. For p^+-poly gate devices, asymmetric SILC (gate bias polarity) and reduced SILC for p^+ poly-$Si_{0.7}Ge_{0.3}$ is observed. The stress injection polarity dependence of p^+-poly gate devices is studied in section 3.4.3. In section 3.4.6 it is found that for very thin oxides (t_{ox} <4 nm) the SILC current at low negative gate voltages (-V_g) is dominated by hole tunneling from the substrate to the gate. This current is interpreted as trap assisted hole tunneling (HTAT).

Also the effect of fluorine(F) on the SILC characteristics of n^+ poly-Si gate devices has been studied (section 3.5). It has been observed that in fluorinated SiO_2 the presence of F suppresses the generation of new oxide traps under high-field electron injection. Hence fluorinated SiO_2 may be attractive to reduce SILC in NVM devices.

Finally in section 3.6, a quantitative model for SILC under FN, MCT and VBT injection conditions is developed. It describes the dependence of the SILC characteristics on the applied stress conditions, the measured field strength and gate bias polarity.

3.2 Physical nature of SILC

Since the first observation of SILC in the early eighties by Maserjian *et al.* [32] several models have been proposed to explain the physical origin of SILC. The most commonly accepted model is based on the *trap-assisted tunneling*(TAT) mechanism [77, 80, 26, 89].

According to this conduction mechanism the carriers *tunnel* from trap-to-trap in the oxide in a *field assisted way.* It has been observed that SILC is proportional to the neutral trap density (D_{ot}) in the bulk of the oxide, created during stress [26, 83, 87]. This trap assisted tunneling to these neutral traps can be a *multi-step process* if more than one trap is involved or a *two-step process* if the carriers tunnel from the cathode into the trap in the oxide and from the trap out to the anode. Since it was observed that even at breakdown, traps only form a small percentage of the oxide volume [90, 91], models based on a two-step tunneling process are therefore justified (see also section 3.6 on page 69).

Considering the energy location of the traps. Recently it has been observed by Takagi *et al.* [92, 93] that electron tunneling through the gate oxide, responsible for SILC, is accompanied by an energy loss of roughly $\mathcal{E}_{relax}$=1.5 eV. Although the origin of this energy relaxation has not been identified yet, a possible explanation is the energy loss due to multi-phonon emission [94, 95] in so-called *energy funnels* [96].

An energy funnel consists of a large density of energy states(DOS) which are

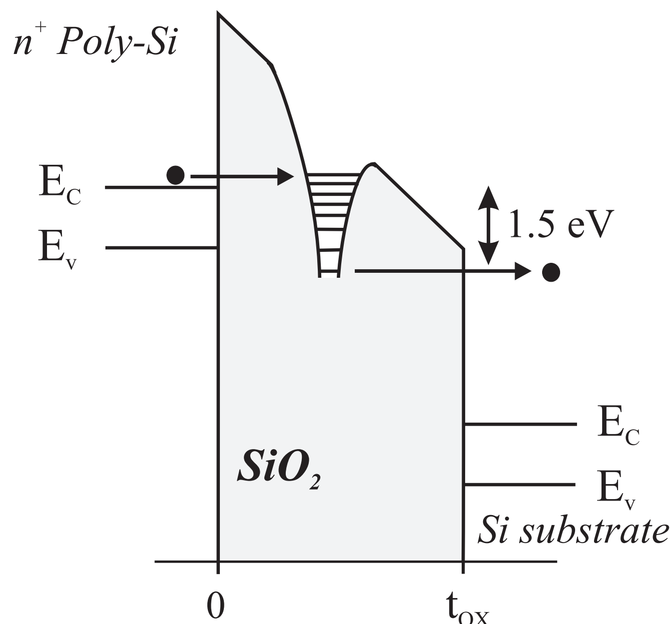

Figure 3.1: Schematic representation of the *Inelastic* Trap Assisted Tunneling(ITAT) mechanism, which is believed to be the dominant conduction mechanism for SILC. The energy relaxation occurs in so-called *energy funnels* by emission of multi-phonons.

present in the oxide trap as a result of a distortion-induced reconstruction of the SiO_2 lattice. This strongly suggest that SILC has to be described by an *inelastic* tunneling process (ITAT) [92, 69, 97] with an energy relaxation of $\mathcal{E}_{relax}$ ≈1.5 eV. A schematic illustration of the conduction mechanism of SILC based on energy funnels and ITAT is given in Fig. 3.1.

In the next section a brief overview of the dependence of SILC on the applied stress and measurement conditions is given.

3.2.1 Dependence of SILC on stress conditions

In this section the impact on the SILC characteristics of used stress conditions, measurement conditions and dielectric layer thickness is briefly reviewed.

- **Time dependence**

It was found by Moazzami *et al.* [80] that SILC is time dependent. They observed that SILC measured immediately after stress has been applied, decreases with time and saturates at a time-independent level. The total SILC current J_{silc} therefore consists of a time-dependent part and a time-independent part. This

means that J_{silc} can be written as the sum of a transient component J^{ac}_{silc} and a steady-state component J^{dc}_{silc} as given in Eq. 3.2:

$$J_{silc}(t) = J^{ac}_{silc}(t) + J^{dc}_{silc} \tag{3.2}$$

This time-dependence poses a restriction on the way we have to measure the SILC characteristics. For the transient component (AC-SILC) the current has to be monitored as a function of time, whereas for the steady-state component (DC-SILC) a current-voltage(I-V) measurement would be sufficient to determine the SILC [83, 84].

- **Oxide thickness**

Moazzami *et al.* [80] further observed a strong oxide thickness dependence on the steady-state SILC component. They found that the DC-SILC rapidly increases with decreasing oxide thickness. While hardly detectable in oxide thicknesses of t_{ox} >13 nm, the steady-state component completely dominates the transient component for t_{ox} <6 nm. This means that the DC-SILC becomes increasingly important with the further down-scaling of devices.

Since the oxide thicknesses considered in this study are all t_{ox} <6 nm, in the remainder of this chapter only DC-SILC will be discussed and will simply be noted as J_{silc}. In order to be certain that only the DC-SILC component is measured, multiple subsequent I-V measurements are performed using a slow sweep rate and are compared with each other. If the difference between two successive measurements is less than 1% the latter characteristic is chosen as an accurate measurement of the DC-SILC. This measurement method is similar as reported in [83].

- **Stress conditions**

Throughout this study, a constant current stress(CCS) is always used to inject electrons under high field injection conditions. Since during tunneling the current density is uniquely related to the oxide field strength for n^+ gate devices, CCS automatically implies stressing at a constant oxide field strength. This CCS is characterized by an injected charge fluence Q_{inj} and a stress current density J_{stress} which are related to each other by the amount of time which is stressed. This is expressed in Eq. 3.3 :

$$Q_{inj} = J_{stress} \cdot t \quad < Q_{bd} \tag{3.3}$$

Under these conditions, the injected charge fluence Q_{inj} and the stress current density J_{stress} can be controlled separately. However, no unique one-to-one correlation exists between the amount of injected charge fluence Q_{inj} and the stress

current density J_{stress} on the SILC characteristics. It was found by De Blauwe *et al.* [83, 88] that in a good approximation the dependence of the DC-SILC characteristics on Q_{inj} and J_{stress} can be described by an *empirical* equation in the form of a power law dependence, as expressed by Eq. 3.4 :

$$J_{silc} \sim Q_{inj}^{\alpha} \cdot J_{stress}^{\beta} \sim D_{ot} \tag{3.4}$$

Where D_{ot} is the neutral trap volume density generated during stress.

From Eq. 3.4 it can be noted that a one-to-one correlation exists between the neutral oxide trap density and the SILC [83, 87, 98, 88, 84] as should be expected. α and β depend on the oxide thickness t_{ox} and they have been determined to be α=0.5, β=0.2 (t_{ox}=7.1 nm), resp. β=0.4-0.6 (t_{ox}= 4.4 nm) [83, 99, 100, 88].

Stressing the gate oxide also leads to charge trapping in the oxide. These effects of trapped charge have to be eliminated, since charge trapping introduces an unwanted shift in the J-V_g curves. This means that no accurate comparison of the SILC current can be made for different stress conditions if trapped charge is present in the oxide. A measure for the amount of net trapped charge is given by the shift in gate-voltage ΔV_g under CCS conditions as a function of Q_{inj}. This shift is used to correct the gate voltage V_g, so the exact oxide field strength E_{ox} can be derived. Note that this can be verified experimentally, since the FN tunneling current also strongly depends on the amount of trapped charge. So if the FN tunneling current before and after CCS overlap in the high field region, the influence of charge trapping is assumed to be negligible.

- **Temperature dependence**

The effect of temperature on the SILC characteristics is an important parameter because often applications require reliable operation of devices at elevated temperatures, sometimes even up to T=150 - 200 °C. First, the dependence of the SILC on the temperature during electrical stress T_{inj} is discussed. It was found in [80, 89, 98] that the steady-state SILC at a fixed oxide field slightly increases with increasing T_{inj}. This increase is comparable with the increase of the total amount of neutral traps in the oxide and is independent of the measurement temperature T_{meas}. This supports the hypothesis that trap-assisted tunneling(TAT) is the main conduction mechanism for SILC. The field dependence of the DC-SILC is not influenced by T_{inj} as is evident from [98].

Next, the dependence of SILC on the temperature during measurement T_{meas} is described from [89, 98]. After CCS has been applied at room temperature (T_{inj}= 25 °C), the SILC characteristics were evaluated at different T_{meas}. No significant difference in DC-SILC was observed as a function of the measurement

temperature T_{meas} [98]. A small temperature dependence with an activation energy of about $\mathcal{E}_{act}$=0.1 eV has been observed at sub-room temperatures, down to liquid-nitrogen temperature (T=-147 °C) [89].

Since from above it can be concluded that the operating temperature has not a large impact on the SILC conduction mechanism, the temperature dependence is not taken into account in our study and all our measurements are done at room temperature , that is T=20 °C.

3.3 SILC in n^+ poly-Si and poly-SiGe gate devices

In this section the DC-SILC characteristics of n^+ poly-Si and n^+ poly-$Si_{0.3}Ge_{0.7}$ gate devices are studied for substrate (+V_g) and gate-injection (-V_g) conditions. The SILC current J_{silc} is monitored as a function of the CCS conditions (Q_{inj} and J_{stress}) by means of monitoring the I-V characteristics, which are measured according to the procedure described in section 3.2.1.

Electrical stress has been applied on A=$3.53 \cdot 10^{-3}$cm^2 n^+ poly-Si/SiGe NMOS capacitors using constant current stress conditions of J_{stress}=±0.1 mA/cm^2. The injected charge fluence Q_{inj} was chosen to range from 5μC/cm^2 to 1 C/cm^2. These stress conditions cover the most important range of stress conditions used in NVMs. The typical injected charge per P/E cycle of a NVM is Q_{inj} ≈5 - 10 μC/cm^2 at current densities in the range of J_{stress}=10 μA/cm^2 - 0.1 A/cm^2. The oxide electric field strength E_{ox} was determined by integration of the quasi-static C-V curves as was already explained in chapter 2.

3.3.1 Experimental Procedures

n^+ poly-Si/SiGe NMOS capacitors were fabricated on 10 Ω-cm p-type silicon substrates with 5.6 nm gate oxide thickness using the same process conditions as in section 2.2 on page 17.

3.3.2 Gate and substrate injection conditions

In Figs. 3.2 and 3.3 the J-E_{ox} characteristics of resp. n^+ poly-Si and n^+ poly-SiGe gate devices are shown after various stress intervals. The phenomenon of Stress-Induced Leakage Current (SILC) is clearly observed at low oxide fields, where the current is enhanced up to two orders of magnitude after electrical stress. In contrast to high oxide fields, where almost no increase in current is observed.

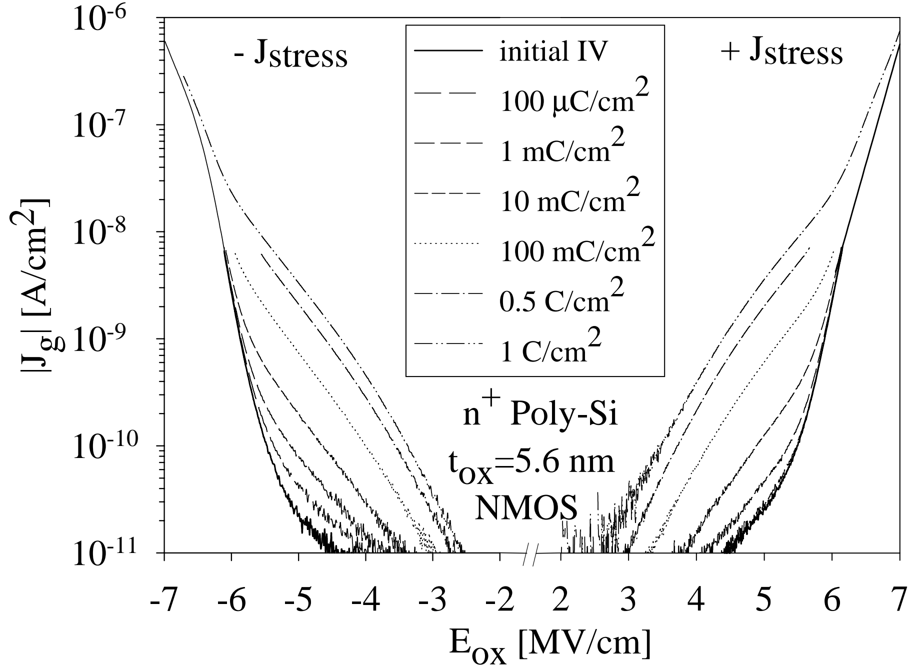

Figure 3.2: J-E_{ox} curves at +V_g and -V_g before and after stress (100 $\mu C/cm^2$ to 1 C/cm^2) for n^+ poly-Si gate material. Injection of stress takes place from the substrate (+V_g) and gate (-V_g) using CCS conditions of J_{stress}=±0.1 mA/cm^2.

From these Figs. it can be observed that there is no significant difference between n^+ poly-Si and n^+ poly-SiGe gate devices for both substrate (+V_g) and gate (-V_g) injection conditions. Also it can be noted that both J-E_{ox} characteristics are (almost) symmetric under gate bias polarity. This means that for n^+ gate devices there is (almost) no bias polarity dependence of the Stress-Induced Leakage Current. This agrees with results found by others [77, 86, 100] for n^+ poly-Si gate devices. Furthermore it can be noted from Figs. 3.2 and 3.3 that the SILC current J_{silc} increases exponentially with E_{ox}, though not as strong as for J_{FN}. This field dependence will be studied in more detail in the next section.

Fig. 3.4 displays the Stress-Induced Leakage Current(J_{silc}) for n^+ poly-Si and n^+ poly-SiGe gate devices as a function of the injected charge Q_{inj}. From Fig. 3.4 it is evident that the SILC current J_{silc} increases continuously with increasing injected charge Q_{inj}. Making use of Eq. 3.4 [83, 88] it is found that all curves can be described reasonable well by a power law dependence of J_{silc} on Q_{inj} with α=0.5. This is in agreement with results found by others for the same oxide thickness range.

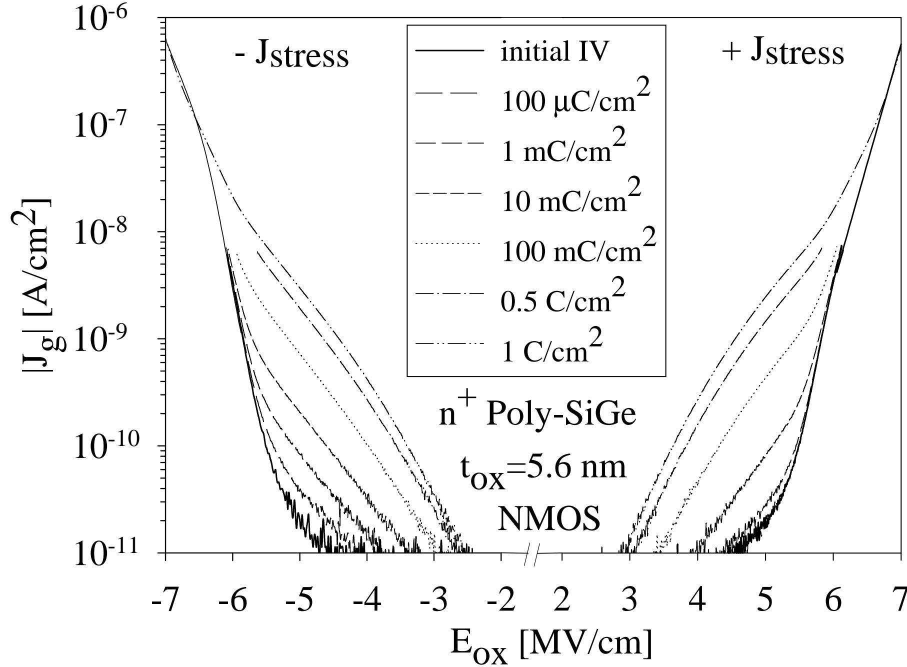

Figure 3.3: J-E_{ox} curves at +V_g and -V_g before and after stress (100 μC/cm^2 to 1 C/cm^2) for n$^+$ poly-$Si_{0.7}Ge_{0.3}$ gate material. Injection of stress takes from the substrate (+V_g) and gate (-V_g) using CCS conditions of J_{stress}=±0.1 mA/cm^2.

3.3.3 Field dependence of SILC in n$^+$-poly gate devices

In this section the dependence of the SILC current J_{silc} on the measurement electric field E_{ox} is discussed . It was already noted that J_{silc} depends exponentially on E_{ox}. In order to determine the field dependence of the SILC current J_{silc} for n$^+$ poly-SiGe gate devices, Fig. 3.3 is re-plotted on a Fowler-Nordheim (FN)-plot. These FN-plots of J_{silc} before and after stress are displayed in Figs. 3.5 and 3.6. From these Figs. it can be observed that the field dependence of the SILC current J_{silc} can be well described by a FN expression with a reduced barrier height of $\mathcal{E}_b$=0.8-0.9 eV for both substrate as well as gate injection conditions (see section 2.4 on page 23).

This field dependence of J_{silc} is similar to n$^+$ poly-Si gate devices and has first been observed by Olivo *et al.* [86] and was later confirmed by others [81, 83, 100].

It has been reported that the field dependence of J_{silc} is independent of the stress conditions Q_{inj} and J_{stress} and can therefore be written as :

$$J_{silc} \sim J_{FN}(\mathcal{E}_b = 0.8 - 0.9\ eV), \qquad \forall\ Q_{inj}, J_{stress} \tag{3.5}$$

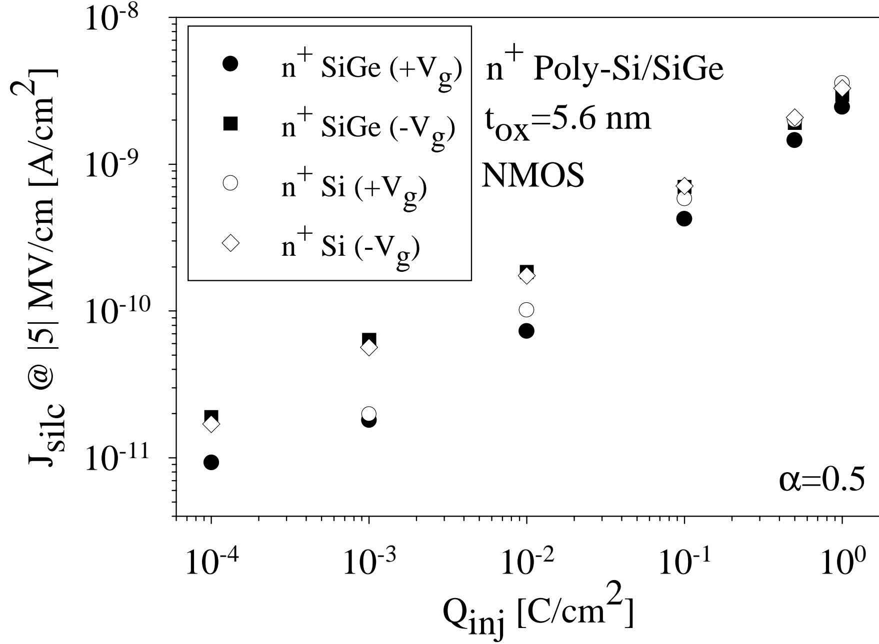

Figure 3.4: Stress-Induced Leakage Current(J_{silc}) as a function of the injected charge Q_{inj} for n^+ poly-SiGe and poly-Si at a fixed oxide field strength of $E_{ox}=\pm 5$ MV/cm.

It should however be stated that $\mathcal{E}_b$ only represents an *effective* barrier height and has no physical meaning. It is important to recall that Eq. 3.5 is just an empirical relation in which $\mathcal{E}_b$ acts as a fit parameter.

A correct physical (quantitative) model which is able to describe the conduction mechanism after stress (J_{silc}) will be developed in section 3.6.

3.3.4 Summary

In summary, it can be concluded that no significant difference between n^+ poly-Si and n^+ poly-$Si_{0.7}Ge_{0.3}$ gate devices is observed for gate (-V_g) and substrate (+V_g) injection conditions. The SILC current J_{silc} is (almost) symmetric with gate bias polarity. The field dependence of the SILC current in both devices can be well described by FN tunneling through an *effective* oxide barrier of reduced height with $\mathcal{E}_b$=0.8-0.9 eV. Furthermore, the SILC current is described in good approximation by a power law dependence of J_{silc} on Q_{inj} with α=0.5.

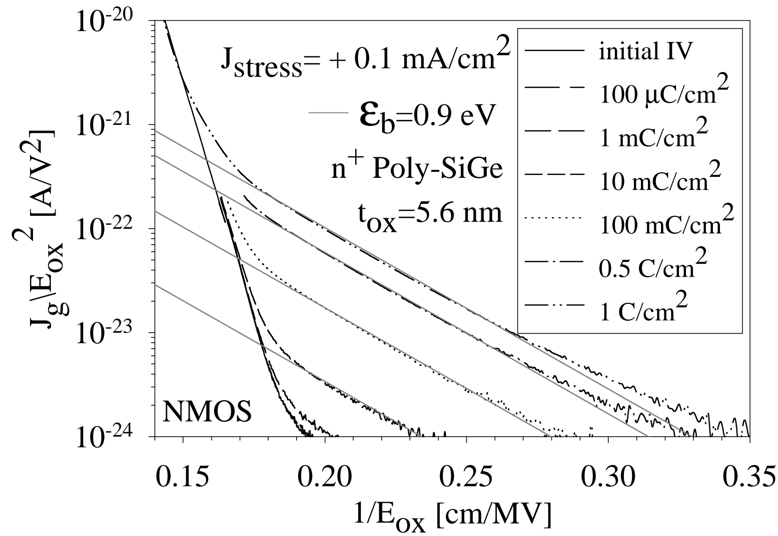

Figure 3.5: J/E_{ox}^2-$1/E_{ox}$ curves at $+V_g$ before and after stress for n^+ poly-$Si_{0.7}Ge_{0.3}$ gate material. From these plots which display the field dependence of the SILC characteristics, an *effective* barrier height of $\mathcal{E}_b$=0.9 eV can be derived.

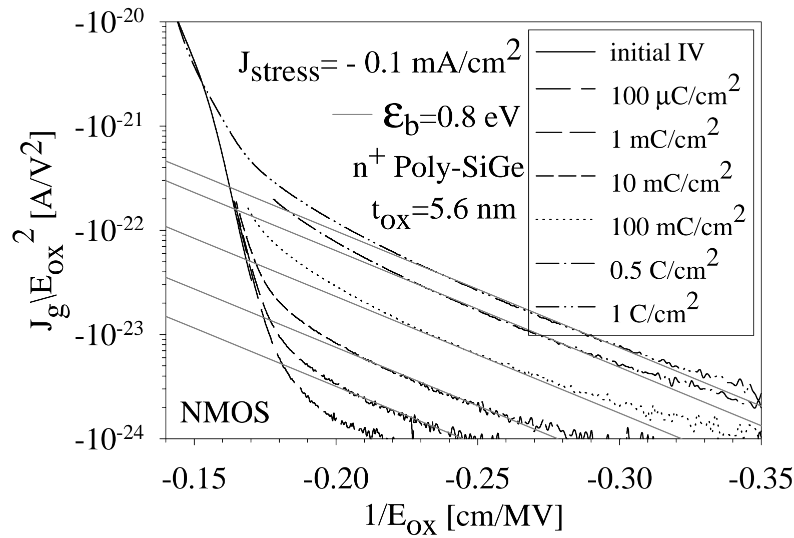

Figure 3.6: J/E_{ox}^2-$1/E_{ox}$ curves at $-V_g$ before and after stress for n^+ poly-$Si_{0.7}Ge_{0.3}$ gate material. From these plots which display the field dependence of the SILC characteristics, an *effective* barrier height of $\mathcal{E}_b$=0.8 eV can be derived.

3.4 SILC in p^+ poly-Si and poly-SiGe gate devices

In this section the SILC characteristics of p^+ poly-Si and p^+ poly-$Si_{0.3}Ge_{0.7}$ gate devices are studied for substrate (+V_g) and gate-injection (-V_g) conditions.

Electrical stress has been applied on $A=4.0\cdot10^{-4}cm^2$ p^+ poly-Si/SiGe PMOS capacitors using the same stress and measurement conditions as for n^+-poly gate devices (see section 3.3).

3.4.1 Experimental Procedures

p^+ poly-Si/SiGe PMOS capacitors were fabricated on 10 Ω-cm n-type silicon substrates with 5.6 nm gate oxide thickness using the same process conditions as in section 2.2 on page 17.

3.4.2 Gate and substrate injection conditions

In Figs. 3.7 and 3.8 the J-E_{ox} characteristics of resp. p^+ poly-Si and p^+ poly-SiGe gate devices at -V_g and +V_g after various stress intervals are depicted. It can be observed that for -V_g injection conditions, the SILC becomes apparent at much higher oxide fields than for substrate injection conditions (+V_g). At comparable oxide field the SILC is orders of magnitude smaller for -V_g stress than for +V_g stress. Hence there is a strong asymmetry of the SILC currents with injection polarity for p^+-gate devices. This is different from n^+-poly gate devices, where the SILC is almost symmetric with gate bias polarity (see section 3.3). For substrate injection conditions the field dependence of the SILC characteristics is comparable with that of n^+-poly gate devices. However, at -V_g the field dependence is very different from that of n^+-poly gate devices. This difference in field dependence will be examined in more detail in section 3.4.5.

It has been noted that SILC is proportional to the neutral trap density D_{ot} created during stress and models based on trap-assisted tunneling(TAT) are used to describe the SILC characteristics. The observed bias asymmetry in SILC for p^+-poly gate devices could be related to a larger tunneling barrier height for TAT (if VBT is dominant), a decreased carrier concentration at the p^+ poly-Si/SiGe-SiO_2 interface for MCT, or a different position of the traps for the -V_g stress condition. This will be investigated in more detail in section 3.6 were a quantitative model for the SILC characteristics is developed to calculate the SILC current under FN, MCT and VBT injection conditions.

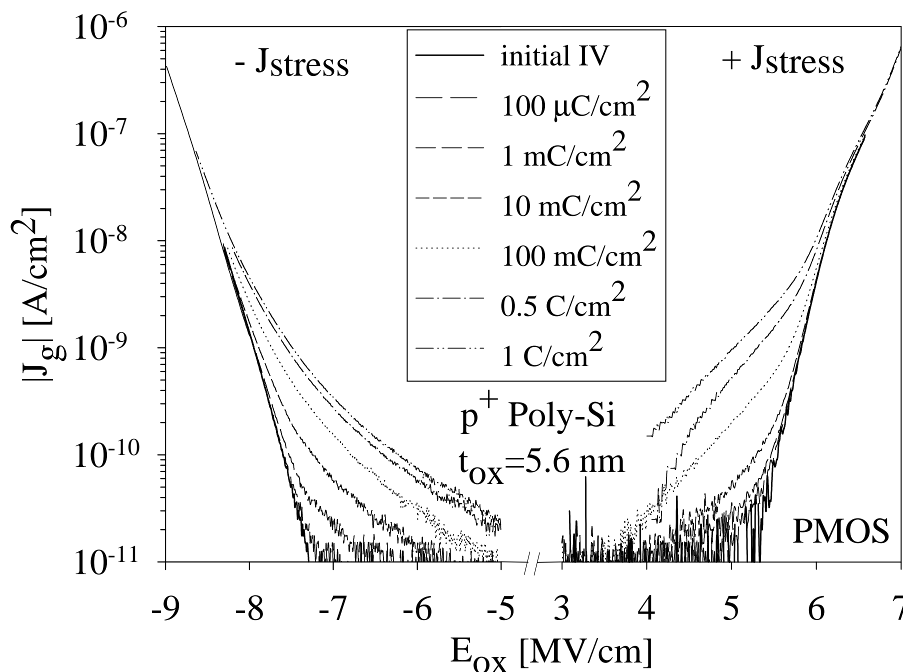

Figure 3.7: J-E_{ox} curves at +V_g and -V_g before and after stress (100 μC/cm^2 to 1 C/cm^2) for p$^+$ poly-Si gate material. Injection of stress takes place from the gate (-V_g) and substrate (+V_g) using CCS conditions of J_{stress}=±0.1 mA/cm^2.

Comparing the SILC characteristics of n$^+$-poly gate devices with p$^+$-poly gate devices (Fig. 3.2 with Fig. 3.7 and Fig. 3.3 with Fig. 3.8) it can be noted that at -V_g SILC is orders of magnitude smaller for p$^+$-poly gate devices. At +V_g injection conditions reduced SILC for p$^+$-poly gate devices compared to n$^+$-poly gate devices is observed. Furthermore, at +V_g the SILC characteristics for the p$^+$ poly-SiGe gate devices are much lower compared to the p$^+$ poly-Si gate devices.

The reduced SILC of the p$^+$ poly-SiGe gate devices compared to the p$^+$ poly-Si reference device for +V_g stress could be the result of a reduced Boron incorporation in the gate oxide. A larger solid solubility and smaller diffusivity of Boron in poly-SiGe lead to a reduced incorporation of Boron in the gate dielectric [101, 44, 40]. The incorporation of Boron in the gate oxide leads to an increase of neutral traps in the oxide and since the SILC current is proportional to the neutral trap density (see Eq. 3.4) this will lead to an increase in SILC current. Hence a lower neutral trap density and therefore reduced SILC for p$^+$ poly-SiGe gate devices is expected [83, 26, 102].

The increased SILC observed for the -V_g condition for p$^+$ poly-SiGe compared to p$^+$ poly-Si gate devices could be related to a shift in the valence band edge position of the gate. The shift in valence band for the p$^+$ poly-SiGe gate

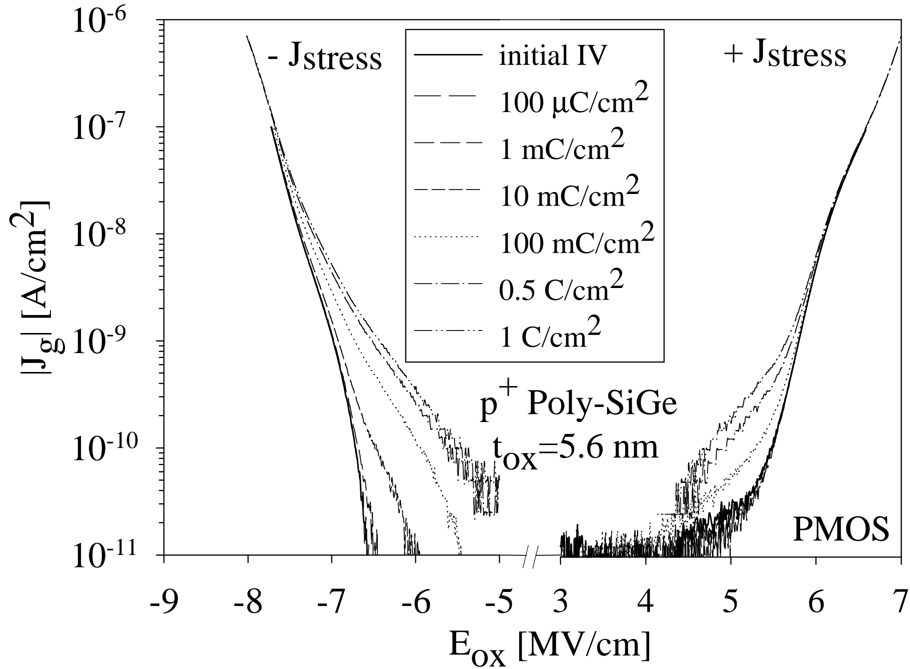

Figure 3.8: J-E_{ox} curves at +V_g and -V_g before and after stress (100 $\mu C/cm^2$ to 1 C/cm^2) for p^+ poly-$Si_{0.7}Ge_{0.3}$ gate material. Injection of stress takes from the gate (-V_g) and substrate (+V_g) using CCS conditions of J_{stress}=±0.1 mA/cm^2.

devices leads to a decrease in E_{ox} during stress at the same current (CCS), see chapter 2 Fig. 2.7. However it also reduces the barrier height $\mathcal{E}_b$ for tunneling to traps under VBT injection conditions and increases the minority carrier electron concentration in the conduction band of the gate at the same gate depletion for MCT. This might lead to an increase of SILC compared to the p^+ poly-Si gate reference devices.

3.4.3 Stress injection bias polarity dependence

In the previous section the SILC characteristics of the p^+-poly gate devices were stressed and measured under the same gate bias polarity conditions. This means that stressing took place under -V_g injection conditions and afterwards the SILC characteristics were also measured for -V_g gate bias polarity. The same was done for substrate (+V_g) injection conditions.

In this section the influence of stress bias polarity on the SILC current J_{silc} is examined. It was already observed in chapter 2 (section 2.4.1 on page 24) that there is a strong asymmetry of the tunnel current for p^+-poly gate devices with gate bias polarity. From Fig. 2.7 it is evident that stressing under CCS conditions

will take place at much higher oxide fields for gate (-V_g) compared to substrate (+V_g) injection conditions. For gate injection conditions, stressing takes place at J_{stress}=-0.1 mA/cm^2 at an oxide field strength of E_{ox}= -10.0 MV/cm(poly-Si) and -9.2 MV/cm(poly-SiGe), while for substrate injection conditions stressing takes place at J_{stress}=+0.1 mA/cm^2 under an oxide field strength of E_{ox}=8.3 MV/cm(poly-Si and poly-SiGe).

So by measuring the SILC current in the opposite bias polarity as the stress polarity, the influence of stress bias polarity on the SILC characteristics can be evaluated.

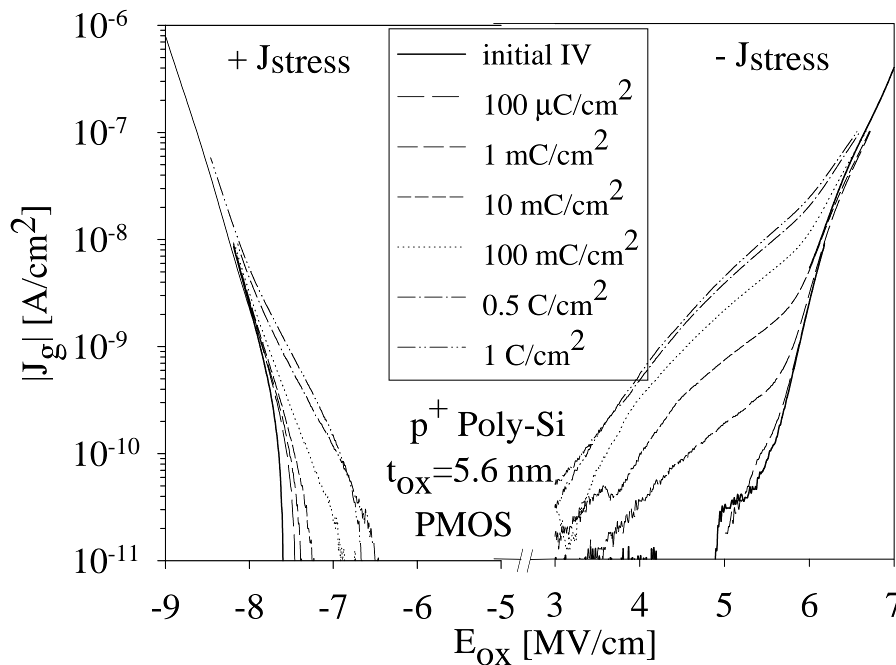

Figure 3.9: J-E_{ox} curves at +V_g and -V_g before and after stress (100 μC/cm^2 to 1 C/cm^2) for p$^+$ poly-Si gate material. Injection of stress takes place from the substrate (+V_g) for -V_g and gate (-V_g) for +V_g using CCS conditions of J_{stress}=±0.1 mA/cm^2.

Figs. 3.9 and 3.10 display the J_g-E_{ox} characteristics of p$^+$ poly-Si and p$^+$ poly-SiGe gate devices at -V_g and +V_g after opposite stress bias polarity conditions. By comparing Fig. 3.9 with Fig. 3.7 and Fig. 3.10 with Fig. 3.8 a significant increase in SILC current for +V_g is observed, while at -V_g the SILC current is significantly reduced. The increase of SILC for -V_g stress is most likely related to the higher oxide field at -V_g compared to +V_g during stress at the same stress current(CCS).

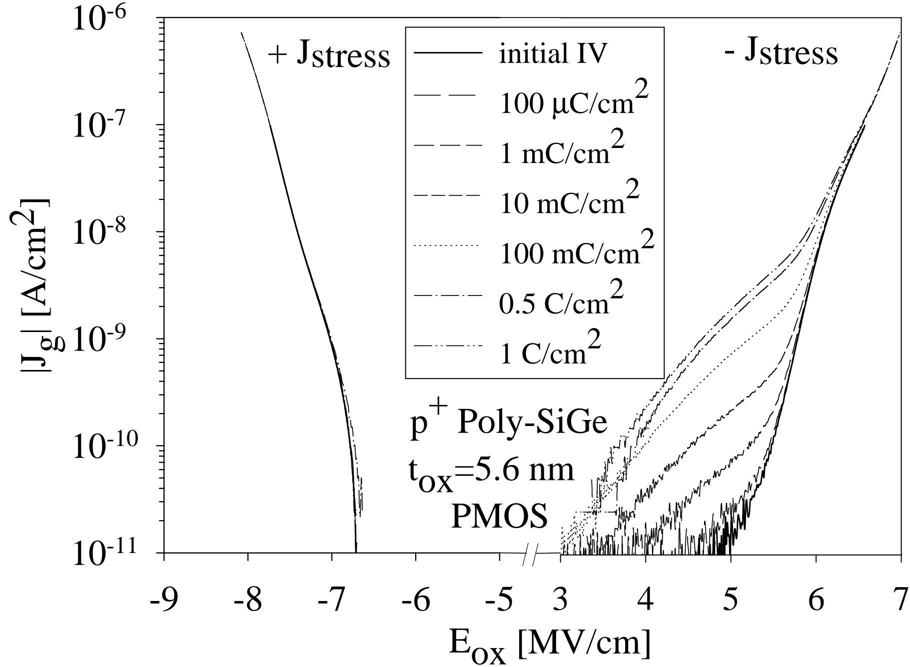

Figure 3.10: J-E_{ox} curves at +V_g and -V_g before and after stress (100 μC/cm^2 to 1 C/cm^2) for p^+ poly-$Si_{0.7}Ge_{0.3}$ gate material. Injection of stress takes from the substrate (+V_g) for -V_g and gate (-V_g) for +V_g using CCS conditions of J_{stress}=±0.1 mA/cm^2.

This seems to be in contradiction with Eq. 3.4, the *empirical* equation found by De Blauwe *et al.* [83, 88]. This equation states that the SILC current J_{silc} should be proportional to $Q_{inj}^{\alpha} \cdot J_{stress}^{\beta}$. This indicates that stressing at a constant current J_{stress}, will result in the same SILC current J_{silc}. This is in contrast with our findings.

Since it is assumed that there exists a one-to-one correlation between the amount of oxide traps D_{ot} and SILC current J_{silc}, it can be concluded that under -V_g stress conditions, due to a higher oxide field, more neutral oxide traps per unit injected charge are generated. This will be examined in more detail in the next section.

3.4.4 SILC generation rate in p^+ gate devices

In this section the SILC generation rate in our p^+-poly gate devices will be reviewed on the basis of our findings. Fig. 3.11 displays the Stress-Induced Leakage Current measured at +V_g as a function of the injected charge Q_{inj} for both stress bias polarity conditions. It can be observed from Fig. 3.11 that the increase in

SILC current as a function of the amount of injected charge Q_{inj} is identical for both stress bias polarity conditions. This indicates that the first part of Eq. 3.4 is also valid for our p^+ gate devices under both stress injection conditions. A good fit with experimental data is obtained with α=0.5.

It is now possible to derive the SILC generation rate of our p^+ gate devices, which is defined as [30] :

$$P_g(silc) = \frac{\Delta J_{silc}}{J_{g(fresh)} \Delta Q_{inj}} \sim \frac{\Delta D_{ot}}{\Delta Q_{inj}} \tag{3.6}$$

From Fig. 3.11 it can be observed that the SILC generation rate of our p^+-poly gate devices is approximately 10 times higher for -J_{stress} as for +J_{stress} bias injection conditions (poly-Si: 10×, poly-SiGe: 13×). So from Eq. 3.6 it can be concluded that the amount of oxide traps D_{ot} generated per unit of injected charge, is approximately 10 times higher for -J_{stress} as for +J_{stress} bias injection conditions. This increase of SILC current is most likely caused by the higher oxide field strength for -V_g compared to +V_g stress bias polarity conditions.

As was already noted in the previous section, this seems to be in contradiction with Eq. 3.4 which was derived for n^+ poly-Si gate devices. However, one should remember that J_{stress} and E_{ox} are directly related to each other for n^+-poly gate devices via the Fowler-Nordheim tunneling equation (see Eq. 2.6). So an increase in stress current automatically implies an increase in oxide field strength E_{ox}. Since from Fig. 3.11 it can be observed that the trap generation characteristics are identical for all stress fields, it can be concluded that J_{stress} determines the wearout (SILC) of the oxide and that the oxide field strength E_{ox} merely acts as an acceleration factor for the degradation process.

It should be noted that this was also found by DeGraeve *et al.* [17]. They also observed that for n^+ poly-Si gate devices electron trap generation is identical for all stress fields and concluded that the electric field acts as an acceleration factor for the degradation process. The increase in SILC current with increasing electrical field strength at the same current could be related to the increase in kinetic energy of the electrons as they travel through the oxide. Following the AHI or hydrogen release model, these *hot-electrons* have higher kinetic energy when they reach the anode and thereby have a higher probability of creating a *hot-hole* resp. H^+ which can tunnel back into the oxide. Also the holes and H^+ can be more energetic. This will lead to more neutral oxide traps to be created and hence to an increase in SILC. So it can be concluded that both the electron flux (J_{stress}) and the total energy released at the anode ($\sim E_{ox}$) are important parameters in the SILC degradation process.

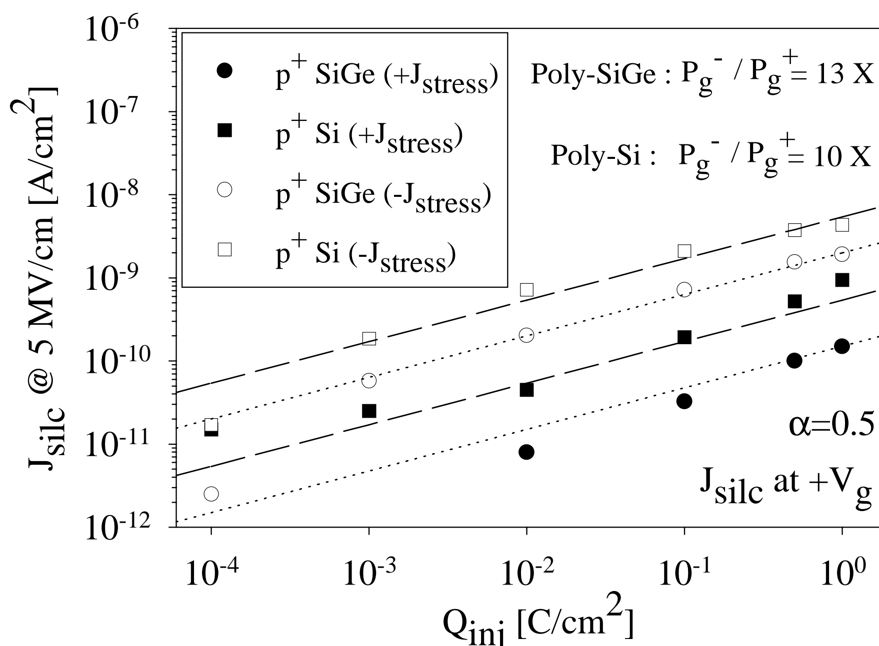

Figure 3.11: Stress-Induced Leakage Current(J_{silc}) as a function of the injected charge Q_{inj} for p^+ poly-SiGe and poly-Si at a fixed oxide field strength of E_{ox}=5 MV/cm after J_{stress}=+0.1 mA/cm^2 and J_{stress}=-0.1 mA/cm^2.

3.4.5 Field dependence of SILC in p^+-poly gate devices

In this section the field dependence of J_{silc} for p^+-poly gate devices is discussed. For $+V_g$ the SILC current after stress can be described well with a FN dependence using an *effective* barrier height of $\mathcal{E}_b$=0.9 eV as was also found for n^+-poly gate devices (see Fig. 3.12). For gate injection conditions ($-V_g$) J_{silc} can not be described by a FN expression with fixed (reduced) barrier height. Variations in shape occur with stress time and oxide field strength, as can be seen from Fig. 3.13. A crude (unphysical) FN fit of the SILC current results in a barrier height of approximately $\mathcal{E}_b$=2 eV, indicating a much stronger field dependence.

Till so far we only investigated the SILC characteristics of n^+ and p^+ MOS capacitors on 5.6 nm gate oxide thickness. However, the reliability of ultra-thin gate dielectrics (t_{ox} <4 nm) is of increasing concern because of the significant direct tunneling currents flowing during normal device operation. It has been shown that for a fixed trap density, the SILC current increases exponentially as the oxide thickness decreases [103, 104, 102]. This means that SILC is becoming more and more important for thinner oxides.

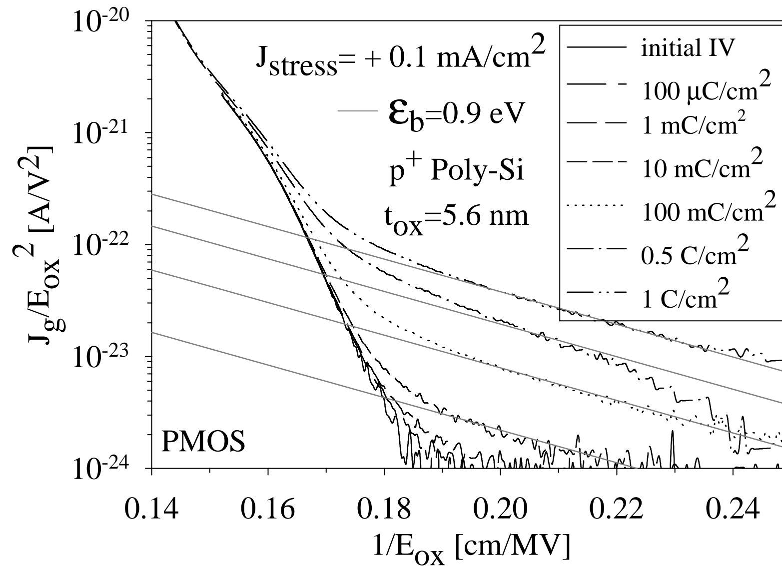

Figure 3.12: J/E_{ox}^2-$1/E_{ox}$ curves at $+V_g$ before and after stress for p^+ poly-Si gate material. From these plots which display the field dependence of the SILC characteristics, an *effective* barrier height of $\mathcal{E}_b$=0.9 eV can be derived.

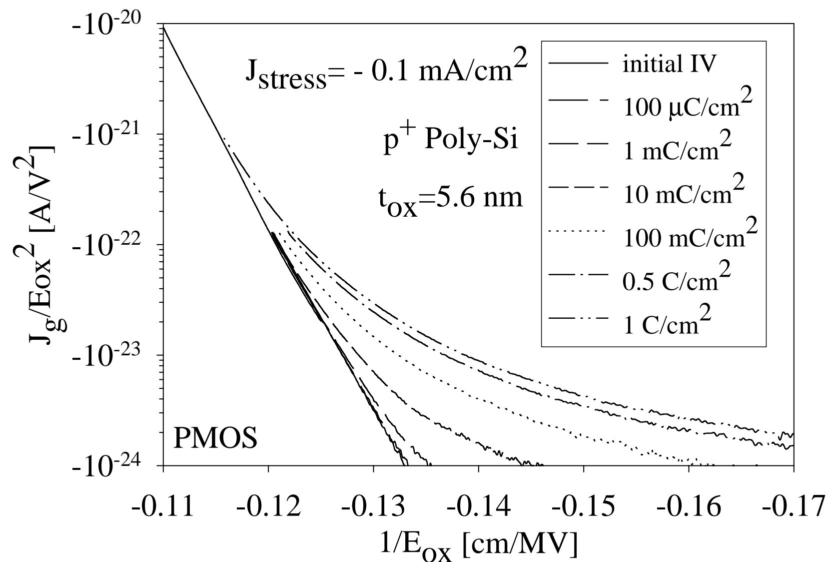

Figure 3.13: J/E_{ox}^2-$1/E_{ox}$ curves at $-V_g$ before and after stress for p^+ poly-Si gate material. From these plots no fixed *effective* barrier height can be derived, since variations in shape occur with stress time and oxide field strength.

Nevertheless, for sub-5 nm oxides the SILC current is hard to detect, since the DT current dominates the SILC current. However, for very thin oxides (t_{ox} <4 nm) it was observed in chapter 2 (section 2.4.1 on page 24) that holes can tunnel from the substrate to the gate in the low voltage regime. The influence of electrical stress on this hole tunneling current has not been investigated yet. This will be the subject of the next section.

3.4.6 Trap assisted hole tunneling(HTAT) in p^+-poly gate devices

In this section the influence of electrical stress on the hole tunneling current in very thin p^+ poly-Si gate oxides (t_{ox} <4 nm) is investigated. For these thin oxides it was observed in chapter 2 that holes can tunnel from the substrate to the gate in the low voltage regime. However the influence of electrical stress on this hole tunneling current has not been studied yet.

3.4.7 Gate injection conditions

To discriminate between electron and hole currents carrier separation measurements on p^+ poly-Si PMOS gate devices are performed with source/drain and n-type Si substrate grounded, see chapter 2 (Fig. 2.12). Fig. 3.14 displays the J_g-V_{ox} characteristics before and after stress of p^+ poly-Si gate devices with 3.1 nm oxide thickness. Injection of stress takes place from the gate (-V_g) under CCS conditions of J_{stress}=-1.0 mA/cm^2.

From Fig. 3.14 it can be seen that for -V_g bias condition a hole current is flowing from the source/drain to the gate in the low voltage regime. This hole current increases strongly with increasing electrical stress. Therefore this current is interpreted as trap assisted hole tunneling (HTAT). Also it can be noted that after stress (Q_{inj}=-300 mC/cm^2) for V_{ox} <-1.0 V the gate current I_{gate} is dominated by the source/drain current $I_{s/d}$, suggesting that in this voltage regime trap assisted hole tunneling is the dominant conduction mechanism. As was already stated in chapter 2, this hole current increases strongly with decreasing oxide thickness and can be important for degradation of ultra-thin oxides, since hot holes are no longer needed to trigger the breakdown process as was required according to the Anode Hole Injection model(AHI) [22, 23, 24]. This increase in hole current after stress is also important for very thin oxide n^+-poly gate devices at -V_g condition and as MCT for +V_g.

3.4.8 Summary

In summary, both the position of the valence band of the gate material and Boron penetration into the gate oxide strongly influence the SILC characteristics for p^+-

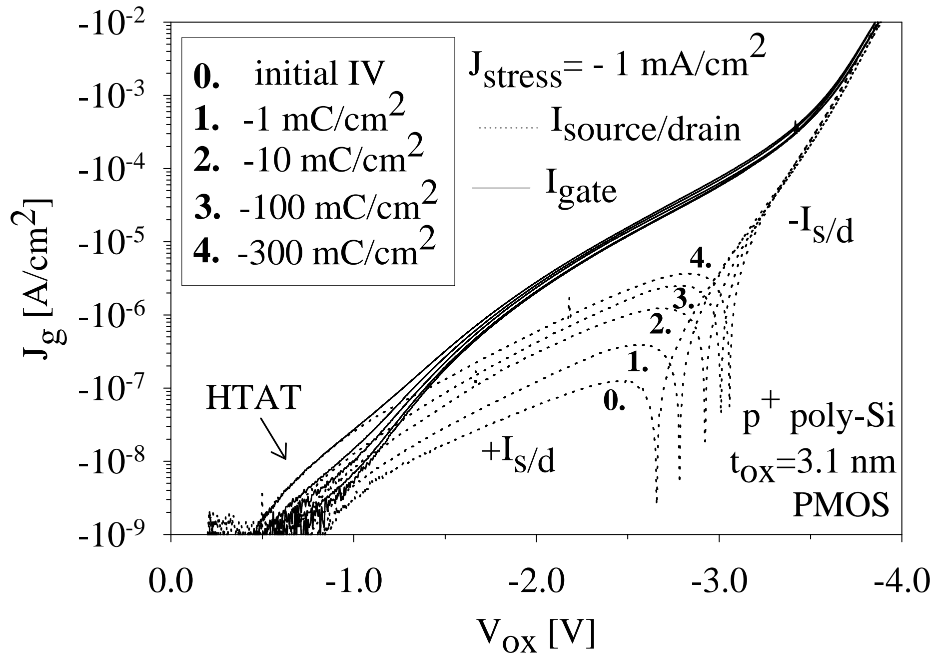

Figure 3.14: Carrier separation measurements on p$^+$ poly-Si gate PMOS devices with 3.1 nm oxide thickness before and after stress (-1 mC/cm^2 to -300 mC/cm^2). Injection of stress takes place from the gate (-V$_g$) under CCS conditions of J$_{stress}$=-1.0 mA/cm^2. A large increase of hole current is observed with increasing electrical stress.

poly gate devices. It was observed that at -V$_g$ SILC is orders of magnitude smaller for p$^+$-poly gate devices compared to n$^+$-poly gate devices. Also at +V$_g$ injection conditions reduced SILC for p$^+$-poly gate devices compared to n$^+$-poly gate reference devices is observed. Furthermore, at +V$_g$ the SILC characteristics for p$^+$ poly-SiGe gate devices are much lower compared to p$^+$ poly-Si gate devices. It can thus be concluded that the degradation of p$^+$-poly gate devices due to SILC is not worse, but presumably even better compared to n$^+$-poly gate devices.

The reduced SILC observed in p$^+$-poly gate devices for -V$_g$ polarity could be attractive for non-volatile memory devices. Boron-doped p$^+$ poly-SiGe may be a very interesting gate material due to low SILC at +V$_g$ and better gate oxide quality compared to p$^+$ poly-Si. For very thin oxides (t$_{ox}$ <4 nm) the SILC current at low -V$_g$ voltages is dominated by holes tunneling from the substrate to the gate. This increase in hole current after stress might be important for very thin gate oxide reliability.

3.5 SILC in F implanted n^+ poly-Si gate devices

In the previous sections the SILC characteristics for p^+-poly gate devices was studied. Gate doping of these devices was done using BF_2^+ as implantation species. Recently, it has been reported that the incorporation of fluorine in the gate oxide of MOSFETs improves the reliability of the SiO_2 under both hot electron and Fowler-Nordheim (FN) injection stress [105, 106, 107]. A drastically improvement of the Q_{bd} distribution tail of the Weibull plot by an appropriate fluorine incorporation into SiO_2 has been reported by Mitani *et al.* [108], while maintaining the average Q_{bd} value [109, 108].

Moreover, it has been observed by Vishnubhotla *et al.* [110] that in fluorinated SiO_2 the presence of F suppresses the generation of *new* oxide traps under high-field electron injection. Hence fluorinated SiO_2 may be attractive for reduced SILC.

This indicates that we have to investigate the influence of fluorine on the SILC characteristics, since F is also present in/near the oxide of our p^+-poly gate devices. This is because gate doping of our devices was done using BF_2 as implantation species.

The influence of fluorine on the SILC characteristics of ultra-thin oxides with a n^+ poly-Si gate material is therefore studied in this section. The reason for studying n^+ poly-Si MOS capacitors instead of comparing B doped samples with BF_2 doped p^+ poly-Si capacitors is that Boron can easily penetrate the gate oxide which leads to an enhanced neutral trap density and increased SILC. Moreover, BF_2 implants cause enhanced Boron diffusion in the gate oxide relative to B implants. So by using F implanted n^+ poly-Si MOS capacitors the influence of fluorine on the SILC characteristics can be studied unambiguously.

In this section the effects of fluorine on the Stress-Induced Leakage Current (SILC) characteristics of ultra-thin oxides with a n^+ poly-Si gate material have been studied. The fluorine was implanted in the poly-Si gate and introduced in the underlying 4.6 nm gate oxide by means of diffusion at elevated temperatures.

3.5.1 Experimental Procedures

n^+ poly-Si NMOS capacitors were fabricated on 5-10 Ω-cm boron doped p-type silicon substrates. A high quality gate oxide with 4.6 nm thickness (ellipsometric) was grown in diluted dry oxygen. An undoped poly-Si layer (400 nm thick) was deposited using a LPCVD system and implanted with 100 keV, $8.0 \cdot 10^{15}$ cm^{-2} As^+. After this fluorine was implanted at 40 keV with varying doses, ranging from $2.0 \cdot 10^{14}$ cm^{-2} to $3.0 \cdot 10^{15}$ cm^{-2}, followed by an anneal at 900°C for 30 minutes to activate the dopant and to diffuse the fluorine in the underlying gate

oxide. Note that F is not directly implanted into the gate oxide in order to avoid damage caused by implantation.

3.5.2 Effect of F on the gate oxide thickness

Quasi-static C-V_g curves of the unstressed n^+ poly-Si NMOS capacitors with various F implantations are shown in Fig. 3.15. From this a flatband voltage of V_{fb}=-0.95 V can be derived. Note that the oxide thickness (t_{ox}) increases with increasing F incorporation. This is consistent with reports on a t_{ox} increase for BF_2 doped p^+-poly Si gates with 3.5 nm oxide thickness [111] and for thicker oxides [112, 108].

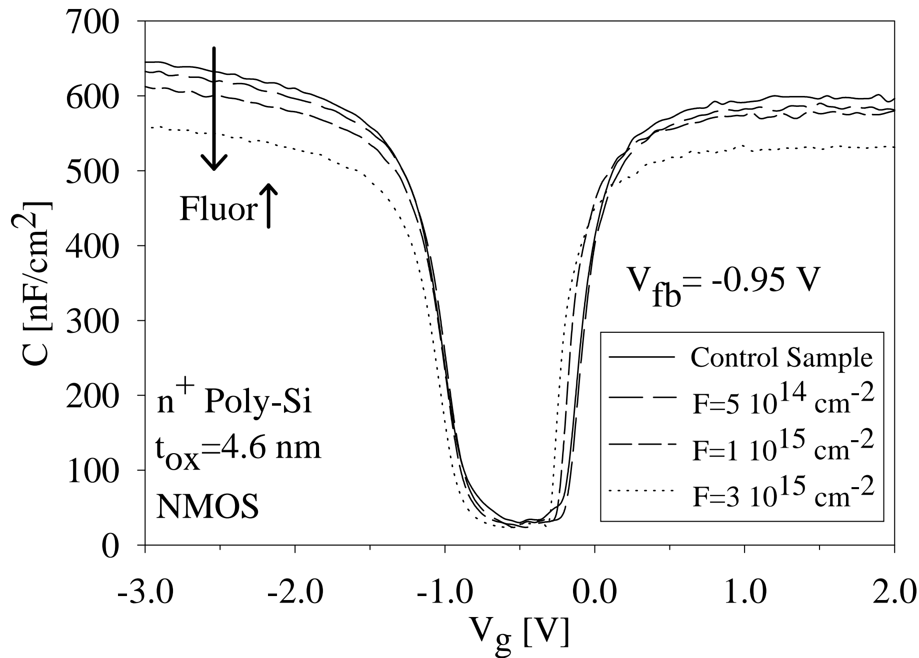

Figure 3.15: Quasi-static C-V_g curves for n^+-poly Si NMOS capacitors with 4.6 nm oxide thickness and various fluorine implants.

Fig. 3.16 displays the increase of the gate oxide thickness as a function of F implantation. Note that the increase in oxide thickness Δt_{ox} is almost linear dependent (with a slope of $\approx$1.1) on the implanted F dosage. This is different from reports on a Δt_{ox} with increasing F dosage observed by Mitani *et al.* [108]. They observed that the increase in oxide thickness is dependent on the implanted F dosage with the square root of F for various oxide thickness. They also concluded that the increase in t_{ox} is independent on the initial oxide thickness. It should however be noted that in both cases the implanted F dosage in the poly-Si gate

was taken as a parameter and not the actual F concentration in the SiO_2. Different anneal temperatures and anneal times might lead to different concentrations of F atoms in the underlying gate oxide and thus a different dependence of Δt_{ox} on the implanted F dosage can be observed.

It should be noted that this increase in oxide thickness can be related to an *actual* increase of oxide thickness or a decrease in the dielectric susceptibility (ϵ_{ox}) of the gate oxide, which leads to an *artificial* oxide thickness increase. It has been reported by Wright *et al.* [112] by using both electrical and optical methods, that this increase is caused by an actual increase of the oxide thickness. Also Mitani *et al.* [108] found that the physical oxide thickness actually increases with increasing F incorporation by comparing TEM images of the gate oxide for various F implants. A model which will explain this increase of oxide thickness will be given below.

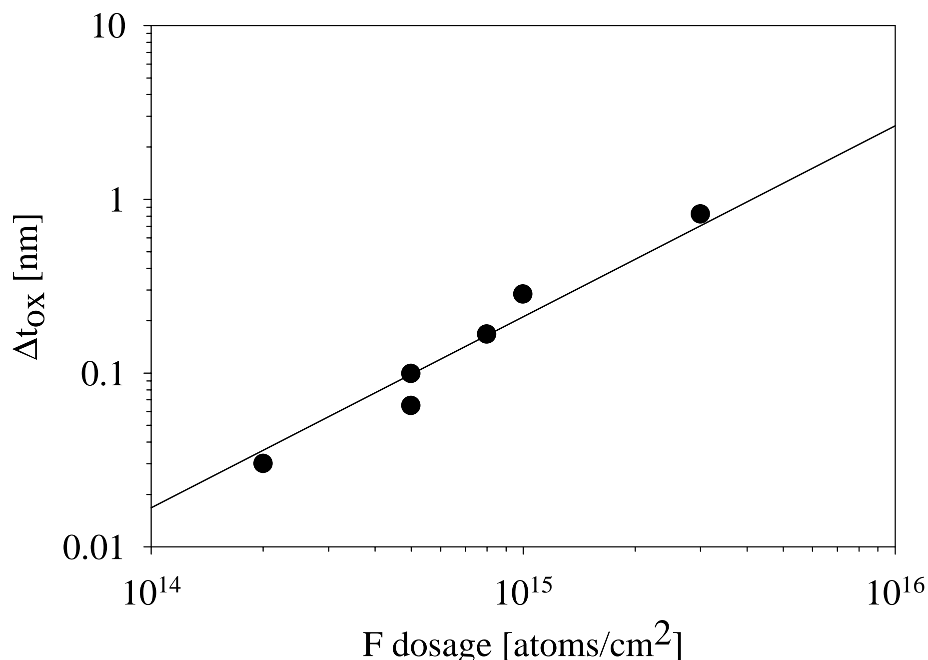

Figure 3.16: Increase in oxide thickness evaluated by quasi-static C-V_g measurements as a function of the implanted F dosage.

3.5.3 Gate injection conditions

Electrical stress has been applied using constant current stress conditions of J_{stress}=-0.1 mA/cm^2 on A=1.0·10^{-4}cm^2 n$^+$ poly-Si NMOS capacitors using the same stress and measurement conditions as in section 3.3.

In Fig. 3.17 the J_g-E_{ox} characteristics of the n^+ poly-Si gate devices with different fluorine implants after various stress intervals are depicted. First it should be noted that the initial (fresh) J_g-E_{ox} characteristics change under influence of the fluorine implants. A transition from Direct Tunneling (DT) and Fowler-Nordheim (FN) tunneling to entirely FN tunneling can be observed with increasing fluorine implant. This is related to an *actual* increase Δt_{ox} of the gate oxide thickness, with increasing fluorine implant.

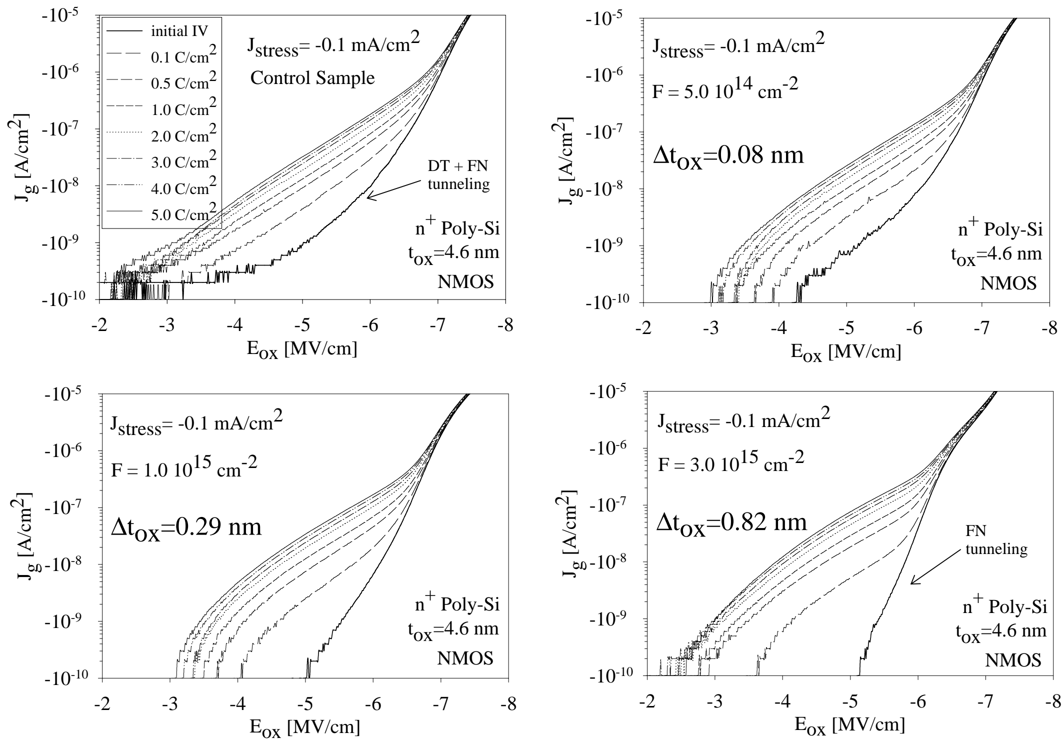

Figure 3.17: J-E_{ox} curves at -V_g before and after stress (0.1 C/cm^2 to 5.0 C/cm^2) for n^+ poly-Si gate material with various fluorine implants. Injection of stress takes from the gate (-V_g) using CCS conditions of J_{stress}=-0.1 mA/cm^2.

To evaluate the SILC as a function of the implanted fluorine, the leakage current $J_{silc} = J_{g(stressed)} - J_{g(fresh)}$ was plotted as a function of the injected charge Q_{inj} for various F implanted doses at a fixed oxide field strength of E_{ox}=-5 MV/cm. Figure 3.18 clearly shows that the SILC is reduced by F incorporation with an implanted dose of F<1.0·10^{15} cm^{-2}. However, for higher fluorine doses (3.0·10^{15} cm^{-2}) an increase of the SILC is observed. These results indicate that

an optimum value for the implanted fluorine dose exists. A small amount of F leads to reduced SILC, while higher levels of F result in enhanced SILC. Comparing the influence of fluor on the SILC and Q_{bd} characteristics, Mitani *et al.* [108] found an improvement of the Q_{bd} distribution tail of the Weibull plot by an appropriate fluorine incorporation into SiO_2, while maintaining the average Q_{bd} value. The reason why fluorine only leads to a small improvement in both SILC and Q_{bd} can be related to the incorporation of F in the gate oxide. It was found by Mitani *et al.* [108] that F atoms pile up at the poly-Si/SiO_2 and SiO_2/mono-Si interfaces instead of being distributed homogeneously over the gate oxide. This explains why the effect of F on the SILC characteristics (and Q_{bd}) is minimal. Next, our results will be explained using a simple model proposed in literature.

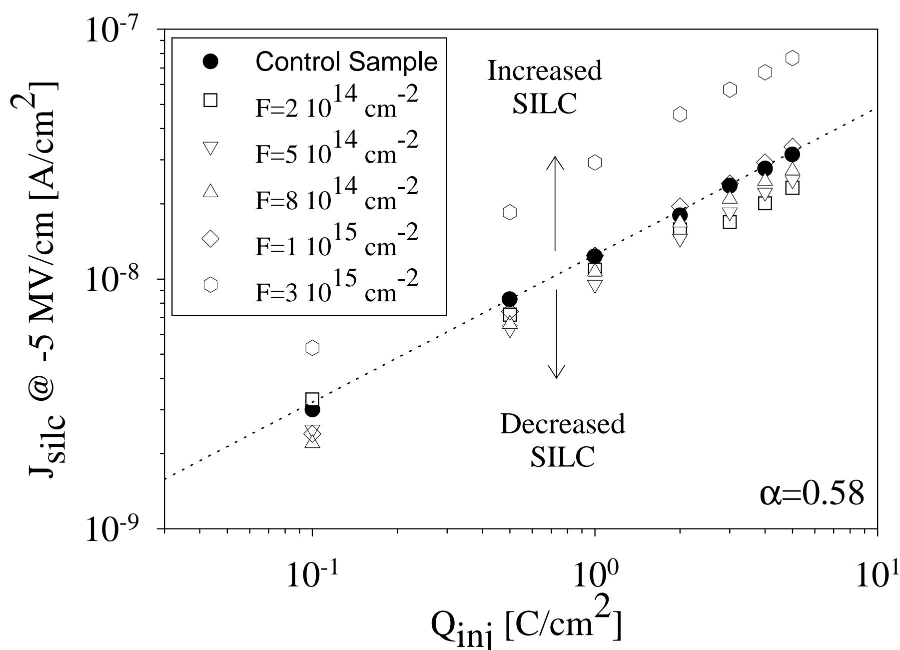

Figure 3.18: Stress-Induced Leakage Current(J_{silc}) as a function of the injected charge Q_{inj}. The leakage current is plotted for various fluorine implants at a fixed oxide field strength of E_{ox}=-5 MV/cm.

Following a simple model proposed by Wright *et al.* [112] our results can be explained as follows. First, fluorine diffuses and bonds to dangling bonds near the Si/SiO_2 and poly-Si/SiO_2 interfaces. Also the weak Si-H (3.18 eV) bonds at the interfaces are replaced by the much stronger Si-F (5.73 eV) bonds. This leads to an improved interface hardness against radiation and hot-electron damage. After these interface regions have been saturated with fluorine, additional

incorporation of fluorine occurs primarily in the gate oxide. Initial neutral traps in the gate oxide are quickly passivated by a small amount of F and it suppresses the generation of new oxide traps under high-field electron injection [110], which lead to reduced SILC. Also the reduction in trap generation due to the structural relaxation of the strained SiO_2 structure by F atoms, would lead to the reduction in SILC current [109, 108]. These strained SiO_2 regions are considered to exist locally near the Si/SiO_2 interface and extend in a scattered manner in the bulk of the oxide [113]. It is considered that these highly strained Si-O bonds are also responsible for dielectric breakdown of the gate oxide [114, 115]. At higher fluorine doses, F will break the Si-O bonds in the gate oxide and displace the oxygen in the Si-O-Si bond, creating non-bridging oxygen defects such as Si-Si bonds [110, 112], which are much more conductive and therefore more sensitive to electrical stress. This will eventually result in an increase of SILC. Lastly, the free oxygen diffuses to the interfaces and oxidizes additional silicon during the anneal at 900°C, leading to an increase of the oxide thickness.

3.5.4 Summary

We investigated the influence of fluorine on the Stress-Induced Leakage Current (SILC) characteristics in n^+ poly-Si NMOS capacitors. High levels of fluorine in the gate oxide have been found to increase the oxide thickness and increased SILC is observed. A small amount of F improves the gate oxide reliability and suppresses the generation of new oxide traps under high-field electron injection, which lead to a reduction of the SILC. However, the effect of fluorine on the SILC characteristics is minimal.

Finally, it should be noted that the effect of F will become more important with decreasing oxide thickness, since larger amount of the SiO_2 will be affected by F incorporation in thinner oxides. This will have its impact on the initial I-V and SILC characteristics of present and future MOSFETs, since many processes such as CVD W and WSi_2, and BF_2 source-drain implantation introduce fluorine near the critical gate oxide.

So far we investigated the SILC characteristics of p^+-poly gate devices experimentally. In the next section we will develop a model to examine the SILC characteristics of p^+-poly gate devices quantitatively.

3.6 Modeling of the SILC characteristics

In this section a two-step tunneling model is proposed to quantitatively describe steady-state SILC under FN, MCT and VBT injection conditions and establish an understanding for the main differences in SILC between n^+ and p^+ poly

gate MOS capacitors. One of the most important aspects in modeling SILC is to establish a representative model for SILC which is based on the appropriate physical origin of SILC without relying on parameter fitting. Only than an accurate statement can be made to explain the SILC characteristics based on calculated results.

In literature many models were developed to model the Stress-Induced Leakage Current(SILC) under FN injection conditions for n^+-poly Si gate devices [103, 92, 116, 117, 97, 118, 119], however a definitive one has not been established yet. Most of these models are based on *elastic* trap-assisted tunneling(TAT) [118], while only few of them are based on *inelastic* trap assisted tunneling(ITAT) [94, 92, 95, 119] . It has been observed by Takagi *et al.* [92, 93] that SILC is accompanied by an energy loss of approximately $\mathcal{E}_{relax}$=1.5 eV for n^+-poly Si gate devices. So the ITAT model is favored over TAT models without any energy loss. To investigate the energy loss in the SILC process of our p^+-poly gate devices, the gate and source/drain currents of p^+ poly-Si gate MOSFETs on 4.8 nm gate oxide before and after MCT stressing are depicted in Fig. 3.19. The increase in gate current (SILC) after stressing is clearly observed. However the increase in source/drain current is found to be much smaller. This indicates that electrons in the SILC conduction mechanism create fewer holes by impact ionization when they are injected in the substrate compared with electrons in the MCT conduction mechanism. This indicates that they have lower energy. Also note that after stressing an increase of source/drain current ($+I_{s/d}$) is observed which flows from the source/drain to the gate and is most likely due to trap-assisted hole tunneling (HTAT). In order to determine the quantum yield after SILC, this hole current has to be left out, so this means that the quantum yield after SILC can only be determined for $|V_{ox}|$ >3.3 V.

The quantum yield γ (corrected for HTAT) before and after MCT stressing is depicted in Fig. 3.20. The quantum yield of impact ionization is determined experimentally by means of carrier separation technique [70, 92, 93] using p-channel MOSFETs with p^+ poly-Si gates on various oxide thickness. Since injection of electrons takes place from the conduction band of the p^+ poly-Si gate under MCT injection conditions, the electron energy (relative to the conduction band edge $\mathcal{E}_c$ in the gate) is simply equal to qV_{ox}, assuming ballistic electron transport in SiO_2. From Fig. 3.20 it can be observed that the electrons in the SILC process after MCT stress lose an energy of about $\mathcal{E}_{relax}$ ≈1.0 eV. This energy loss is lower than what was previously measured on thicker oxides ($\mathcal{E}_{relax}$=1.5 eV on t_{ox}=5.6 nm) for n^+ poly-Si gate devices [92, 93]. The decrease in $\mathcal{E}_{relax}$ could be related to the decrease in gate oxide thickness. However, further experimental work is needed to validate this assumption. In the remainder of this chapter an energy

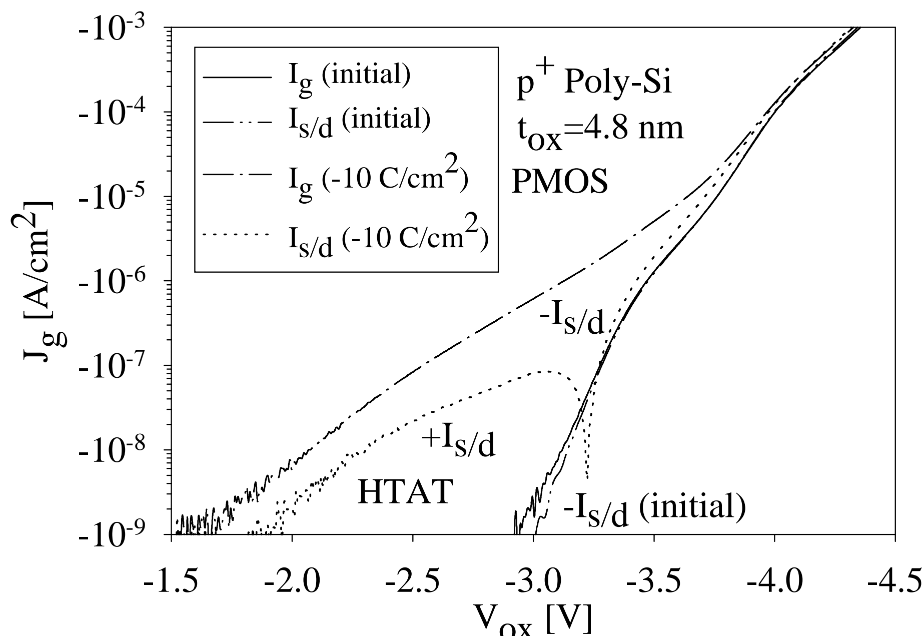

Figure 3.19: Gate and source/drain currents of p^+ poly-Si gate PMOSFET's on 4.8 nm gate oxide before and after MCT stressing.

loss of $\mathcal{E}_{relax}$=1.5 eV is therefore assumed for our p^+-poly gate devices on t_{ox}=5.6 nm gate oxide thickness.

It should however be noted that if SILC is due to *elastic* tunneling (TAT) of valence band electrons(VBT) [118] there is no real energy loss, but the electrons in the SILC process also have less energy compared to the initial characteristics. This is because if SILC is due to valence band electrons, the energy of the electrons in the SILC process is $\mathcal{E}_g$=1.12 eV lower relative to the conduction band edge $\mathcal{E}_c$ in the gate. This means that if SILC is due to TAT of valence band electrons there is no real energy loss and thus would the measured energy loss in Fig. 3.20 be apparent.

However, Takagi *et al.* [92, 93] concluded that by examining the substrate hole current of n-channel MOSFETs before and after FN stressing that valence band electron tunneling is not the dominant mechanism for SILC. This can also be concluded from our measurements, following the reasoning below.

Under $+V_g$ injection conditions, the accumulated substrate has a large density of electrons in both the valence and conduction available, which could act as SILC current. However for the $-V_g$ bias condition, the p^+-poly gate becomes the cathode. In this case, the valence band still has a large density of electrons

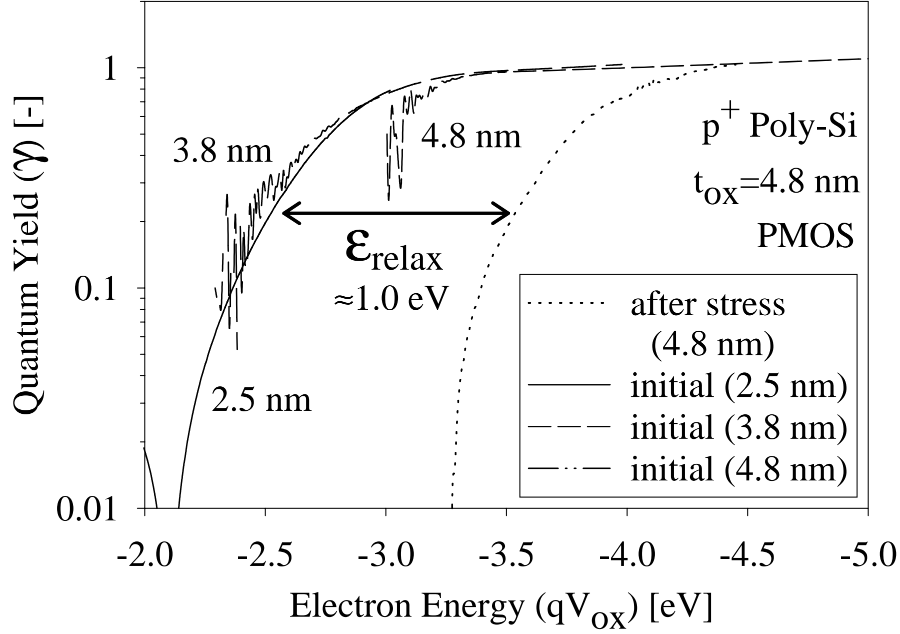

Figure 3.20: Experimental determined quantum yield γ as a function of the electron energy qV_{ox} of p^+ poly-Si gate PMOS devices for 4.8, 3.8 and 2.5 nm gate oxide thickness.

available for tunneling but the amount of electrons in the conduction band is drastically reduced. So if SILC is due to tunneling of electrons from the valence band of the cathode, then the SILC characteristics should be roughly the same for both $+V_g$ and $-V_g$ injection conditions. On the contrary, if SILC is due to conduction band electrons reduced SILC should be measured under $-V_g$ bias conditions. Comparing Fig. 3.7 with Fig. 3.9 (poly-Si) and Fig. 3.8 with Fig. 3.10 (poly-SiGe) under the same stress polarity conditions ($+J_{stress}$) it is observed that SILC is much reduced for $-V_g$. From this it can be assumed that SILC is primary due to tunneling of electrons from the conduction band of the cathode.

This indicates that SILC in our p^+ gate devices is accompanied by an energy loss $\mathcal{E}_{relax}$ for both injection conditions, and thus an energy loss mechanism *must* be included in a carrier transport model for SILC.

We therefore also propose for p^+-poly gate devices a quantitatively two-step tunneling model of the Stress-Induced Leakage Current(SILC) which is based on *inelastic* trap-assisted tunneling(ITAT) mechanism. In this model electrons tunnel *inelastically* into an intermediate trap in the oxide lose 1.5 eV of energy and then tunnel out to either the conduction band of the SiO_2 or to the anode

electrode as is schematically depicted in Fig. 3.21. Note that the increase in hole current due to HTAT after stressing is not included in this model, since the model will only be used to calculate the SILC for p^+-poly gate devices on thicker oxides (t_{ox}=5.6 nm). This means that the model will only be valid for t_{ox} >5 nm.

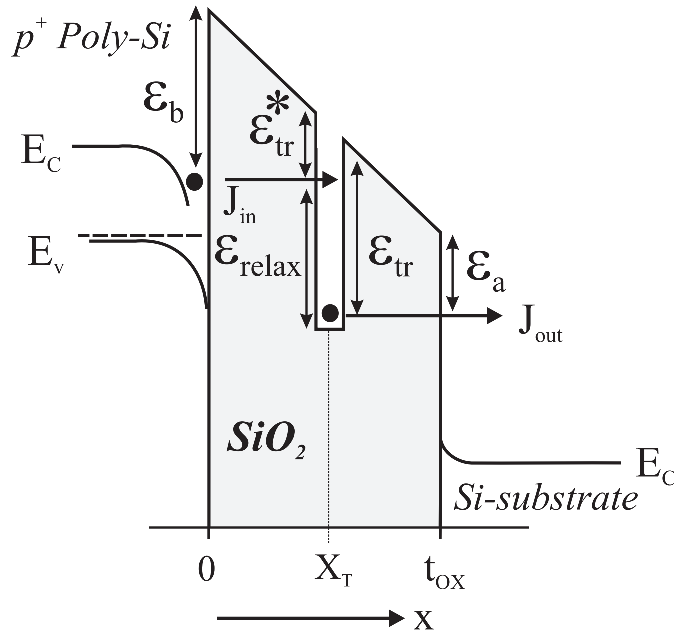

Figure 3.21: Modeling parameters used to model the Stress-Induced Leakage Current(SILC) using a simple two-step tunneling model based on *inelastic* trap assisted tunneling(ITAT) with an energy relaxation of $\mathcal{E}_{relax}$=1.5 eV.

3.6.1 A simple two-step tunneling model

Under steady-state conditions, the electron current flowing into the intermediate trap, J_{in}, and flowing out of the trap, J_{out} are balanced by each other and can be expressed as, see also Fig. 3.21 :

$$J_{in} = \sigma_{in}(1-f)D_{ot} \cdot J_{et}(\mathcal{E}_b, \mathcal{E}^*_{tr}, E_{ox}) \tag{3.7}$$
$$J_{out} = \sigma_{out} f D_{ot} \cdot J_{et}(\mathcal{E}_{tr}, \mathcal{E}_a, \mathcal{E}_f = 0, E_{ox}) \tag{3.8}$$

with :

$$J_{in} = J_{out} \tag{3.9}$$

Where J_{et} is the tunneling current density which is calculated using the Esaki-Tsu equation [75] (see Eq. 2.11), σ_{in} is the trap capture cross section, f is the occupation probability of the traps, D_{ot} is the density of the traps and σ_{out} is their emission cross section.

Note that J_{in} and J_{out} have the dimension current density per unit film thickness [A/cm^3]. Although the density of traps in the oxide most likely have an energy and space distribution, it is difficult to determine the accurate form of $D_{ot}(x,\mathcal{E})$. So at first, it is assumed that $D_{ot}(x,\mathcal{E})=D_{ot}$ is constant irrespective of the position and the energy level. Actually this is not a severe constraint and is also assumed by others [120]. Also note that for the current flowing out of the trap J_{out} the tunneling probability from a localized center to the anode should be used in a strict sense. However assuming just FN tunneling out of the trap is much more convenient due to the lack of knowledge of the physical characteristics of the traps and it has been successfully used by others [103, 92, 116, 97, 118, 119].

The transmission coefficients for tunneling into and out of the trap $T^* \cdot T_{in}$ and $T^* \cdot T_{out}$ are calculated on the basis of the Wentzel-Kramers-Brillouin(WKB) approximation, which results in :

$$T^* \cdot T_{in}(\mathcal{E}_b, \mathcal{E}^*_{tr}, E_{ox}) = \exp\left[\frac{2\sqrt{2m^*}}{3qE_{ox}\hbar}\left(\mathcal{E}_b^{\frac{3}{2}} - \mathcal{E}_{tr}^{*\frac{3}{2}}\right)\right] \tag{3.10}$$

$$T^* \cdot T_{out}(\mathcal{E}_{tr}, \mathcal{E}_a, E_{ox}) = \exp\left[\frac{2\sqrt{2m^*}}{3qE_{ox}\hbar}\left(\mathcal{E}_{tr}^{\frac{3}{2}} - \mathcal{E}_a^{\frac{3}{2}}\right)\right] \tag{3.11}$$

Where $\mathcal{E}_b$ is the barrier height at the Si/SiO_2 interface, $\mathcal{E}^*_{tr}$ being the trap energy level with respect to the conduction band of the SiO_2, $\mathcal{E}_{tr}$ the trap energy level (with energy relaxation) and $\mathcal{E}_a$ is the effective anode barrier height.

These barrier heights can be expressed as :

$$\mathcal{E}_b = 3.1\ eV \text{ (FN and MCT) or } 4.2\ eV \text{ (VBT)} \tag{3.12}$$

$$\mathcal{E}^*_{tr} = \mathcal{E}_b - qE_{ox} \cdot x \tag{3.13}$$

$$\mathcal{E}_{tr} = \mathcal{E}^*_{tr} + \mathcal{E}_{relax} \tag{3.14}$$

$$\mathcal{E}_a = \begin{cases} \mathcal{E}_b + \mathcal{E}_{relax} - qE_{ox}t_{ox} & \text{for low field, direct tunneling} \\ 0 & \text{for high field, FN tunneling} \end{cases} \tag{3.15}$$

Where x is the location of the trap and t_{ox} is the oxide film thickness.

From Eq. 3.15, it should be noted that for low oxide field strength $\mathcal{E}_a$ can become larger than 3.1 eV. This means that the trap energy level $\mathcal{E}_{tr}$ is located below the

conduction band of the anode. In this case, the captured electrons cannot tunnel out of the traps because the final state of tunneling lies within the bandgap of the anode, where there are hardly any states. So the SILC is only calculated in the range where $\mathcal{E}_a$ <3.1 eV.

Using Eq. 3.9 the *inelastic* trap-assisted tunneling current is expressed as :

$$J_{itat}(x, E_{ox}) = J_{in} = J_{out} \tag{3.16}$$

$$= \frac{\sigma_{in}\sigma_{out} \cdot J_{et}(\mathcal{E}_b, \mathcal{E}^*_{tr}, E_{ox}) \cdot J_{et}(\mathcal{E}_{tr}, \mathcal{E}_a, E_{ox})}{\sigma_{in} \cdot J_{et}(\mathcal{E}_b, \mathcal{E}^*_{tr}, E_{ox}) + \sigma_{out} \cdot J_{et}(\mathcal{E}_{tr}, \mathcal{E}_a, \mathcal{E}_a, E_{ox})} \cdot D_{ot} \tag{3.17}$$

The Stress-Induced Leakage Current J_{silc} which is the total tunneling current flowing through the SiO_2 is derived by integrating Eq. 3.16 and is described by :

$$J_{silc}(E_{ox}) = \int_0^{t_{ox}} J_{itat}(x, E_{ox}) \, \mathrm{d}x \tag{3.18}$$

Fig. 3.22 displays the spatial distribution of the trap assisted tunneling current, calculated using Eq. 3.16. From this it can be observed that the ITAT current is maximal for a given trap position x=X_T which is most efficient in producing the Stress-Induced Leakage Current. This trap which gives the largest contribution to the SILC is called *the most favorable trap position* X_T. The meaning of t_{eff} in Fig. 3.22 is the effective thickness over which the ITAT tunneling current flows mainly.

3.6.2 Model verification

Figs. 3.23 and 3.24 show the calculated SILC and initial characteristics for p^+ poly-Si at $+V_g$ and $-V_g$ after an injected charge of Q_{inj}=±1.0 C/cm^2. The physical parameters used for the calculation of the Stress-Induced Leakage Current are : m_d=0.33·m, m^*=0.35·m, $\mathcal{E}_b$=3.1(FN,MCT) or 4.2(VBT) eV, n_v=6, and σ_{in}=σ_{out}=10^{-15}cm^2. The capture cross section of the neutral traps σ has been determined by Sakakibara *et al.* [94, 95] to be 10^{-15}-10^{-16}cm^2, however they are significant only as far as orders of magnitude are concerned.

Fig. 3.23 shows the calculated SILC and initial characteristics of our p^+ poly-Si gate devices on 5.6 nm oxide at $+V_g$ after an injected charge of Q_{inj}=+1.0 C/cm^2. From Fig. 3.23 it can be observed that for p^+ poly-Si at $+V_g$ injection conditions good agreement with experimental results is obtained. The weaker

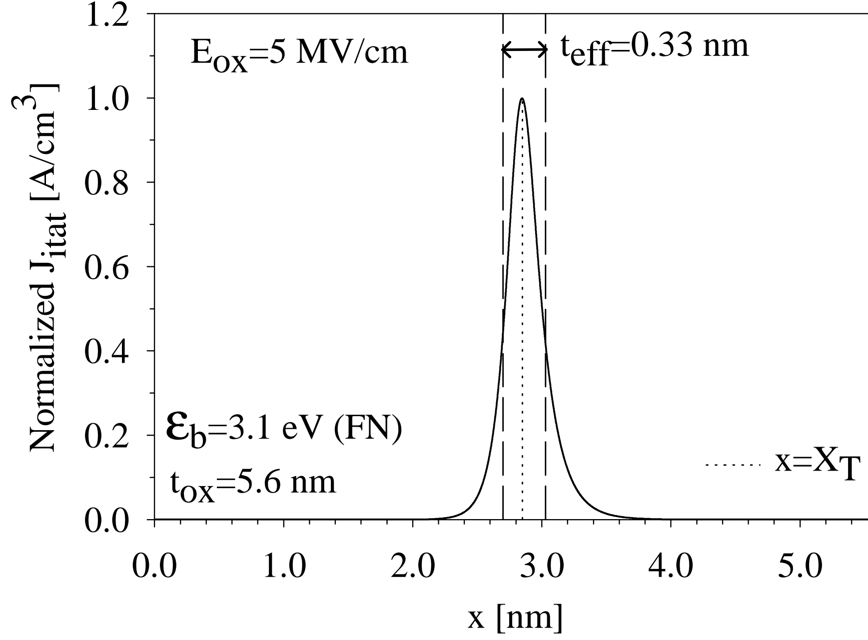

Figure 3.22: Calculated spatial distribution of the *inelastic* trap assisted tunneling current density per unit film thickness flowing through the SiO_2 layer. This current is maximal for a given trap position X_T which is most efficient in producing the SILC.

field dependence of the experimental SILC component is described very well by *inelastic* trap assisted tunneling as was also observed by others [92, 97, 119]. A good fit with experiments is obtained for a trap density of D_{ot}=9.2·10^{17}cm^{-3}.

For gate injection conditions (-V_g) the situation is much more complicated, see Fig. 3.24. For high oxide field strengths (E_{ox} >-7 MV/cm) the amount of electrons in the conduction band of the p^+ poly-Si gate is high enough to enable minority carrier trap assisted tunneling. So for high oxide field strengths the SILC is mainly dominated by minority carriers (electrons) from the conduction band of the p^+ gate. For low oxide field strengths (E_{ox} <-7 MV/cm) the SILC current at -V_g is caused by ITAT of valence band electrons, since gate depletion is reduced. Note that for this VBT current an energy relaxation of $\mathcal{E}_{relax}$=1.5 eV is also assumed (ITAT), in contrast to TAT models based on VBT were no energy loss is taken into account [118].

From Fig. 3.24 it can be noticed that including trap assisted VBT for low oxide field strengths and trap assisted MCT for high oxide field strengths a reasonable fit can be obtained with the experimentally measured SILC data. From calculations a neutral trap density of D_{ot}=5.6·10^{18}cm^{-3} is obtained for *inelastic* trap

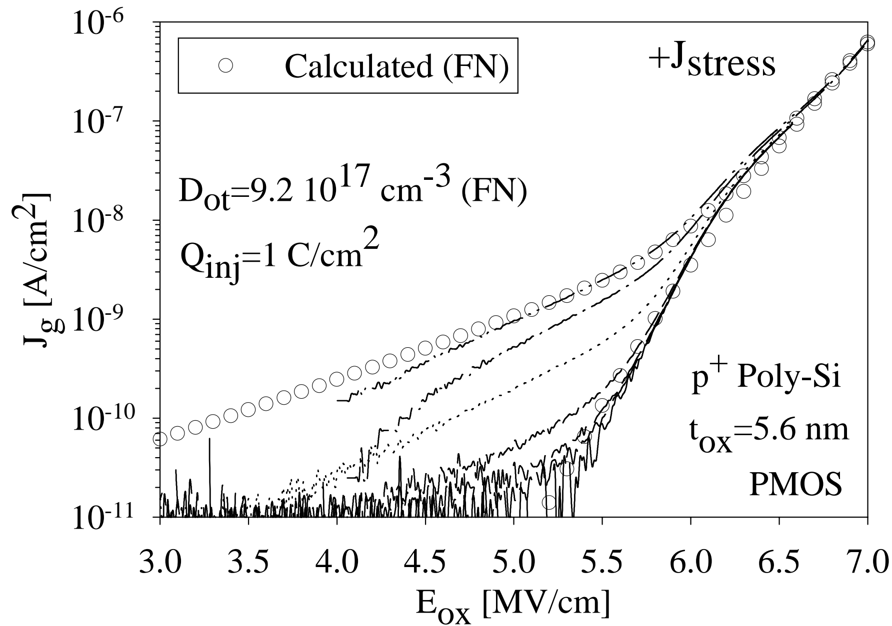

Figure 3.23: Calculated(FN) and measured J-E_{ox} curve at $+V_g$ before and after $+V_g$ stress for p^+ poly-Si gate material.

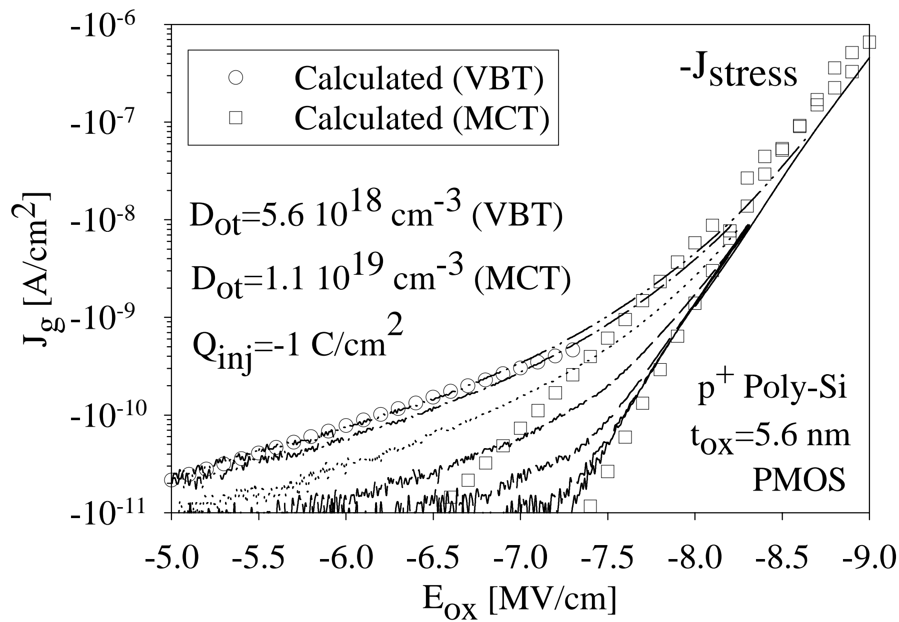

Figure 3.24: Calculated(VBT and MCT) and measured J-E_{ox} curve at -V_g before and after -V_g stress for p^+ poly-Si gate material.

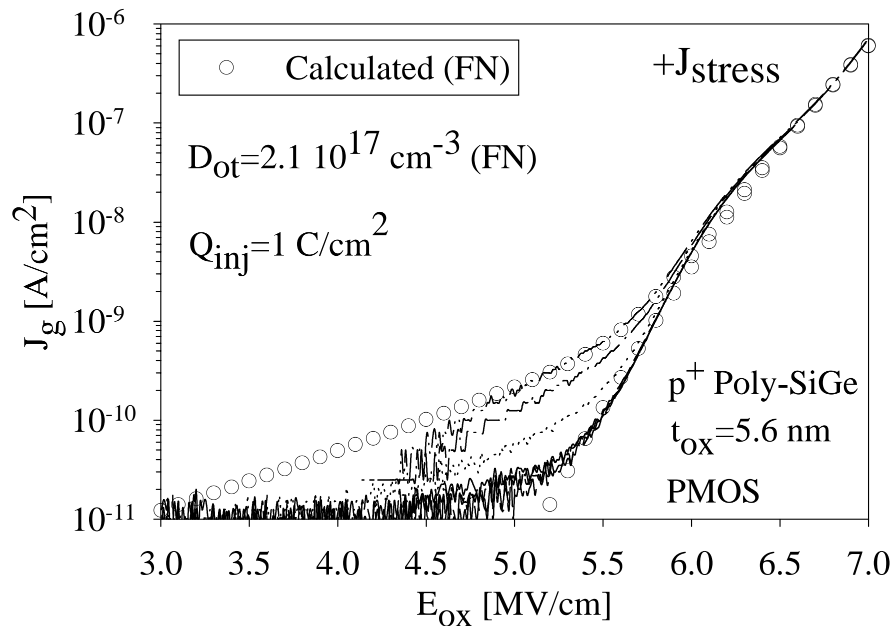

Figure 3.25: Calculated(FN) and measured J-E_{ox} curve at $+V_g$ before and after $+V_g$ stress for p^+ poly-SiGe gate material.

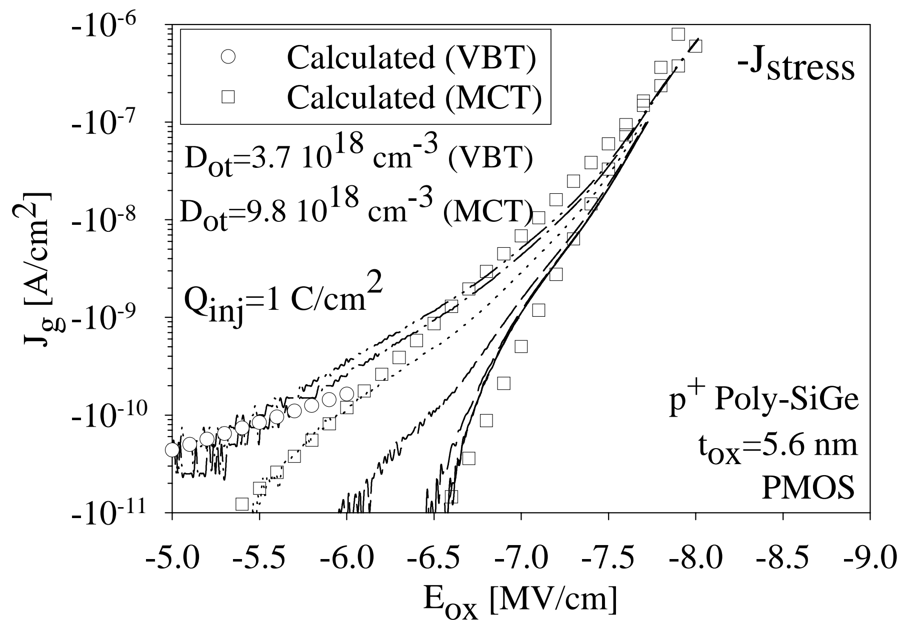

Figure 3.26: Calculated(VBT and MCT) and measured J-E_{ox} curve at -V_g before and after -V_g stress for p^+ poly-SiGe gate material.

assisted VBT electrons and D_{ot}=1.1·10^{19}cm^{-3} for *inelastic* trap assisted MCT electrons. The difference in tunneling mechanism also explains why it is not possible to derive a fixed effective barrier height from the J/E^2_{ox}-1/E_{ox} curves for -V_g injection conditions, as was already observed in section 3.4.5. The increased neutral trap density for -V_g injection conditions compared to +V_g, is in accordance with an increase of SILC found in section 3.4.3 for +V_g under opposite stress injection conditions (-V_g), however the increase of D_{ot} (6× for VBT and 12× for MCT) is not the same as obtained experimentally in section 3.4.3 (poly-Si: 10×), although it is within experimental and modeling errors.

Figs. 3.25 and 3.26 show the calculated SILC and initial characteristics of our p^+ poly-SiGe gate devices on 5.6 nm oxide at +V_g and -V_g injection conditions. The injected charge was Q_{inj}=±1.0 C/cm^2. Note that the bandgap of the gate material is changed from $\mathcal{E}_g$=1.12 eV (poly-Si) to $\mathcal{E}_g$=0.9 eV (poly-SiGe), which influences the I-V and SILC characteristics for -V_g gate bias polarity. From Figs. 3.25 and 3.26 it can be observed that a good fit with experiments is obtained for a trap density of D_{ot}=2.1·10^{17}cm^{-3} for +V_g injection conditions and D_{ot}=3.7·10^{18}cm^{-3}(VBT) and D_{ot}=9.8·10^{18}cm^{-3}(MCT) for -V_g injection conditions. The increased neutral trap density for -V_g injection conditions compared to +V_g, is in accordance with an increase of SILC found in section 3.4.3. However, the increase of D_{ot} (18× for VBT and 47× for MCT) is higher as obtained experimentally in section 3.4.3 (poly-SiGe: 13×). This difference could be related to the non-uniform distribution of traps in the oxide. Refining the model would require the inclusion of a position and energy dependent distribution of traps in the oxide $D_{ot}(x,\mathcal{E})$.

In Fig. 3.27 the most favorable trap position X_T is plotted as a function of the oxide field strength E_{ox} for p^+ poly-Si gate devices under +V_g and -V_g injection conditions. From Fig. 3.27 it can be noted that the position of X_T, remains almost constant with increasing oxide field strength E_{ox}. This is an important feature of the *inelastic* tunneling process. Since the position of the traps is determined by the balance between the tunnel current into the traps and the tunnel current out of the traps, the position of X_T becomes almost unchanged because the tunneling into and out of the traps is dominated by the direct tunneling process. This is in contrast with the *elastic* tunneling process, where FN tunneling from the trap to the cathode is dominating the SILC. Since Fowler-Nordheim tunneling(FN) has a much stronger dependence on E_{ox} compared to direct tunneling(DT), X_T moves towards the anode for elastic tunneling with increasing E_{ox} [119].

Furthermore it can be observed that the X_T is located near the center of the SiO_2 film for both FN and VBT injection conditions. However, for MCT injection conditions the most favorable trap position is shifted towards the cathode

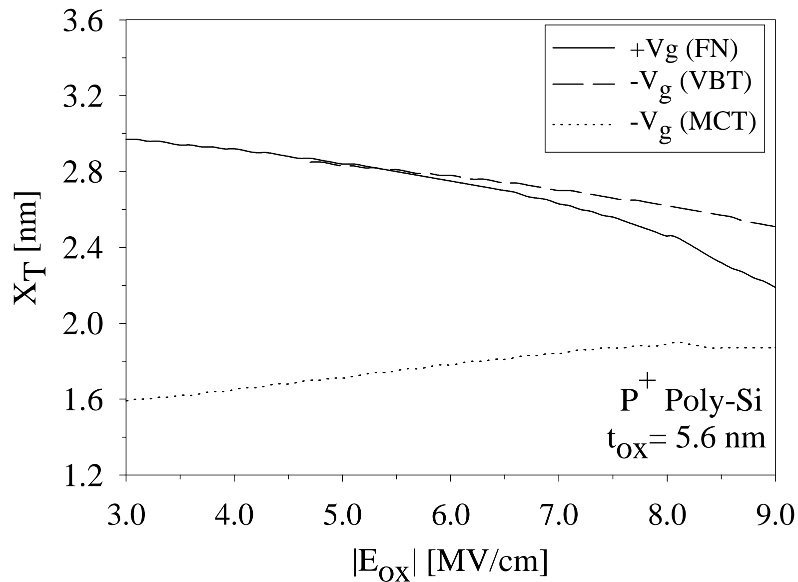

Figure 3.27: Calculated most favorable trap position X_T as a function of the oxide field strength E_{ox} for p^+ poly-Si gate devices under $+V_g$ and $-V_g$ injection conditions.

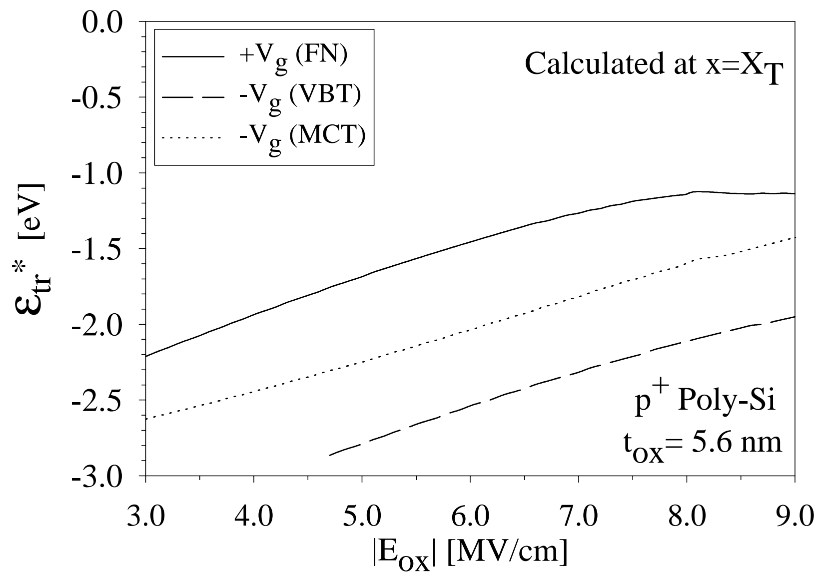

Figure 3.28: Calculated energy trap level $\mathcal{E}_{tr}^*$, with respect to the bottom of the conduction band in the SiO_2 as a function of the oxide field strength E_{ox} for p^+ poly-Si gate devices under $+V_g$ and $-V_g$ injection conditions.

interface. This can be explained by the fact that there are less electrons available for tunneling to traps compared to the FN injection condition. The position of the traps is determined by the balance between the tunnel current into the traps and the tunnel current out of the traps. Since for MCT the amount of electrons available for tunneling is less than FN tunneling, X_T will shift towards the cathode, so the probability for tunneling to traps is increased and hence compensates for the fewer electrons available for tunneling. This way the balance between the tunnel current into the traps and the tunnel current out of the traps is restored.

It should however be noted that X_T only has meaning for large area MOS capacitors. For Non-Volatile Memory(NVM) cells, which have small areas the situation is completely different. For small area cells the actual distribution of traps $D_{ot}(x,\mathcal{E})$ has a large influence on the SILC characteristics.

Fig. 3.28 displays the calculated energy trap level $\mathcal{E}_{tr}^{*}$, measured from the conduction band of the SiO_2. From the model it is estimated that the traps have an energy level of 1.3 - 2.2 eV (FN), 1.4 - 2.6 eV (MCT) and 2.0 - 2.8 eV (VBT) below the conduction band edge of the SiO_2.

3.7 Conclusions

In this chapter the Stress-Induced Leakage Current(SILC) of MOS capacitors with n^+ and p^+ poly-Si and poly-$Si_{0.7}Ge_{0.3}$ gates has been studied. For n^+-poly gate devices, symmetric SILC with respect to gate bias polarity was observed. For p^+-poly gate devices, asymmetric SILC (gate bias polarity) and reduced SILC for p^+ poly-$Si_{0.7}Ge_{0.3}$ was observed. For p^+ gate devices it was found experimentally and evaluated theoretically using a two-step tunneling model based on ITAT, that the amount of neutral traps generated per unit of injected charge is approximately one order of magnitude higher for -V_g injection conditions compared to +V_g injection of stress. This increase of SILC for -V_g stress is most likely due to the higher oxide field at -V_g during stress using the same stress current(CCS). The reduced SILC observed in p^+-poly gate devices could be attractive for non-volatile memory devices. Boron-doped poly-SiGe may be a very interesting gate material due to low SILC at +V_g and better gate oxide quality. For very thin oxides (t_{ox} <4 nm) the SILC current at low -V_g voltages is dominated by holes tunneling from the hole inversion layer in the substrate to the gate. This increase in hole current after stress is important for very thin gate oxide reliability. The effect of fluorine(F) on the SILC characteristics of n^+ poly-Si gate devices has also been studied. Results indicate that an optimum value for the implanted fluorine dose exists. A small amount of F leads to reduced SILC, while higher levels of F result in enhanced SILC. Furthermore it was observed that the oxide thickness increases with increasing F incorporation.

Chapter 4

Gate oxide breakdown of n$^+$ and p$^+$ poly-Si gate devices

In this chapter results are presented of the time-to-breakdown (t_{bd}) of both n$^+$ and p$^+$ poly-Si gate devices on ultra-thin gate oxides (t_{ox} <5 nm). For the 2.5 nm oxides (n$^+$ poly-Si gate) a decrease in t_{bd} of nearly 4 orders of magnitude is observed when the ambient temperature is increased from 25°C to 200°C. Also a weak gate bias polarity dependence is observed with respect to time-to-breakdown if t_{bd} is plotted as a function of the gate voltage V_g. For p$^+$-poly Si gate devices an increase of t_{bd} with increasing gate anneal RTA temperature, i.e. increasing active gate doping, is observed, which is most likely related to a decrease in tunneling current during stress at a fixed gate voltage. This indicates that both the total energy release at the anode and the electron fluence are important parameters for t_{bd} of ultra-thin oxides. It appears that constant voltage stress (CVS) is also preferable for p$^+$-poly gate devices on sub-5 nm gate oxides.

4.1 Introduction

The reliability of ultra-thin gate dielectrics (t_{ox} <5 nm) is of increasing concern because of the significant direct tunneling currents flowing during normal device operation. Further downscaling of the gate oxide thickness is not only limited by Stress-Induced Leakage Current(SILC) as was already observed in chapter 3, but soft-breakdown(SB) and the increase of temperature acceleration of time-to-breakdown(t_{bd}) [7, 48, 49] also are a major concern for further down-scaling of the gate oxide thickness. Gate oxide reliability has been studied mainly for n$^+$-doped poly-Si gate devices. In this chapter the reliability (time-to-breakdown) of both n$^+$ and p$^+$ gate devices on ultra-thin oxides is studied.

First in section 4.2 the experimental procedures for the fabrication of the ultra-thin gate oxides with n$^+$ poly-Si and p$^+$ poly-Si gate MOS capacitors are described. After this the temperature acceleration of the time-to-breakdown of

n^+-poly Si gate devices on 3.9 nm and 2.5 nm oxides is studied as a function of the gate voltage for temperatures between room temperature and 200°C in section 4.3. In section 4.4 the t_{bd} measurements of p^+ poly-Si gate devices on 4.8 nm oxide thickness are studied as a function of the gate voltage for different gate RTA anneal temperatures, i.e. different active gate doping.

4.2 Experimental Procedures

The samples prepared for gate oxide breakdown study consists of gated-diodes and can essentially be split up in two sets. The first set consists of n^+ poly-Si NMOS capacitors with 3.9 and 2.5 nm gate oxide thickness and are used to study the temperature acceleration of time-to-breakdown (t_{bd}).

The seconds set consists of p^+-poly Si gate PMOS capacitors with 4.8 nm oxide thickness and various gate anneal RTA temperatures. These samples are used to investigate the effect of RTA anneal temperature on the t_{bd} characteristics of p^+ gate devices. The gate RTA anneal temperature was varied between 990°C and 1070°C for 20 seconds.

- **Set 1**
  The n^+ poly-Si NMOS capacitors were fabricated on 15-25 Ω-cm p-type silicon substrates. Well implants were done by 140 keV, $5.0{\cdot}10^{12}$ cm^{-2} using B^+ followed by a 90 keV, $7.0{\cdot}10^{12}$ cm^{-2} anti-punch through implant with B^+ and a 16 keV, $2.7{\cdot}10^{12}$ cm^{-2} V_t implant with B^+. A high quality gate oxide with 2.5 and 3.9 nm thickness (ellipsometric) was grown in N_2 diluted dry oxygen at 800°C(3.9 nm) and at 650°C(2.5 nm) in wet oxygen. Undoped poly-Si(150 nm thick) was deposited amorphously and implanted with $3.0{\cdot}10^{14}$ cm^{-2} As^+ at 15 keV. Pocket implant was done at 15 keV with $5.0{\cdot}10^{12}$ cm^{-2} B^+. Source/drain implantation was done with $4.0{\cdot}10^{15}$ cm^{-2} As^+ at 40 keV. The final activation anneal is done by a Rapid Thermal Anneal (RTA) at 1030°C for 20 seconds.

- **Set 2**
  p^+ poly-Si PMOS capacitors were fabricated with 4.8 nm oxide thickness and various RTA anneals using the same process conditions as in section 2.2 on page 17.

4.3 Oxide breakdown of n$^+$-poly Si gate devices

In this section the time-to-breakdown of n$^+$-poly Si gate devices on 3.9 nm and 2.5 nm oxides is studied as a function of the gate voltage for temperatures between room temperature and 200°C. Fig 4.1 shows the J_g-V_g characteristics for the n$^+$-poly Si gate devices on 3.9 nm and 2.5 nm oxides for various temperatures. From Fig 4.1 it is evident that the temperature dependence of the J_g-V_g characteristics is weak, since tunneling is not very dependent on temperature. The temperature dependence observed at low -V_g for t_{ox}=2.5 nm is explained as follows. The n$^+$-poly Si gate devices on 2.5 nm oxides have a flatband voltage of V_{fb}=-0.95 V at T=25°C and the threshold voltage is close to V_t=0 V. So for +V_g the substrate is already inverted. However for -V_g < -0.95 V the built-in field between the n$^+$ poly-Si gate and the p-substrate is opposite to V_g. Since V_{fb} decreases with increasing temperature, E_{ox} increases with increasing temperature at the same -V_g. So with increasing temperature the tunneling current density increases due to the increase of E_{ox} and an increased temperature dependence is observed. Note that this temperature dependence will be reduced if the I-V characteristics are plotted as a function of E_{ox}. Furthermore, it can be noted that the curves are not symmetric with respect to the gate voltage due to band-bending in the substrate (V_{fb} ≈-0.95 V(25°C)), as was already mentioned in chapter 2.

Next, the t_{bd} of the n$^+$ poly-Si gate devices is studied as a function of the gate voltage for temperatures between room temperature and 200°C. All measurements were performed on n$^+$ poly-Si NMOS capacitors with a gate area of A=300 × 300 μm^2 under constant voltage stress (CVS) injection conditions as will be explained below.

4.3.1 Constant gate voltage stress(CVS)

In the previous chapter stressing took place under constant current stress (CCS) conditions for gate devices on 5.6 nm oxide thickness. CCS was chosen, since during tunneling the current density is uniquely related to the oxide field strength. So CCS automatically implies stressing at a constant oxide field strength. Moreover it was observed in chapter 3 that both the electron flux (J_{stress}) and the total energy released at the anode (∼E_{ox}) are important parameters for the oxide degradation process.

However with decreasing oxide thickness, we enter the region where electron transport through the oxide becomes ballistic (i.e. no energy loss) for t_{ox} < 5 nm. For this oxide thickness region it has been observed in literature that

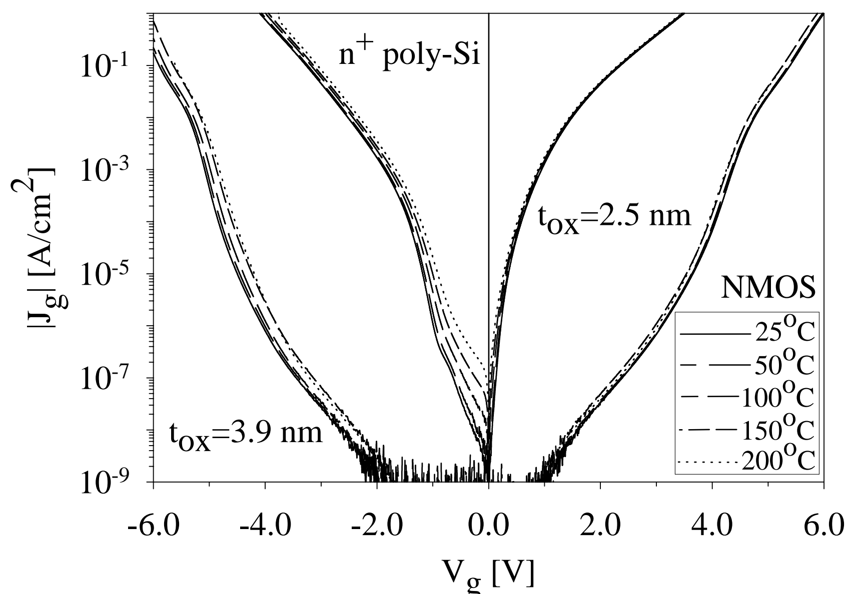

Figure 4.1: I-V measurements of n^+ poly-Si gate NMOS capacitors with 3.9 nm and 2.5 nm oxide thickness. The temperature was varied from 25°C to 200°C.

the charge-to-breakdown Q_{bd} becomes a strong function of stress polarity, gate doping and so on [121]. The polarity dependence of Q_{bd} for constant current stressed thin oxides has been investigated much and in general this observation has been related to the structural 'extrinsic' differences in the two interfacial regions (poly-Si/SiO_2 versus mono-Si/SiO_2 interface). However recently it was shown by DiMaria *et al.* [122] that this so called polarity gap becomes smaller if the Q_{bd} is related to the applied gate voltage V_g instead of the oxide field strength E_{ox}.

It has been suggested by DiMaria *et al.* [122] that to get near universal behaviour (no asymmetry) of t_{bd}, the data should be plotted as a function of the maximum electron energy with respect to the Fermi level position at the anode/oxide interface, which is approximately equal to $q|V_g|$. Since for sub-5 nm oxides the electrons travel ballistically through the oxide and therefore loose no energy, the gate voltage approximately determines the injected electron energy with respect to the Fermi level position at the anode/oxide interface rather than the electric field strength, as was the determining factor for thicker oxides. It was also observed by DiMaria *et al.* [122] that the probability of defect generation depends on the Fermi-level position at the anode/oxide interface. So for ultra-thin oxides (t_{ox} <5 nm) it was proposed that the gate voltage rather than the oxide field determines the breakdown of the gate oxide [123].

Furthermore, Nigam *et al.* [124] have proposed that CVS is more practical since in contrast to CCS, CVS is assumed to be process independent. They concluded that for ultra-thin oxides the t_{bd} should therefore always be plotted and extrapolated as a function of V_g instead of E_{ox}. Indeed for sub-5 nm gate oxides the polarity gap disappears if t_{bd} is plotted as a function of V_g [49]. So it is suggested that for sub-5 nm gate oxides CVS is preferred over CCS. This will be examined in more detail in the next section.

4.3.2 Time-to-breakdown of n^+ poly-Si gate devices

Figs. 4.2 and 4.3 display the t_{bd} of n^+ poly-Si gate devices on 3.9 nm and 2.5 nm oxides as a function of V_g for temperatures between room temperature and 200°C. In this chapter time-to-breakdown corresponds to the first recorded breakdown phenomenon (soft- or hard-breakdown).

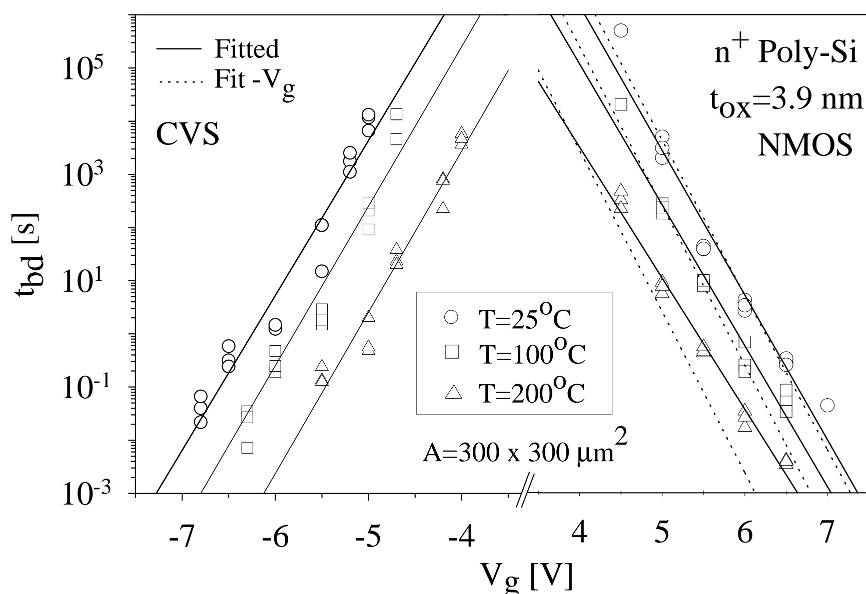

Figure 4.2: Time-to-breakdown (t_{bd}) measurements of n^+ poly-Si NMOS gate devices on 3.9 nm oxide thickness under different CVS injection conditions. The temperature was varied from 25°C to 200°C. Dotted lines are measured data at -V_g injection conditions.

From these Figs. it is immediately clear that the time-to-breakdown decreases significantly with increasing ambient temperature. For the 2.5 nm gate oxide thickness a decrease in t_{bd} of nearly 4 orders of magnitude is observed when the temperature is increased from 25°C to 200°C. This will have a large impact on the reliability of ultra-thin oxides at operation conditions, especially

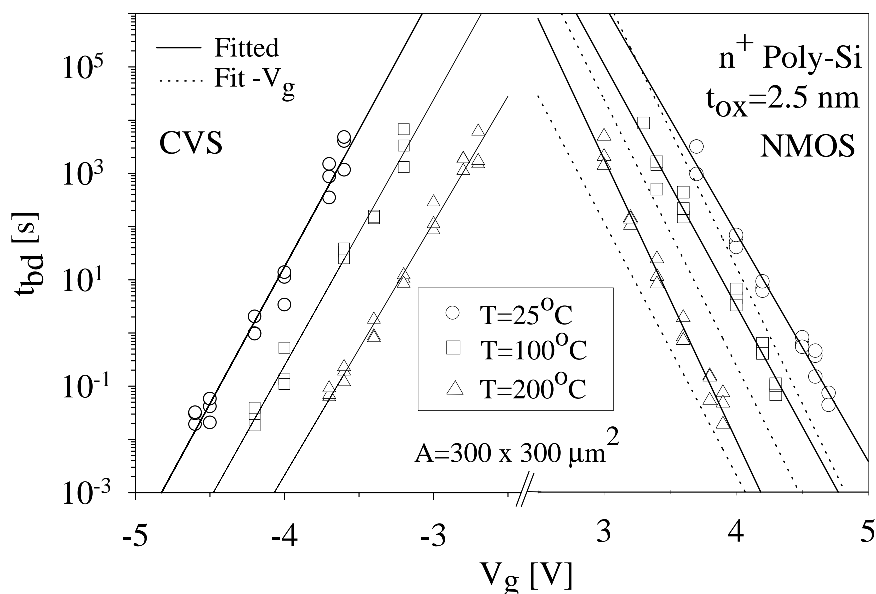

Figure 4.3: Time-to-breakdown (t_{bd}) measurements of n^+ poly-Si NMOS gate devices on 2.5 nm oxide thickness under different CVS injection conditions. The temperature was varied from 25°C to 200°C. Dotted lines are measured data at -V_g injection conditions.

since applications often require reliable operation of devices at elevated temperatures, sometimes even up to T=150 - 200 °C. This temperature acceleration of t_{bd} becomes more profound with decreasing oxide thickness, as can be seen by comparing Fig. 4.2 with Fig. 4.3. The temperature acceleration of t_{bd} could be related to the temperature dependence of the J-E_{ox} characteristics. Tunneling itself is a temperature independent process, but the number of electrons available for tunneling depends on the temperature. Also the flatband voltage V_{fb} is temperature dependent. The conversion from gate voltage to E_{ox} using Eq. 2.4 will thus result in a higher gate current with increasing temperatures at a fixed oxide field strength. However it was observed that this temperature dependence of the gate current at a fixed oxide field strength is negligible compared to the temperature acceleration of t_{bd} and thus *can not* explain the temperature dependence of t_{bd}. The other most likely explanation of the temperature dependence of t_{bd} is the enhancement of the defect generation rate P_g with increasing temperature. This enhancement of defect generation rate in thinner gate oxides is indeed found by others [48]. This means that with increasing temperature more traps are created per amount of injected charge, i.e. $P_g(T)$ (see also Eq. 3.6).

Next, the stress polarity dependence of t_{bd} is investigated. The dotted lines in

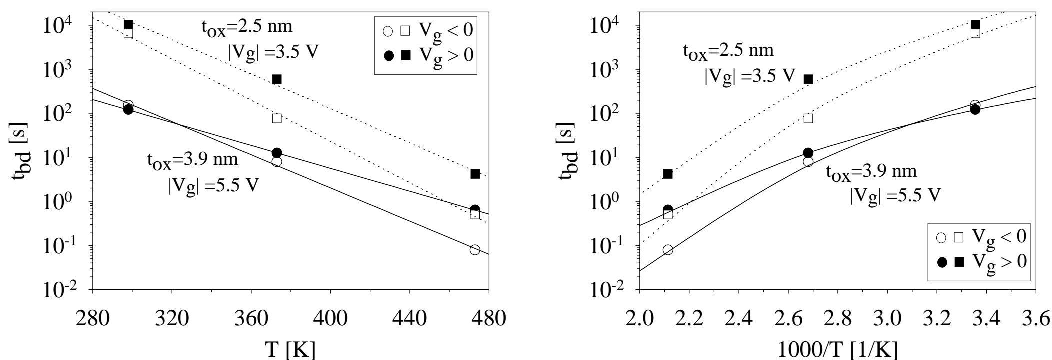

Figure 4.4: Temperature dependence of t_{bd} for two different oxide thicknesses (2.5 nm and 3.9 nm). A linear relation between t_{bd} and T is obtained, indicating that the temperature acceleration of t_{bd} is non-Arrhenius and therefore no activation energy can be determined.

Figs. 4.2 and 4.3 are measured data at -V_g injection conditions plotted for +V_g. Comparing the dotted lines with measurements done at +V_g injection conditions it can be observed that t_{bd} is almost independent of stress polarity, if plotted as a function of V_g. This agrees with results found by others. [122, 124, 49]. The slight difference in slope between +V_g and -V_g stress polarity could be related to the limited data available or due to minor structural differences in the two interfacial regions. For gate injection conditions (-V_g) the t_{bd} might be slightly lower due to non-uniform injection conditions (doping level varies over grain) enhancing the local creation of traps.

This is an important result, since from these measurements it might be concluded that V_g and t_{bd} have a unique relationship for sub-5 nm oxides. However, it should be noted that from Fig. 4.1 it is evident that stressing under CVS takes place at a much larger current density for +V_g injection conditions compared to -V_g bias polarity. The current density under CVS is more than one order of magnitude higher for +V_g compared to -V_g injection conditions. This means that, while t_{bd} is the same for both bias polarities, Q_{bd} (see Eq. 1.1) is higher for -V_g bias polarity. The difference in J_{stress} for -V_g and +V_g bias polarity is remarkable, since in chapter 3 for 5.6 nm gate oxides it was concluded that both the electron flux and the total energy released at the anode are important parameters in the degradation process. From the results above it can thus be concluded that for sub-5 nm oxides knowing both the electron flux (J_{stress}) and the total energy released at the anode is *no longer* sufficient to predict the oxide degradation process. This means that for sub-5 nm oxides both the electron energy and electron flux do not determine the oxide degradation process uniquely. It has been suggested by Bude *et al.* [125] that this could be explained by taking

into account the energy distribution of the generated holes in the anode. They developed a *anode* Fermi-level dependent AHI model which is successful in explaining above found observations.

Fig. 4.4 shows the t_{bd} plotted as a function of T and 1/T. From this it can be observed that for a fixed gate stress voltage a straight line is observed if t_{bd} plotted as a function of T. Plotting t_{bd} versus 1/T, curved lines are obtained indicating that the temperature acceleration of t_{bd} is non-Arrhenius and therefore no activation energy $\mathcal{E}_{act}$ can be determined. These results agree with results found by others [48, 49].

4.4 Oxide breakdown of p^+ poly-Si gate devices

In this section the t_{bd} measurements of p^+ poly-Si gate devices on 4.8 nm oxide thickness are studied for different gate RTA anneal temperatures. The gate RTA anneal temperature was chosen to vary from 990°C, 1010°C to 1070°C for 20 seconds. Stressing took place under CVS injection conditions of V_g=-6.5 V using A=50 × 50 μm^2 p^+ poly-Si PMOS capacitors. All measurements were done at room temperature.

It has been observed by Nigam *et al.* [124] that the t_{bd}-distribution of n^+ poly-Si gate devices is independent of active gate doping. Stressing under CVS conditions for different active gate doping (different gate RTA anneal temperatures) should therefore result in the same t_{bd}-distribution. Fig. 4.5 displays the t_{bd} measurements of p^+ poly-Si gate devices on 4.8 nm gate oxide thickness. From Fig. 4.5 it can be observed that for p^+ poly-Si gate devices the situation is different. An increase of t_{bd} with increasing gate RTA anneal temperature is observed.

This indicates that for our p^+ poly-Si gate devices no unique relation between t_{bd} and V_g is found. So it seems that for CVS the t_{bd} distribution depends not only on the Fermi-level position at the anode/oxide interface, but is also dependent on the Fermi-level of the cathode/oxide interface. Note that the increase of t_{bd} with increasing gate anneal temperature *can not* be explained by an increase of boron-penetration in the gate oxide. It is believed that an increase in gate anneal temperature can give significant boron incorporation in the gate oxide [54, 126]. This would lead to an enhancement of traps in the gate oxide, which would reduce the t_{bd} with increasing gate anneal temperature [126]. However, the opposite is observed. The increase of t_{bd} with increasing RTA anneal temperature as observed in our p^+ poly-Si gate devices is most likely related to a decrease in tunneling current during stress at a fixed gate voltage V_g=-6.5 V. For a gate RTA

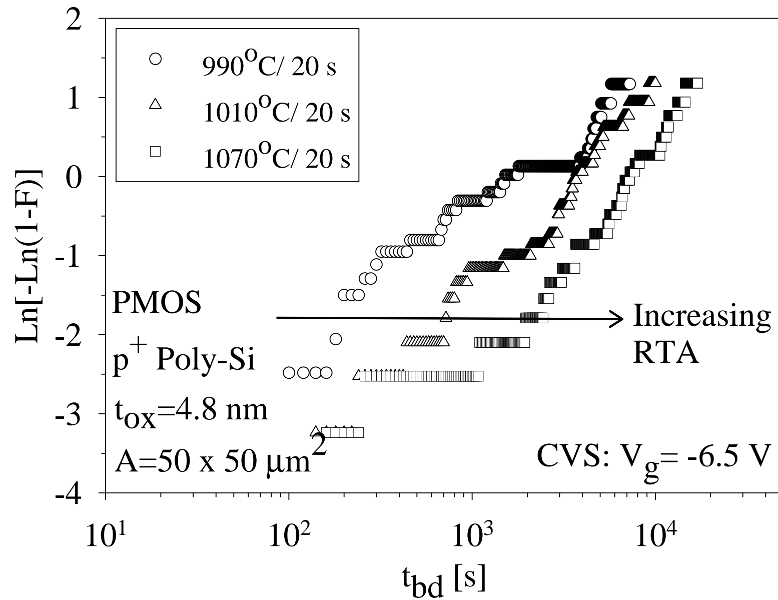

Figure 4.5: Time-to-breakdown (t_{bd}) distribution of p$^+$ poly-Si gate PMOS devices and 4.8 nm oxide thickness under CVS injection conditions of V_g=-6.5 V. The gate RTA anneal temperature was chosen to be 990°C, 1010°C and 1070°C for 20 seconds.

anneal temperature of 990°C, the gate current density is J_g=-4.4 mA/cm^2 for 1010°C the current density is J_g=-2.88 mA/cm^2 and for the RTA temperature of 1070°C the current density is J_g=-0.88 mA/cm^2 at a fixed gate voltage of V_g=-6.5 V.

This shows that not only the total energy release at the anode, but also the electron fluence is an important parameter for the t_{bd} of ultra-thin oxides. Moreover, if CVS and t_{bd} are used for gate oxide reliability comparison, it can be assumed that nMOSFETs are more vulnerable to oxide breakdown than pMOSFETs for -V_g under normal operation conditions [127]. This is related to the lower tunneling current flowing through the pMOSFET compared to the nMOSFET using the same voltage stress conditions (CVS), which is basically the same as the increase in t_{bd} with increasing active gate doping for our p$^+$ gate devices (see Fig. 4.5). So this means that pMOSFETs can last longer with a higher t_{bd} than the nMOSFETs.

From the results obtained in this chapter it can thus be concluded that both the total energy release at the anode (~V_g) and the electron fluence, as well as the ambient temperature are important parameters for the t_{bd} of ultra-thin oxides. For our p$^+$ poly-Si gate devices, the highest t_{bd} is obtained for the largest thermal budget. Although t_{bd} depends on active gate doping in our p$^+$ poly-Si

gate devices under CVS at -V_g injection conditions, it appears that constant voltage stress (CVS) is also preferable for p^+ poly-Si gate devices on sub-5 nm gate oxides.

4.5 Conclusions

In this chapter the time-to-breakdown (t_{bd}) of both n^+ and p^+ poly-Si gate devices on ultra-thin gate oxides (t_{ox} <5nm) was studied. For the n^+ poly-Si gates a decrease in t_{bd} of nearly 4 orders of magnitude is observed (t_{ox}=2.5 nm) when the ambient temperature is increased from 25°C to 200°C. This will have a large impact on the reliability of ultra-thin oxides at operation conditions, especially since applications often require reliable operation of devices at elevated temperatures. For p^+ poly-Si gate devices an increase of t_{bd} with increasing gate anneal RTA temperature is observed. This is most likely related to a decrease in tunneling current during stress at a fixed gate voltage. This indicates that both the total energy release at the anode and the electron fluence are important parameters for t_{bd} of ultra-thin oxides.

Chapter 5

I-V characteristics of n$^+$ poly-Si gate devices after breakdown

In this chapter results are presented of the post-breakdown electrical characteristics of n$^+$ poly-Si MOS capacitors with 8 nm and 10 nm thick oxides. The dependence of the post breakdown I-V characteristics on capacitor area, substrate doping and breakdown power were evaluated. Depending on gate and substrate doping polarity, different post breakdown characteristics were observed. For n$^+$-poly/oxide/n$^+$-substrate MOS capacitors the post breakdown characteristics resemble that of a resistance. The value of the resistance is determined by the filament cross-section formed through the emission of energy stored in the MOS capacitor before breakdown. For n$^+$-poly/oxide/p-substrate MOS capacitors the I-V characteristics after high power breakdown resemble that of a nanometer size diode with a high I_{on}/I_{off} ratio. The breakdown voltage of these diodes is high due to the gate action. For low power breakdown the diodes become "non-ideal" and their "non-ideality" depends strongly on stress current. The conduction mechanism after low power breakdown is still not well understood. The I-V characteristics of these devices were also measured at variable temperature to study the dominant conduction processes after breakdown. At very low power dissipation soft-breakdown may occur. This shows that soft-breakdown does not only occur in sub-5 nm oxides, but can also be enforced in 8 nm gate oxide thickness structures if the total energy during breakdown is limited.

5.1 Introduction

It has been reported that the breakdown of ultra-thin oxides (t_{ox} <4 nm) is difficult to detect [36] because the post breakdown I-V characteristics are not significantly different from the initial I-V characteristics. The conduction mechanism after breakdown is therefore an important issue. This is even more important when the power dissipation during breakdown is limited as happens for instance for thin oxides and small area MOS capacitors in circuits. Under these

circumstances soft-breakdown (SB) may occur [33], i.e. breakdown becomes a less well-defined phenomenon and the question whether this corresponds to real oxide failure is still to be resolved [36].
However, still little is known about the final breakdown mechanism and about the I-V characteristics after breakdown. In this chapter it will be shown that the barrier between soft-breakdown and hard-breakdown is not described by device parameters [34] but is entirely characterized by the energy threshold of catastrophic current runaway. It is suggested that dielectric (hard)breakdown of SiO_2 is caused by a local catastrophic runaway phenomenon. The I-V characteristics after breakdown are determined by the filament cross-section formed through the dissipation of energy stored in the MOS capacitor before breakdown. This is investigated by studying the post breakdown I-V characteristics of carefully designed n^+ poly-Si gate MOS capacitors with 8-10 nm oxide thickness. The stress current and capacitor area were varied to study the dependence of electrical power on the post breakdown I-V characteristics. A gate oxide thickness of 8-10 nm was chosen to reduce parasitic direct tunneling(DT) current flowing parallel with that of the damaged oxide area.

First in section 5.2 the experimental procedures for the fabrication of the n^+ poly-Si gate MOS capacitors with 8-10 nm oxide thickness are presented. In section 5.3 the measurement set-up for low power breakdown of the gate oxide is described. Next, in section 5.4 the post breakdown I-V characteristics of n^+ poly Si/oxide/n^+-substrate MOS capacitors are studied. The post breakdown characteristics resemble that of a resistance, its value is determined by the filament cross-section formed through the emission of energy stored in the MOS capacitor before breakdown. To further investigate this, an electro-thermal model is developed in section 5.5 which allows us to derive some physical characteristics of the filament cross-section formed after breakdown. Further, in section 5.6 the post breakdown I-V characteristics of n^+ poly-Si/oxide/p-substrate MOS capacitors is investigated. After breakdown the I-V characteristics resemble that of a nanometer size diode, its ideality factor depends strongly on stress current and power dissipation during breakdown. The I-V characteristics of these diodes were measured in forward ($-V_g$) and reverse ($+V_g$) direction and at variable temperatures to study the dominant conduction processes after breakdown. Finally in section 5.9 an application for these diodes formed after breakdown is described. Since nano-scale diodes can be formed easily they can be used in One Time Programmable(OTP) memories called Diode Programmable Read Only Memories(DPROMs).

5.2 Experimental Procedures

The samples prepared for this study can essentially be split up in two sets. The first set consists of n^+ poly-Si MOS capacitors with 10 nm oxide thickness on n^+-substrates and are used to study the influence of capacitor area and electrical power on the post breakdown I-V characteristics. These structures are chosen, since after breakdown a resistance is formed connecting the gate and substrate, which value can be evaluated relatively easy as a function of breakdown power.

The second set consists of n^+ poly-Si NMOS capacitors with 8 nm gate oxide thickness. The post-breakdown I-V characteristics resemble that of a diode, due to the opposite doping polarity of gate and substrate.

- **Set 1**
  The n^+ poly-Si MOS capacitors were fabricated on 2-5 Ω-cm n-type silicon substrates. First the resistance of the substrate surface was decreased by implantation of P^+ at 100 keV, $5.0 \cdot 10^{15}$ cm^{-2}, followed by a furnace anneal at 800°C for 30 minutes to remove the lattice damage. A 100 nm thick field oxide was used for isolation. Next a high quality gate oxide with 10 nm thickness (ellipsometric) was grown in diluted dry oxygen at 900°C. Undoped poly-Si layers (300 nm thick) were deposited using a LPCVD system. Gate doping was done by a 100 keV, $6.0 \cdot 10^{15}$ cm^{-2} As^+ implant followed by a furnace anneal at 900°C for 30 minutes.

- **Set 2**
  The n^+ poly-Si NMOS capacitors consisted of a 10^{16} cm^{-3} p-type doped substrate. A 700 nm thick LOCOS was used for isolation and a high quality gate oxide with 8 nm thickness (ellipsometric) was grown in diluted dry oxygen. Undoped poly-Si layers (300 nm thick) were deposited using a LPCVD system. Gate doping was done by a 80 keV, $1.0 \cdot 10^{16}$ cm^{-2} As^+ implant followed by a furnace anneal at 900°C for 30 minutes.

5.3 Breakdown of the gate oxide

Breakdown of the gate oxide is achieved using constant current stress CCS conditions, by forcing a limited stress current I_s through the MOS capacitor. Hereby inducing Fowler-Nordheim tunneling until breakdown occurs, see Fig. 5.1. CCS was employed to minimize additional thermal effects, since the stress voltage is

automatically decreased immediately if breakdown occurs to keep the current constant. This is opposite to constant voltage stress CVS, were during and after breakdown the voltage is kept constant. This leads to additional stress, making the breakdown not well defined. Furthermore it should be noted that the total energy stored on the MOS capacitor and the parasitic capacitances of the measurement set-up are released through the breakdown path during discharging, assuming that the on-chip series resistance of the MOS structure can be neglected. The parasitic capacitances of the cables of the measurement set-up are in the order of 100 pF/m, which is much larger than the capacitance of the MOS capacitor (typical <1 pF). So discharging of the capacitors at breakdown will be determined entirely by the set-up and is not controllable if the discharging of the parasitic capacitances is not minimized.

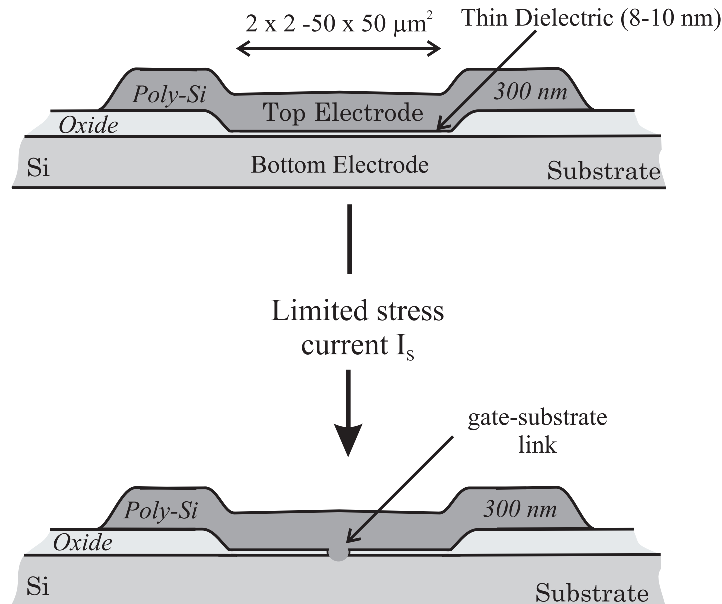

Figure 5.1: Cross section of the MOS structure. Stressing of the devices is done by forcing a limited stress-current -I_s through the capacitor until breakdown occurs, resulting in the formation of a gate-substrate link.

Controlled (low power) breakdown is ensured by placing a $R_{probe-tip}$=1 MΩ series resistance close to the probe tip to limit the discharge of parasitic capacitances in the wafer measurement set-up. After breakdown of the gate oxide the 1 MΩ resistance was removed, so the post breakdown characteristics could be measured. Moreover, carefully designed structures with on-chip series resistors ($R_{on-chip}$ ≈1 MΩ) are also used to minimize the discharging of the parasitic capacitances during breakdown. These are necessary conditions to ensure low power breakdown, especially in thicker oxides.

5.4 I-V characteristics after breakdown Part I: linear characteristics

In this section the post breakdown characteristics of the n^+ poly-Si/SiO_2/n^+-substrate structures are studied. The post breakdown I-V characteristics are presented in Fig. 5.2. The stress current was fixed at I_s=-1 μA. After breakdown, multiple I-V characteristics were measured with increasing current compliance I_c. Fig. 5.3 displays the post breakdown resistance R_{bd}=V/I, re-plotted as a function of the current. It can be noted that for low currents the post breakdown I-V characteristics of the n^+ poly-Si/SiO_2/n^+-substrate devices are similar to a resistance. Also it can be observed that the post breakdown resistance R_{bd} has a distinct maximum which shifts towards higher currents with increasing current compliance I_c. For higher currents the post breakdown resistance R_{bd} decreases and becomes approximately inversely proportional to the current, i. e. R_{bd} ~1/I.

It should be noted that these characteristics show resemblance with that of a programmed *antifuse* [128]. The term *antifuse* will be explained in section 5.9.

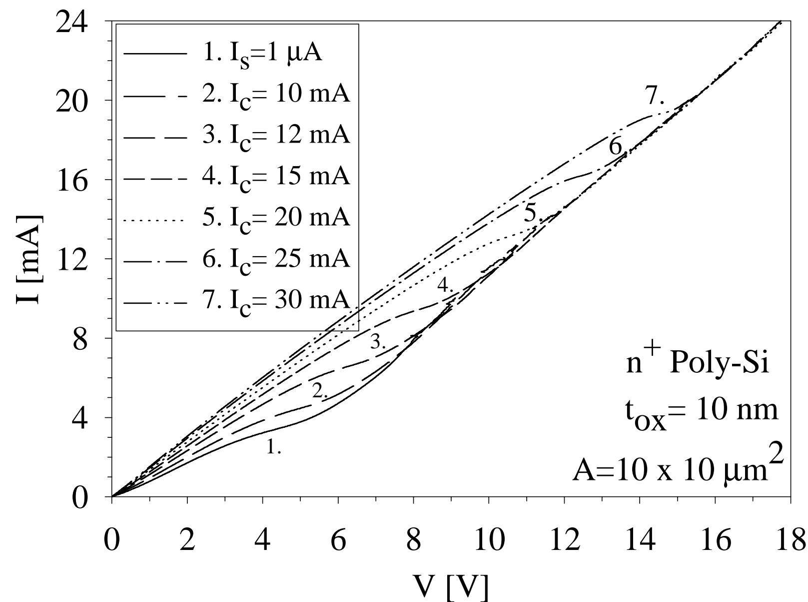

Figure 5.2: Post breakdown I-V characteristics of n^+ poly-Si/SiO_2/n^+-substrate MOS capacitors. The stress current was chosen to be I_s=-1 μA. Multiple I-V characteristics were measured with increasing current compliance I_c.

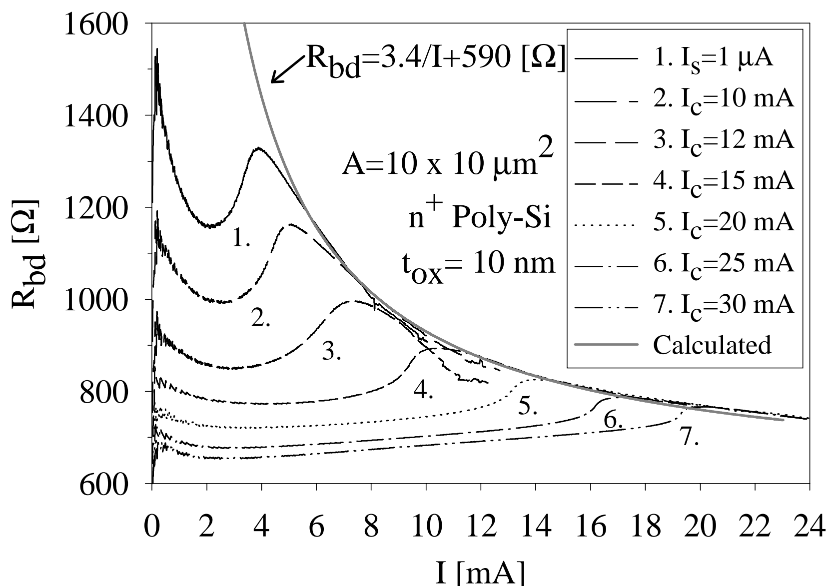

Figure 5.3: Post breakdown R-I characteristics of n^+ poly-Si/SiO_2/n^+-substrate MOS capacitors. Multiple R-I characteristics are plotted with increasing current compliance I_c.

In the next section a model is developed which will explain the measured post-breakdown I-V characteristics of n^+ poly-Si/SiO_2/n^+-substrate structures. The dependence on the physical parameters involved in the breakdown process will also be examined.

5.5 Modeling of the I-V characteristics after breakdown

In this section the post breakdown I-V characteristics of the linear n^+ gate- n^+ substrate link are modeled. Recently, Suñé *et al.* [129] showed that the current after hard-breakdown can be modeled as atomic-size conduction channels with radius in the r_c=1 to 10 nm range, which behave as classical Sharvin point contacts or Quantum point contacts. However, they assumed that thermal effects are limited. For currents in the range of ∼mA and a conductive channel in the ∼nm range, the current density through the breakdown site will be in the order of $J_{bd} \approx 10^{11}$ A/cm^2 and thus *Joule heating* can not be neglected.

Since thermal effects play a significant role in (high power)breakdown of the gate oxide an electro-thermal model has been developed which takes both the electrical as well as the thermal effects into account.

5.5.1 An electro-thermal model

In this section an electro-thermal model is presented [130, 131, 132, 133] which quantitatively describes the current-voltage characteristics after breakdown of the linear gate-substrate link. This model can also be used to study the dependence of the breakdown power on several physical characteristics, like the size of the link after breakdown and the resistance of the gate-substrate link after breakdown. The approach of this electro-thermal model is as following :

We start with the basic heat transfer equation :

$$C_t \frac{\partial \vec{T}}{\partial t} = -\nabla \cdot \vec{S} + H \tag{5.1}$$

with:

$$\vec{S} = \kappa \nabla \vec{T} \tag{5.2}$$

Where C_t is the thermal heat capacity, $\vec{T}$ is the temperature of the lattice, $\vec{S}$ is the heat flux and H is the heat generation.

The following assumptions are made :

- **Steady-state**

  As a fist order approximation, we are going to investigate only steady-state conditions, so the thermal capacitors are not taken into account.

$$C_t \frac{\partial \vec{T}}{\partial t} = 0 \tag{5.3}$$

- **Spherical symmetry**

  If the heat generating area has a spherical- or cylindrical symmetry, the temperature distribution in the silicon can be evaluated relatively easily. Usually this symmetry does not occur in semiconductor devices, however for our post breakdown link this is quite a good approximation as can be observed from [134, 135] and was evaluated using TEM measurements, as will be shown later on in section 5.6.

  Since the size of the link is much smaller than the thickness of the conductive silicon layers on both sides of the dielectric, modeling the temperature gradient and the resultant heat conduction by a simple sphere is a good

approximation.

Under this assumption we can simplify this 3D system into a 1D system by using spherical co-ordinates :

$$\nabla \cdot \vec{S} = \frac{1}{r^2}\frac{\partial}{\partial r}\left[r^2 \kappa \frac{\partial T(r)}{\partial r}\right] \tag{5.4}$$

- **All heat is generated uniformly (with power P) in a sphere with radius $\mathbf{r}_c$**

  Next, let us assume that the heat which is generated by *Joule heating* is dissipated entirely within the link itself. This means that it is assumed that the SiO_2 layer is infinitely thin compared to the radius r_c of the gate-substrate link ($r_c \gg t_{ox}$.).

  This is plausible to assume, since the current density is the highest inside the core. So, it is assumed that the gate-substrate link after breakdown consists of a spherical core with dimensions r_c in which all the heat is generated uniformly and that all equipotentials are concentric, see Fig. 5.4.

$$H = \frac{P}{4/3\pi r_c^3} \tag{5.5}$$

with :

$$P = I^2 \cdot R_c \tag{5.6}$$

Where P is the total heat generation, r_c is the radius of the core of the link, I is the current flowing through the link and R_c is the resistance of the link.

Under these assumptions the temperature distribution outside the core of the gate-substrate link can be described as [130, 133] :

$$T(r) = \frac{P}{4\pi\kappa r} + T_{amb} \quad r > r_c \tag{5.7}$$

Here T_{amb} is the ambient temperature, which is approached for $r \rightarrow \infty$.

Next, the core radius of the gate-substrate link after breakdown r_c can be evaluated by making use of Eq. 5.7, which results in :

$$r_c = \frac{I_{bd}^2 R_{c,bd}}{4\pi\kappa\left[T(r_{c,bd}) - T_{amb}\right]} \tag{5.8}$$

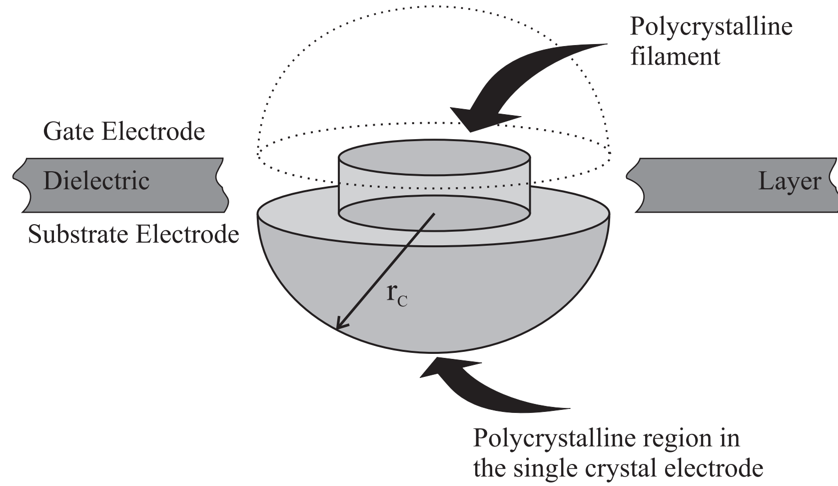

Figure 5.4: Schematic representation of the gate-substrate link after breakdown . It is assumed that the link consists of a spherical core with dimensions r_c in which all the heat is generated uniformly, i.e. $r_c \gg t_{ox}$ and that all equipotentials are concentric.

Where $T(r_{c,bd})$ is the temperature of the core at breakdown, which is the melting temperature of the dielectric layer, in this case SiO_2, $T(r_{c,bd})=T_{SiO_2}=1900$ K. I_{bd} is the current at breakdown, which is just the **maximum** current that flows through the gate-substrate link **during** formation of the link and $R_{c,bd}$ is the resistance of the gate-substrate link at breakdown.

Let us now evaluate the resistance of the gate-substrate link. Inside the core of the link a uniform current density is assumed, which is given by Eq. 5.9 :

$$J_c = \frac{I}{2\pi r_c^2} \quad r < r_c \tag{5.9}$$

The current density outside the core of the link is approximated as a radial flow and at point r, the current density is given by Eq. 5.10 :

$$J = \frac{I}{2\pi r^2} \quad r > r_c \tag{5.10}$$

The resistance of the core of the gate-substrate link can now be derived, since a uniform current density in the link implies a constant electric field strength and thus by making use of Eq. 5.9 the resistance of the core of the link after breakdown would take the form of :

$$R_c \approx \frac{V_c}{I} = \frac{E_c 2r_c}{I} = \frac{2\rho_c(T) J_c r_c}{I} = \frac{\rho_c(T)}{\pi r_c} \tag{5.11}$$

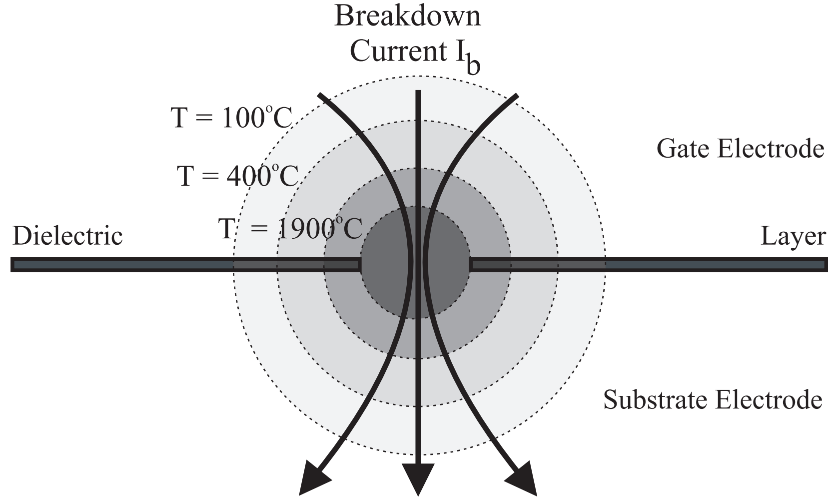

Figure 5.5: Schematic representation of the temperature distribution outside the core of the gate-substrate link at breakdown. The breakdown current I_{bd}, produces sufficiently high temperatures to melt the silicon (and SiO_2 film) over a small volume centered around the point of breakdown.

Where V_c is the voltage across the gate-substrate link, E_c the electrical field across it and ρ_c(T) is the electrical resistivity of the core material.

The resistance outside the core of the gate-substrate link can also be derived. It is reasonable to assume that the gate-substrate link consists of a mixture of (poly-) Si, SiO and SiO_2. For simplicity let us assume that it consists only of polycrystalline silicon as depicted in Fig. 5.4. Since the conductive medium inside and outside the core of the link is different, these two regions should be treated separately. The resistance outside the core of the gate-substrate link consists of a spreading resistance from the substrate electrode $R_{s,sub}$ and a spreading resistance from the gate electrode $R_{s,gate}$ and they can be expressed as [8, 133] :

$$R_{s,tot} = R_{s,gate} + R_{s,sub} = \frac{\rho_g(T)}{2\pi r_c} + \frac{\rho_s(T)}{2\pi r_c} \tag{5.12}$$

Where $R_{s,tot}$ is the total spreading resistance, ρ_g(T) is the electrical resistivity of the gate material and ρ_s(T) is the electrical resistivity of the substrate material.

The total resistance of the gate-substrate link can now be expressed using Eq. 5.11 and 5.12 and is just the sum of the core resistance and the spreading resistance of the gate and substrate electrode :

$$R_l = R_c + R_{s,gate} + R_{s,sub} = \frac{2\rho_c(T) + \rho_g(T) + \rho_s(T)}{2\pi r_c} \tag{5.13}$$

It is now also possible to express the resistance of the link at breakdown $R_{l,bd}$ as a function of the breakdown current I_{bd} by using Eqs. 5.8 and 5.13, which results in :

$$R_{l,bd} = \frac{\sqrt{2(2\rho_{c,bd} + \rho_{g,bd} + \rho_{s,bd})\kappa \left[T_{r_{c,bd}} - T_{amb}\right]}}{I_{bd}} \approx \frac{V_{f,bd}(\rho, \kappa, T_{SiO_2})}{I_{bd}} \tag{5.14}$$

Where $V_{f,bd}$ is called the *characteristic* gate-substrate link voltage. Since $V_{f,bd}$ consists only of material parameters at breakdown, it acts like a Figure of Merit(FOM) which enables us to compare different post breakdown I-V characteristics with each other for different breakdown currents I_{bd}.

In the discussion above, it is assumed that the thermal conductivity κ is constant over the whole temperature range. However, it should be noted that κ for Si is temperature dependent, varying from κ=1.56 [W/Kcm] at room temperature(T_{amb}=300 K) to κ=0.25 [W/Kcm] at T_{Si}=1681 K close to the melting point of Si [136].

An appropriate expression for the temperature dependence of κ can be found in [137, 132] and is given by Eq. 5.15 : [1]

$$\kappa(T) = \kappa_0 T^{-4/3} \tag{5.15}$$

Where κ_0=3110 [$WK^{1/3}cm^{-1}$].

The thermal conductivity of silicon has also been measured from 3 K to the melting point of Si by Glassbrenner *et al.* [136] and it has been confirmed that Eq 5.15 fits the data of Glassbrenner *et al.* at least within 8% accuracy.

By taking the temperature dependence of κ into account, the temperature distribution outside the core of the gate-substrate link Eq. 5.16 is now described by making use of Eq. 5.4 :

$$T(r) = \left[T_{amb}^{-1/3} - \frac{P}{12\pi\kappa_0 r}\right]^{-3} \tag{5.16}$$

The core radius of the gate-substrate link after breakdown r_c can be evaluated using Eq. 5.16, which results in :

$$r_c = \frac{I_{bd}^2 R_{c,bd}}{4\pi\kappa_0 \left[T_{amb}^{-1/3} - T(r_{c,bd})^{-1/3}\right]} \tag{5.17}$$

[1] Actually, this is one of the key features, why the radius of the gate-substrate link can be increased for $I>I_{bd}$ at elevated temperatures, while for $I<I_{bd}$ the heating of the link is negligible. This will be explained later on.

It is now again possible to express the resistance of the link at breakdown $R_{l,bd}$ as a function of the breakdown current I_{bd} by using Eqs. 5.17 and 5.13, which results in :

$$R_{l,bd} = \frac{\sqrt{6(2\rho_{c,bd} + \rho_{g,bd} + \rho_{s,bd})\kappa_0 \left[T_{amb}^{-1/3} - T(r_{c,bd})^{-1/3}\right]}}{I_{bd}} \approx \frac{V_{f,bd}}{I_{bd}} \quad (5.18)$$

This is basically the same expression as Eq. 5.14.

In the discussion above, it was also assumed that the SiO_2 layer is infinitely thin compared to the radius r_c of the gate-substrate link. However for low power programming, the radius of the core r_c might be comparable to or even smaller than the thickness of the SiO_2 layer. This means that for low power programming it is necessary to consider the resistance contribution from the conductive channel as well. Modeling the conductive channel as a cylinder of height t_{ox} and radius r_c as depicted in Fig. 5.4, the resistance of the core of the link R_c can be expressed as :

$$R_c \approx \frac{V_c}{I} = \frac{\rho_c(T)}{\pi r_c} + \frac{\rho_c(T) t_{ox}}{\pi r_c^2} = \frac{\rho_c(T)}{\pi r_c}\left[1 + \frac{t_{ox}}{r_c}\right] \quad (5.19)$$

Note that the second term in Eq. 5.19 is inversely proportional to the square of the core radius r_c, which means that the resistance of the link after breakdown $R_{l,bd}$ is no longer inversely proportional to the breakdown current I_{bd} if we take into account the finite SiO_2 layer thickness. Eqs. 5.14 and 5.18 are therefore only a fairly good approximation for the resistance of the link at breakdown as long as $r_c \gg t_{ox}$.

Fig. 5.6 displays the core radius of the breakdown site r_c as a function of the electrical power which is used to form the link during breakdown. The core radius r_c is calculated using Eq. 5.8, assuming a thermal conductivity of κ_{eff}=0.25 [W/Kcm] close to the melting point of Si. Also Eq. 5.17 is plotted in Fig. 5.6. From Fig. 5.6 it can be noted that during breakdown there is no large difference between Eq. 5.8 and Eq. 5.17.

Moreover it can be observed that the size of the conductive link r_c can be strongly influenced by the electrical power ($P=I_{bd}^2 \cdot R_{c,bd}$) dissipated during breakdown and is typically between 10 nm and 100 nm for practical values of P. For very low power $P<10^{-3}$ W, the link size is calculated to be below 1 nm. However, for these extremely small link sizes the link can probably not be formed. This will most likely lead to soft breakdown(SB) of the gate oxide, as will be explained later on.

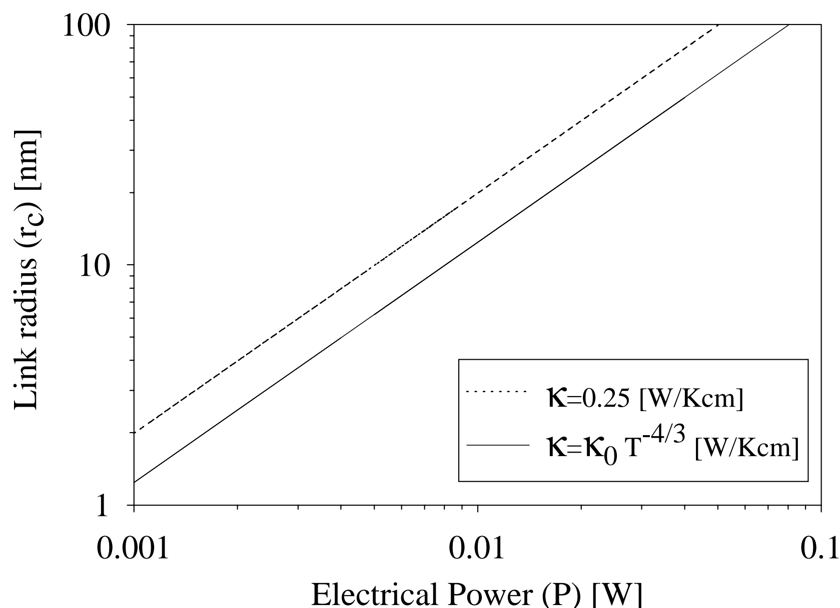

Figure 5.6: Calculated core radius of the gate-substrate link after breakdown as a function of the electrical power which is used to form the link during breakdown, using Eq. 5.8 and Eq. 5.17.

5.5.2 Model verification

We can now use our electro-thermal model derived in the previous section and compare it with measurements (see Fig. 5.3). First of all the value of the resistance after breakdown R_{bd} is determined solely by the **maximum** current I_{bd} which flows through the link **during** breakdown. The resistance increases at a current just before I_{bd} due to heating of the conductive link ($I \approx I_{bd}$). After this the post breakdown resistance of the link R_{bd} drops when the material of the conductive channel melts and continues to decrease beyond the original resistance as the current exceeds the breakdown current ($I > I_{bd}$). This decrease in resistance is due to the permanent widening of the conductive gate-substrate link.

From Fig. 5.3 it can be observed that for high currents, i.e. $I > I_{bd}$ the resistance can be well described using a 1/I dependence. This indicates that Eq. 5.14 is a fairly good expression for the value of the resistance at breakdown. The series resistance of our devices is determined to be 590 Ω. Using Eq. 5.8 or Eq. 5.17 the core radius of the gate-substrate link after breakdown r_c can now also be determined and is in the order of $r_c \approx 25$ nm for $I_{bd}=4$ mA.

It should however be noted that the melting of the link takes place before the current reaches the breakdown current I_{bd}. This is because melting of the link, which most likely consists mainly of Si, has a lower melting point ($T \approx 1700$ K) than SiO_2 ($T \approx 1900$ K), so melting of the conductive link takes place at a lower

current ($I<I_{bd}$) than melting of the initial dielectric, i.e. widening of the link ($I \geq I_{bd}$).

From the discussion above it can thus be concluded that the breakdown current I_{bd} which flows through the link during breakdown, produces sufficiently high temperatures to melt the silicon and SiO_2 film over a small volume centered around the point of breakdown. After breakdown a small electrically conductive link connecting the gate and substrate is formed in the dielectric layer with the properties of a resistance. It should however be noted that all this was derived under the assumption that all energy stored on the MOS capacitor (and parasitic capacitances) is released through the breakdown path during discharging and that parallel conduction through the oxide after breakdown is negligible, i.e. t_{ox} >4 nm.

The *characteristic* gate-substrate link voltage $V_{f,bd}$ is determined from Fig. 5.3 to be $V_{f,bd}$=3.4 V for our devices. This is an important result, since from Eq. 5.14 it was concluded that $V_{f,bd}$ only depends on the material parameters ρ,κ and T_{SiO_2}. So this means that $V_{f,bd}$ does not depend on the gate oxide thickness t_{ox}. This has important implications for ultra-thin gate oxides. With decreasing gate oxide thickness stressing takes place at lower voltages V_s. If the stress voltage V_s becomes lower than the *characteristic* gate-substrate link voltage $V_{f,bd}$ the post breakdown I-V characteristics can no longer be described using our electro-thermal model. The most likely explanation for this is that for stress voltages $V_s < V_{f,bd}$ the formation of the gate-substrate link due to thermal effects (*Joule heating*) is no longer possible. This most likely means that at breakdown the link does no longer melt. Under these conditions soft breakdown may occur, which will be explained in more detail in section 5.8.

Note that under the condition of $V_s < V_{f,bd}$, the link size after breakdown is extremely small and thus the condition $r_c \gg t_{ox}$ may no longer hold. However, from Eq. 5.19 it can be concluded that for this condition the resistance of the core of the link R_c after breakdown will be even higher. This means that according to our electro-thermal model the *"characteristic"* voltage after breakdown should be even higher than $V_{f,bd}$.

It is thus clear that the link after breakdown is entirely described by the filament cross-section formed after breakdown. The core radius of the gate-substrate link after breakdown depends on the breakdown current I_{bd}. However it can be noted from Fig. 5.3 that the stress current I_s used to breakdown the gate oxide is much lower than the breakdown current $I_{bd} \approx$4 mA measured afterwards, which determines the value of the resistance after breakdown. The reason for $I_{bd} > I_s$ might be attributed to the current increase caused by the discharging of the MOS capacitor. The breakdown current I_{bd} is namely also influenced by the dissipation

of energy stored in the MOS capacitor before breakdown ($=\frac{1}{2}C_{ox}\Delta V^2$). A simple first order equivalent electrical circuit which describes oxide breakdown under CCS injection conditions has been evaluated and will be presented in the next section.

5.5.3 Modeling of breakdown of the gate oxide

In this section a simple first order equivalent electrical circuit which describes oxide breakdown under CCS injection conditions will be presented. Before breakdown the structure simply consists of the oxide capacitance C_{ox} and parasitic capacitance C_{par}. By applying a constant current stress I_s large enough to induce Fowler-Nordheim tunneling through the gate oxide an additional leakage path through the gate oxide is enforced. This is best modeled by placing a highly *non-linear* resistance R_{FN} in parallel with the capacitor, as is indicated in Fig. 5.7. Furthermore, there will be a voltage drop over the poly-Si gate and Si-substrate due to series-resistance, which can be modeled simply as resistances (R_{poly} and R_{sub}). Also the parasitic capacitances of the measurement set-up are included, which are terminated by a $R_{probe-tip}$=1 MΩ series resistance to minimize their discharge current during breakdown. The complete equivalent electrical circuit which describes oxide breakdown under CCS injection conditions is given by Fig. 5.7.

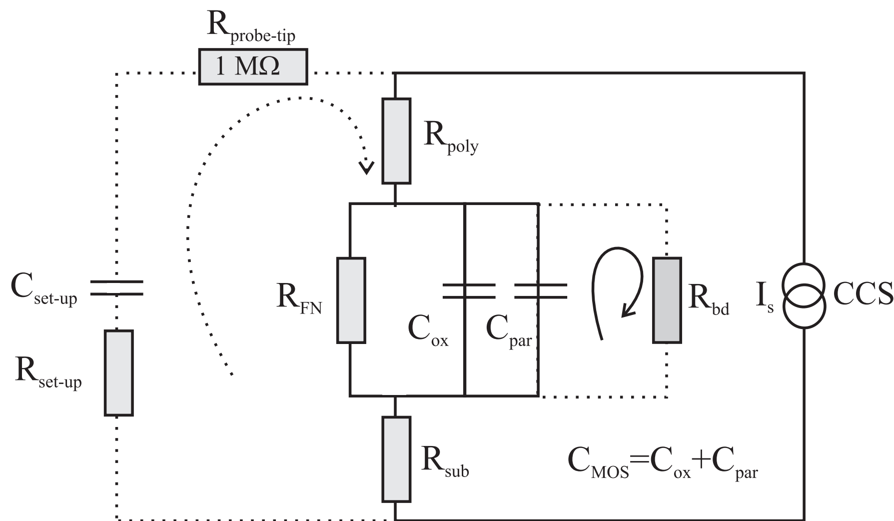

Figure 5.7: A simple first order equivalent electrical circuit which describes oxide breakdown under CCS conditions.

At breakdown, it is assumed that the total energy stored on the MOS capacitor including parasitic capacitors are released through the breakdown path during discharging of the capacitors. Assuming that the current due to discharging of the measurement set-up can be neglected (due to the $R_{probe-tip}$=1 MΩ series resistance) the release of energy during breakdown is only due to the MOS capacitor and is given by :

$$E_{dis} = \frac{1}{2} C_{MOS} \left(V_{before}^2 - V_{after}^2 \right) \approx \frac{\epsilon_{ox} A}{2 t_{ox}} \left(V_s^2 - V_{f,bd}^2 \right) \tag{5.20}$$

Where C_{MOS}=C_{ox}+C_{par} is the total MOS capacitance, which is equal to the oxide capacitance and parasitic capacitances of the MOS structure. V_{before} and V_{after} are respectively the voltage drop before and after breakdown, A is the MOS capacitor area, V_s is the (stress) voltage at the stress current I_s and $V_{f,bd}$ the *characteristic* voltage after breakdown.

Note that Eq. 5.20 only hold for V_{before} >V_{after}, i.e. V_s >$V_{f,bd}$ as was already explained in the previous section.

The maximum current which flows through the breakdown path determines the post breakdown I-V characteristics. This current is caused by the discharging of the MOS capacitor during breakdown I_{cap} and due to the parallel conduction through the oxide during and after stress I_s under CCS injection conditions. The breakdown current I_{bd} can be calculated, resulting in Eq. 5.21 :

$$I_{bd} = I_s + I_{cap} = I_s + \frac{\Delta Q}{\Delta t} \approx I_s + C_{MOS} \frac{\Delta V}{\Delta t} \approx I_s + \frac{\epsilon_{ox} A}{t_{ox}} \left(\frac{V_s - V_{f,bd}}{\tau_{bd}} \right) \tag{5.21}$$

Where Q is the total charge on the MOS capacitor before breakdown and τ_{bd} is the discharging time of the capacitor during breakdown.

The only parameter we do not know exactly is the time in which the discharge of the MOS capacitor was completed. This is however an important parameter and has a large influence on the breakdown current I_{bd}, as can be noted from Eq. 5.21. The discharging time τ_{bd} is therefore taken to be equal to experimental values found in literature, as will be discussed later on. From Eqs. 5.20 and 5.21 it can be noted that if V_s >$V_{f,bd}$ (and τ_{bd} →0) the I-V characteristics after breakdown are completely determined by the energy release during discharging of the MOS capacitor. This is often observed for thick oxides t_{ox} >5 nm and limited stress currents I_s. However if V_s ≈$V_{f,bd}$ (or $\tau_{bd} \rightarrow \infty$) the energy release during discharging of the MOS capacitor can be neglected and the post breakdown I-V characteristics are determined by the stress current I_s only. This is the case for thin gate oxides (t_{ox} <4 nm) and high stress currents I_s.

In our thick-oxide gate devices, for a capacitor area of A=10 $\times$ 10 μm^2 and an oxide thickness of t_{ox}=10 nm the oxide capacitance is approximately C_{ox} $\approx$0.4 pF. The parasitic capacitance C_{par} (gate overlap and bondpad) is determined to be C_{par} $\approx$0.6 pF. This means that the total capacitance of the MOS structure is C_{MOS}=C_{ox}+C_{par} $\approx$1 pF. For a stress current of I_s=1 μA, the stress voltage at this current is approximately V_s $\approx$13 V. If we now want to calculate the current which flowed through the link during breakdown the only parameter we need to know is the time in which the discharge of the capacitor was completed. Cohen *et al.* [138, 139] measured the discharging of their capacitors on t_{ox}=6.5-9.5 nm equivalent oxide thickness using a fast digital oscilloscope. They showed that the discharge of their capacitors was completed in about τ_{bd}=4 ns. This is much longer than the time period necessary to reach thermal equilibrium τ_{th}, which is in the order of [133] :

$$\tau_{th} \approx \frac{L_{th}^2}{D_{th}} \approx \frac{(100\ [nm])^2}{0.87\ [cm^2/s]} = 0.1\ [ns] \tag{5.22}$$

Where L_{th} is the dimension of the volume being heated during breakdown and D_{th} [9] is the thermal diffusivity of silicon, here taken at T=300 K.

If the duration at which the breakdown current flowed is much shorter than the time to reach thermal equilibrium , i.e. $\tau_{bd} < \tau_{th}$, a stable state will not be reached and no stable conductive link can be formed. Moreover, the reaction between Si and SiO_x also takes time, making the time necessary for which the breakdown current needs to flow much longer than that required for thermal equilibrium. So τ_{bd}=4 ns seems to be a realistic value for the time during which the breakdown current I_{bd} must flow through the breakdown path to form a stable link.

Using Eq. 5.21 this results in a breakdown current of approximately I_{bd}=I_s+1 [pF]$\cdot$10 [V]/4 [ns]$\approx$2.5 mA, which is in the same order as the experimentally obtained value of I_{bd}, as can be seen from Fig. 5.3. Note that the breakdown current I_{bd} is completely determined by the current I_{cap} due to discharging of the MOS capacitor. The stress current I_s does not influence (apart from the stress voltage V_s) the breakdown current at all in our devices. Also note that the discharge of parasitic capacitances of the measurement set-up is neglected, although they are probably much larger than the MOS capacitance itself. This assumption is valid since the $R_{probe-tip}$=1 MΩ series resistance close to the probe tip limits the discharge of parasitic capacitances in the wafer measurement set-up at breakdown.

5.5.4 Summary

It can be concluded that high power dielectric breakdown of SiO_2 (P>0.01 W) is caused by a local catastrophic runaway phenomenon. The I-V characteristics after breakdown are determined entirely by the filament cross-section formed through the emission of energy stored in the MOS capacitor before breakdown. The post breakdown characteristics of n^+-poly/oxide/n^+-substrate MOS capacitors resemble that of a resistance, its value is determined entirely by the filament cross-section formed through the dissipation of energy stored in the MOS capacitor before breakdown. The size of the conductive link can be strongly influenced by the electrical power ($V_{bd} \cdot I_{bd}$) dissipated during breakdown and is typically between 10 nm and 100 nm. An electro-thermal model was developed which is able to explain the measurements.

5.6 I-V characteristics after breakdown Part II: non-linear characteristics

In this section the post breakdown characteristics of n^+ poly-Si/SiO_2/p-substrate NMOS capacitor structures are studied. It should be noted that this configuration is much more complicated to investigate.

First of all the post breakdown I-V characteristics of n^+ poly-Si NMOS gate devices are more difficult to interpreted compared to n^+ poly-Si/SiO_2/n^+-substrate structures. In the latter case the conduction mechanism after breakdown is mainly due to electrons. However, for n^+ poly-Si NMOS gate devices, apart from electrons, holes might also contribute to the conduction process after breakdown (bulk conduction).

Furthermore, at breakdown a link is formed in the SiO_2 connecting the gate and substrate. For the n^+ poly-Si NMOS gate devices this means that at breakdown the structure resembles that of a diode biased in high injection conditions. It is known that the turn-on and turn-off transients of a diode are completely different than that of a resistance. This results from the time needed for the minority charge distribution to change to the new bias condition after breakdown. The discharging time of the n^+ poly-Si NMOS capacitor will therefore be much longer compared to n^+ poly-Si/SiO_2/n^+-substrate devices, i.e. $\tau_{bd} > 4$ ns. This will also influence the breakdown current I_{bd}. The current which flows through the link during discharging of the n^+ poly-Si NMOS capacitors will therefore be much lower compared to the n^+ poly-Si/SiO_2/n^+-substrate devices at the same stress conditions.

First of all the post breakdown characteristics of the n^+ poly-Si/SiO_2/p-substrate structures after high power (P>0.01 W) breakdown are studied. Next the I-V

characteristics after low power breakdown are investigated. Carefully designed structures with on-chip series resistors are used to ensure low power breakdown. Finally it will be shown that if a limited amount of current flows through the conductive link, soft-breakdown may occur.

5.6.1 I-V characteristics after high power breakdown

In this section the post breakdown characteristics of n^+ poly-Si NMOS gate devices after high power breakdown are studied.

The forward and reverse I-V characteristics

The I-V characteristics after high power breakdown of n^+ poly-Si NMOS capacitors with different gate area are presented in Fig. 5.8.

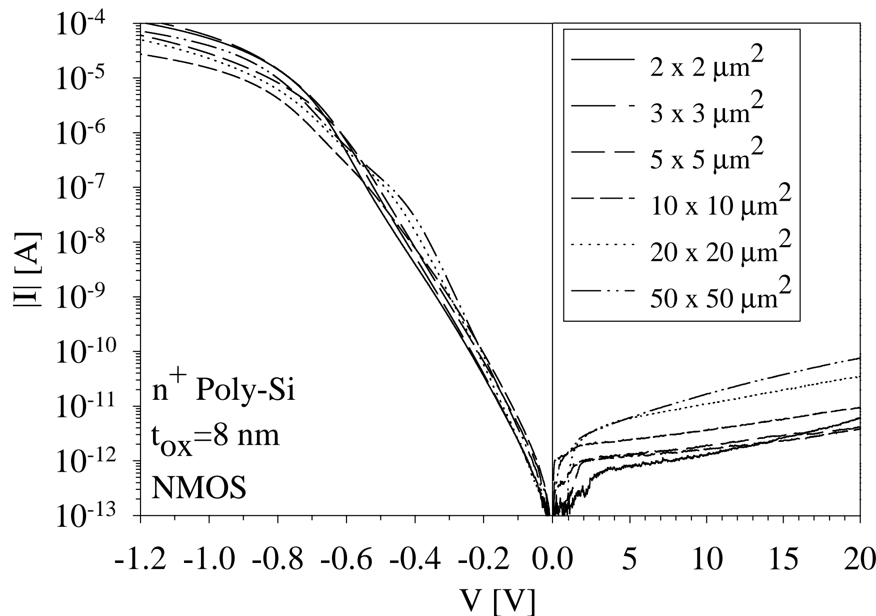

Figure 5.8: Capacitor area dependence of the n^+ poly-Si NMOS I-V characteristics after high power oxide breakdown. The stress current was fixed at I_s=-10 mA.

To ensure high power breakdown, a large breakdown current I_{bd} is needed. This can be achieved by using a high stress current I_s. To enable a high stress current, the 1 MΩ series resistance close to the probe tip has to be removed during stress. This is since for high I_s the voltage drop over the resistor will be very high (>100 V) which can not be supplied by the measurement equipment. However, by removing the 1 MΩ resistance there will also be a large current flowing through the link at breakdown due to discharging of parasitic capacitances in

the measurement set-up. This will also influence the current which flows through the link during breakdown of the gate oxide I_{bd}.

Fig. 5.8 displays the I-V characteristics after high power breakdown. The stress current (and compliance) was fixed at I_s=-10 mA (gate injection) and the capacitor area was varied between A=4 and 2500 μm^2. The $R_{probe-tip}$=1 MΩ series resistance was removed during stress.

From Fig. 5.8 it can be observed that after high power breakdown the I-V characteristics resemble that of a diode with an ideality factor close to n=1. This low value of the ideality factor reflects the good quality of the junction. Also note that at low -V_g the forward current does not depend on the capacitor area. The reverse current is low and does not depend strongly on the capacitor area. After breakdown a gated diode with gate connected to the diode [66] is formed.

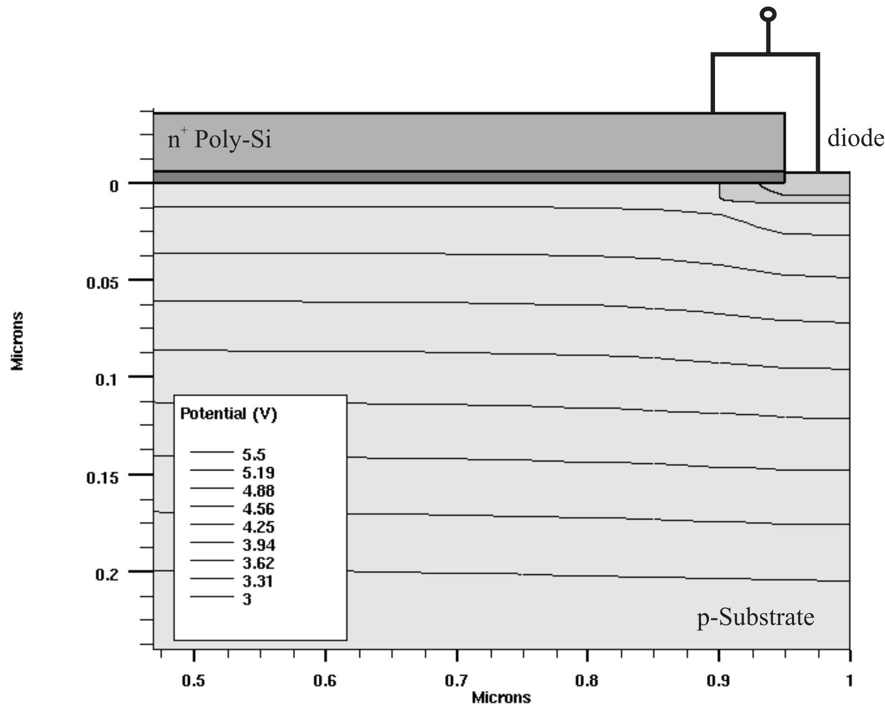

Figure 5.9: Simulated equipotential lines of our n^+ poly-Si NMOS gate devices after breakdown (gated diode) for a reverse voltage of +V_g=5 V. The gate action is clearly visible.

For this gated diode structure at +V_g no inversion layer can form and the device is biased in deep depletion for +V_g. The diode breakdown voltage was determined to be high (V_b=60 V) , it resembles that of a planar junction due to the gate action, see Fig. 5.9.

It is assumed that during breakdown the oxide melts around a small spot

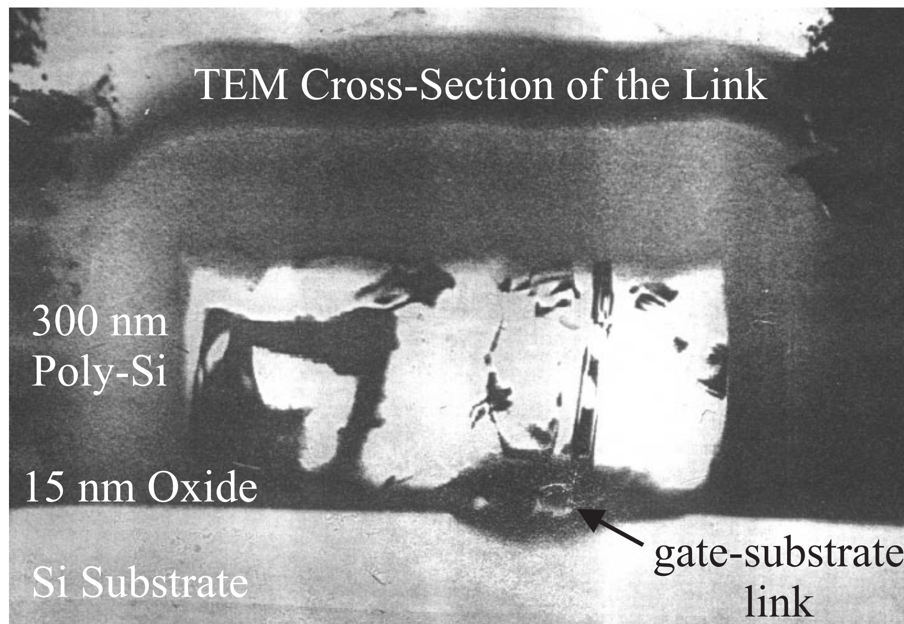

Figure 5.10: Transmission Electron Microscope(TEM) of a the gate-substrate link after high power breakdown. The size of the link has a radius of about r_c=30-40 nm. TEM photo courtesy of G. Fleuren, Philips Nijmegen.

centered around the point of breakdown and after breakdown a so-called gate-substrate link is formed in the oxide. This can also be observed in Fig. 5.10 using Transmission Electron Microscope(TEM). The size of the molten area determines the link size, therefore the size of the link depends strongly on the breakdown power as was already observed for the n^+ poly-Si/SiO_2/n^+-substrate structures. For high power breakdown, the link size of our n^+ poly-Si NMOS devices is in the order of r_c=10-40 nm.

Temperature dependence of the I-V characteristics

The temperature dependence of the post breakdown I-V characteristics of a high power formed device are shown in Fig. 5.11. At low forward voltage (-V_g) a strong temperature dependence is observed. For high forward voltages the series resistance limits the current and a reduced temperature dependence is observed. From the temperature dependence of the reverse current (+V_g) an activation energy close to $\mathcal{E}_{act}$=1.0 eV is derived, which indicates that the reverse current is dominated by the diffusion current in the Si substrate. The low leakage current in reverse direction and relatively high forward current indicate that the diode formed after breakdown is of good quality.

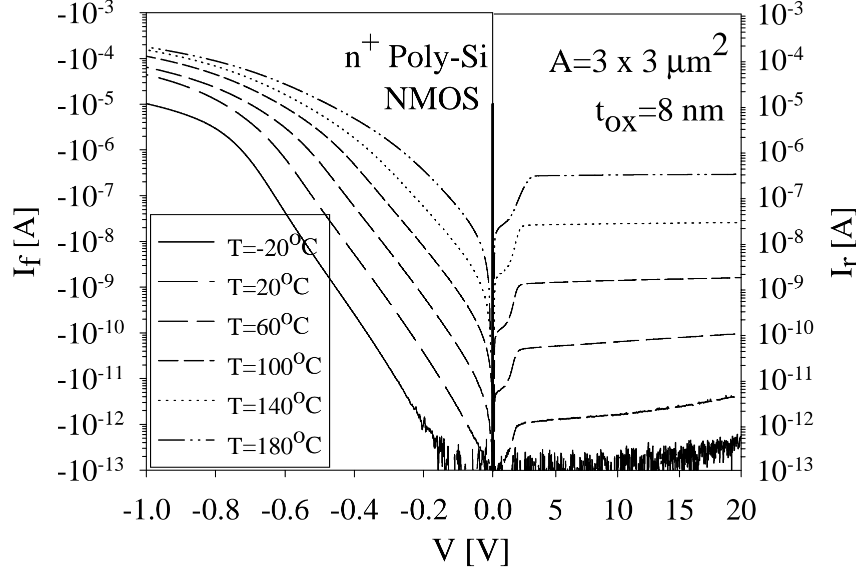

Figure 5.11: I-V characteristics after high power breakdown for -V_g and +V_g bias conditions of n^+ poly-Si NMOS capacitors. The stress current was fixed at I_s=-10 mA. The temperature after breakdown was varied from -20°C to 180°C.

Substrate dependence of the I-V characteristics

In this section the substrate doping dependence on the post breakdown characteristics of n^+ poly-Si NMOS gate devices after high power breakdown is studied. The stress current (and compliance) was fixed at I_s=-10 mA (gate injection) and the capacitor area is A=10 × 10 μm^2.

Fig. 5.12 displays the post breakdown I-V characteristics for a substrate doping of $N_{sub}=10^{16}$ cm^{-3} (Fig. 5.12, solid line) and $N_{sub}=10^{19}$ cm^{-3} (Fig. 5.12, dashed line). From the forward characteristics it is possible to extract the junction quality factor (n=1.2 (low N_{sub}) and n=2.2 (high N_{sub})). Note that the relatively high leakage current and junction quality factor (n=2.2) for the highly doped substrate is caused by Shockley-Read-Hall(SRH) generation and is therefore typical for highly doped p-n junctions. The reverse current for the highly doped substrate is high due to SRH and the breakdown voltage is low, V_b= 5.3 V.

It can thus be concluded that the I-V characteristics of the n^+-poly/oxide/p-substrate NMOS capacitors after high power breakdown can be interpreted in terms of an ideal nanometer scale gated diode with the gate connected to the diode. Next the post breakdown characteristics of n^+ poly-Si NMOS gate devices after low power breakdown are studied.

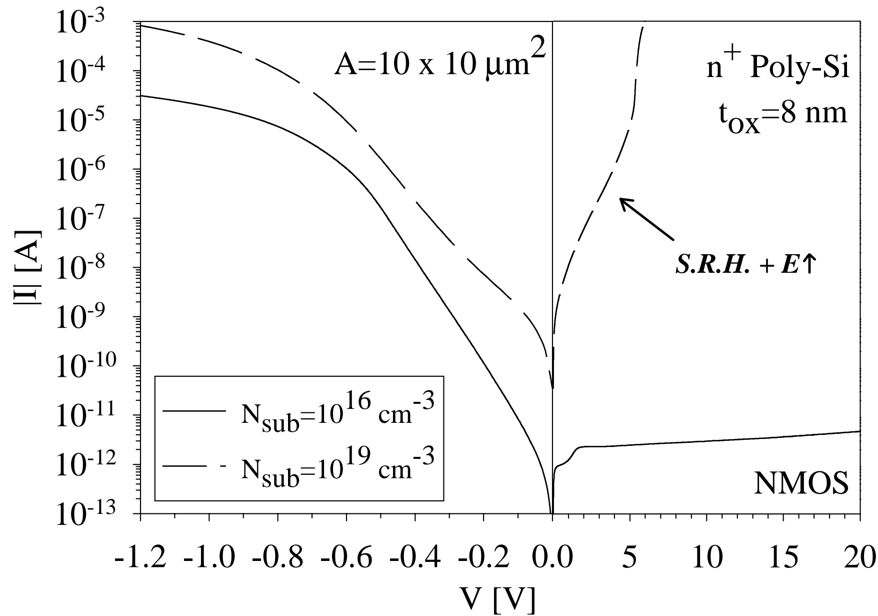

Figure 5.12: Post breakdown I-V characteristics for two different substrate doping $N_{sub}=10^{16}$ cm^{-3}(solid line) and $N_{sub}=10^{19}$ cm^{-3}(dashed line). The stress current was fixed at I_s=-10 mA.

5.6.2 I-V characteristics after low power breakdown

In this section the post breakdown characteristics of n$^+$ poly-Si NMOS gate devices after low power breakdown are studied. Controlled low power breakdown is ensured by placing a 1 MΩ series resistance close to the probe tip to limit the discharge of parasitic capacitances in the wafer measurement set-up. This is necessary condition to ensure low power breakdown, especially in thicker oxides. After breakdown of the gate oxide the 1 MΩ resistance was removed, so the post breakdown characteristics could be measured. Carefully designed structures with on-chip series resistors where used to minimize the current I_{cap} due to discharging of the test structures. Furthermore, the total capacitance of the devices is kept as low as possible and is in the order of C_{ox}=10-100 fF.

The forward and reverse I-V characteristics

The I-V characteristics after low power breakdown of n$^+$ poly-Si NMOS capacitors with different gate area are presented in Fig. 5.13. The stress current (and compliance) was fixed at I_s=-0.5μA (gate injection) and the capacitor area was varied between A=4 and 2500 μm^2.

Lets first interpreted the measurements assuming that the I-V characteristics resemble that of a gated diode with gate connected to the diode. From Fig. 5.13

it can be noted that the reverse current is low and does not depend strongly on the capacitor area. For low power breakdown, the forward current increases strongly with increasing capacitor area. The forward characteristics are non-ideal for low power breakdown, but become more ideal with increasing capacitor area. For larger gate area, the energy stored in the capacitance ($\frac{1}{2}C_{ox}\Delta V^2$) increases and as a result I_{bd} increases, resulting in high power breakdown. The size of the link and the material quality of the link depends strongly on the energy available during breakdown. With increasing gate area, I_{bd} increases and as a result a larger link size and improved material quality in the link is obtained. For low power breakdown the link material may consist of a mixture of Si, SiO and SiO_2. An increase in power will result in a more ideal diode because the link size increases and the material will become more Si like. Also for low power breakdown the size of the link can be below 10 nm giving rise to very high series resistances ($R_{s,tot} > 1$ MΩ). It can be noted that this series resistance is much higher compared to the n^+ poly-Si/SiO_2/n^+-substrate structures ($R_{s,tot} \approx$1500 Ω) at approximately the same stress current I_s. This can be explained by the fact that the total capacitance of the n^+ poly-Si NMOS gate devices is much lower, in the order of C_{ox}=10-100 fF.

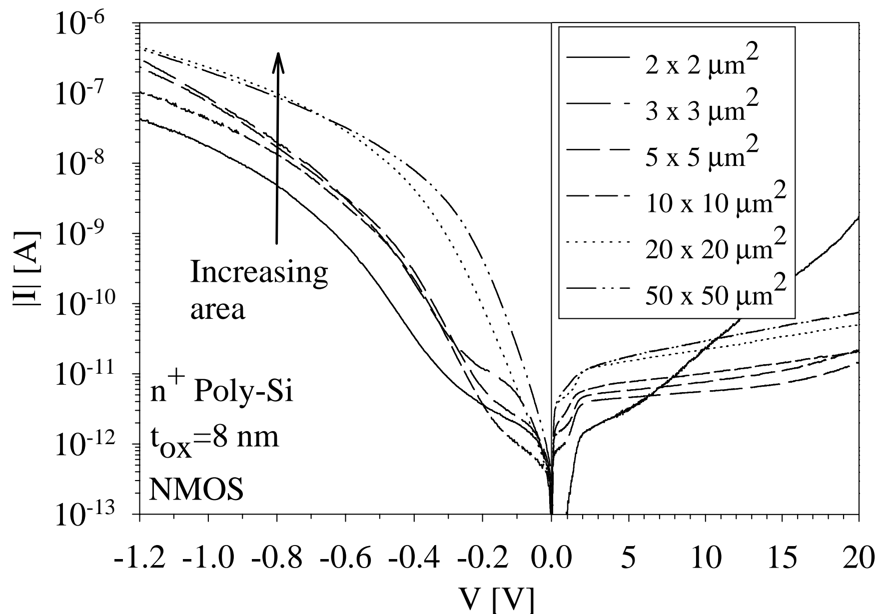

Figure 5.13: Gate area dependence of the n^+ poly-Si NMOS I-V characteristics after low power oxide breakdown. The stress current was fixed at I_s=-0.5 μA.

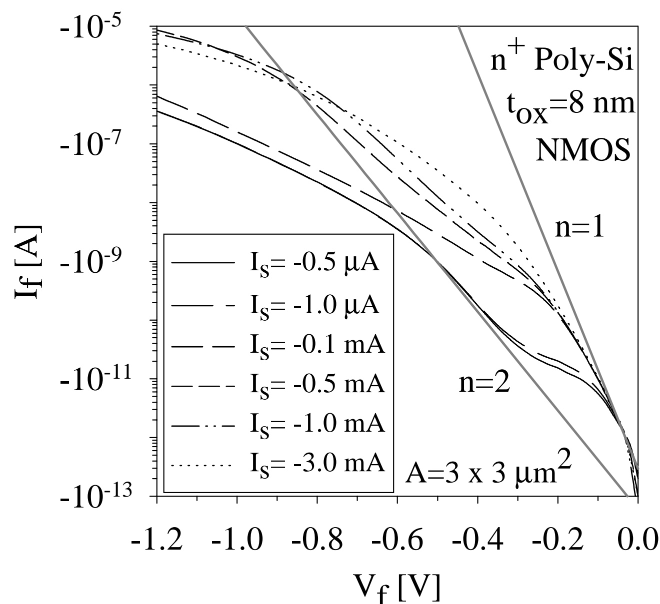

Figure 5.14: Post low power breakdown I-V characteristics of n^+ poly-Si NMOS capacitors, measured at -V_g. Multiple I-V characteristics are plotted with increasing stress current I_s.

Together with the turn-off transient behaviour of the diode formed at breakdown (τ_{bd} >4 ns) this will result in a much lower breakdown current I_{bd} and thus resulting in a smaller link size as for the n^+ poly-Si/SiO_2/n^+-substrate structures.

Fig. 5.14 displays the post low power breakdown forward I-V characteristics of our n^+ poly-Si NMOS capacitors as a function of the stress current I_s for a capacitor area of $A=3\times3\mu m^2$. It is again observed that the forward I-V characteristics (-V_g) strongly increase with increasing breakdown power and also become more ideal. At high forward voltages the spreading resistance $R_{s,tot}$ limits the current. By assuming a diode type behavior the ideality factor n of these diodes can be evaluated for different stress currents I_s. From Fig. 5.14 it can be observed that the ideality factor is between n=1 and n=2, shifting towards n=1 (more ideal diode) with increasing stress current I_s.

Next the temperature dependence of the post breakdown I-V characteristics of n^+ poly-Si NMOS capacitors after low power breakdown are investigated.

Temperature dependence of the I-V characteristics

The temperature dependence of the I-V characteristics of a low power formed device is depicted in Fig. 5.15. At low forward voltage (-V_g) a strong temperature dependence is observed. The activation energy is gate voltage dependent

and is approximately $\mathcal{E}_{act}$=0.6 eV at a forward voltage of V_f=-0.1 V. For high forward voltages the series spreading resistance limits the current and a reduced temperature dependence is observed, with an activation energy of $\mathcal{E}_{act}$=0.1 eV.

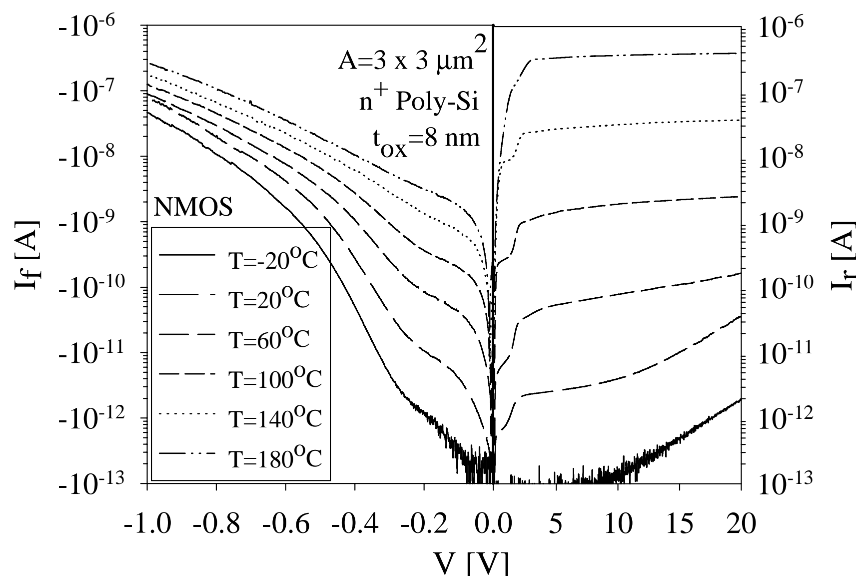

Figure 5.15: I-V characteristics after low power breakdown for $-V_g$ and $+V_g$ bias conditions of n^+ poly-Si NMOS capacitors. The temperature after breakdown was varied from -20°C to 180°C.

The temperature dependence of the reverse current ($+V_g$) is plotted in Fig. 5.16. An activation energy $\mathcal{E}_{act}$ of 0.59 eV is obtained at low temperatures and a $\mathcal{E}_{act}$ of 0.99 eV is found for elevated temperatures. This means that at low temperatures the reverse current is dominated by generation in the depletion region, while for high temperatures the diffusion current becomes dominant. This is confirmed by the gate area dependence of the reverse current, see Fig. 5.16. At low temperatures the reverse current depends on the capacitor area, indicating that the reverse current is dominated by generation in the depletion region. However, at high temperatures no gate area dependence is found which is consistent with the fact that the diffusion current is dominant in this temperature region. This shows that the surface generation rate is low even after high stress.

From Fig. 5.15 it can also be noted that at elevated temperatures the reverse current is higher compared to the forward current. This is different as observed for the post high power breakdown I-V characteristics, which resemble that of a

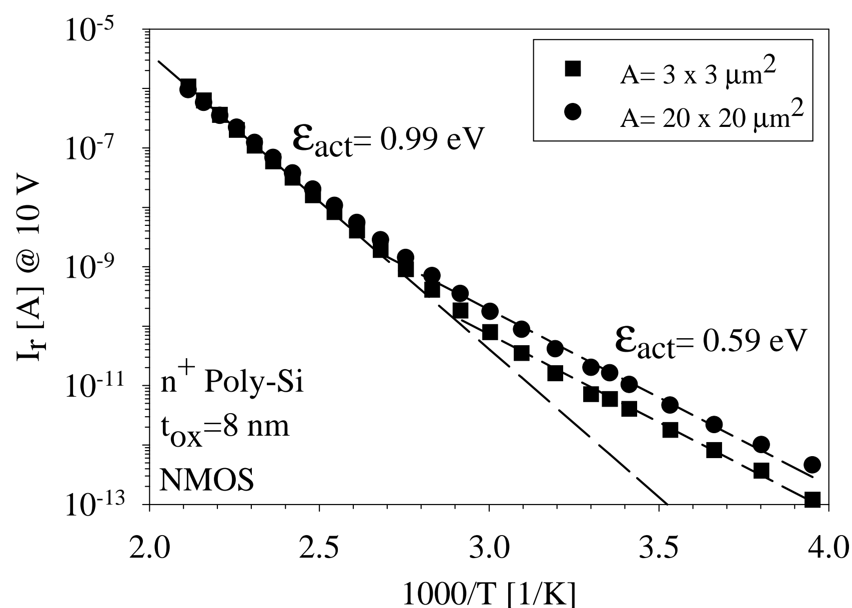

Figure 5.16: Temperature dependence after breakdown of the reverse ($+V_g$) post low power breakdown I-V characteristics of n^+ poly-Si NMOS capacitors. The temperature range is 25°C to 200°C.

gated diode, see Fig. 5.11. This raises questions about the possible conduction mechanism(s) after low power breakdown. The conduction mechanism after low power breakdown will be investigated in more detail in section 5.8. First however the post breakdown I-V characteristics of n^+ poly-Si NMOS capacitors are investigated if only a very limited power is used to form the link. This means that the gate substrate link after breakdown is extremely small. Under these conditions soft breakdown may occur. The soft breakdown characteristics of n^+ poly-Si NMOS capacitors on 8 nm oxide thickness are studied in the next section.

5.6.3 Summary

The I-V characteristics of thin oxide n^+-poly/oxide/p-substrate NMOS capacitors after high power breakdown are interpreted in terms of a nanometer scale gated diode with the gate connected to the diode. The size of the link depends strongly on the power dissipation during breakdown and hence also on the area of the MOS capacitor and parasitic capacitances of the measurement set-up. This indicates that care should be taken when measuring the post breakdown I-V characteristics. For low power breakdown, the forward currents of the diode like characteristics are non ideal and at high forward gate bias limited by the series spreading resistance. With increasing stress current the forward characteristics become more ideal.

5.7 I-V characteristics after soft breakdown

In the previous section the I-V characteristics of n^+ poly-Si NMOS capacitors after low and high power *hard breakdown* were investigated. In this section the post breakdown I-V characteristics after *soft breakdown* are investigated. Soft breakdown is observed if only a very limited power is used to form the gate substrate link.

Since it has been concluded that the I-V characteristics after breakdown depend strongly on the amount of energy released through the breakdown path during discharging of the MOS and parasitic capacitances, it seems logical to assume that the barrier between soft-breakdown and hard-breakdown is not described by device parameters [34, 35] but is entirely characterized by the energy threshold of catastrophic current runaway.

Soft-Breakdown(SB), quasi-breakdown or B-mode SILC occurs if a limited amount of current flows through the conductive link and does not cause a thermal-runaway effect. It has been confirmed using emission spectroscopy directly after soft-breakdown occurred that the current path is localized in nature [33]. So we speculate that there exists an energy threshold E_{th} for which if E_{dis} exceeds the threshold, irreversible thermal damage, i.e. hard breakdown occurs. If, however $E_{dis} < E_{th}$ a high resistance path remains intact, resulting in soft-breakdown. This means that E_{dis} is a key parameter in evaluating gate oxide reliability. This energy threshold of catastrophic current runaway, separating the boundary between HB and SB was recently also proposed by others [140].

It was already noted that the current which flows through the breakdown path during breakdown determines the post breakdown I-V characteristics. This current is caused by the discharging of the MOS capacitor during breakdown I_{cap} and due to the conduction through the oxide during and after breakdown I_s under CCS injection conditions, see Eq. 5.21. By using a limited stress current I_s, the current which flows through the breakdown path at breakdown will be determined only by the discharging current I_{cap} of the MOS capacitor.

Under this condition ($I_s \ll I_{cap}$), it can be observed from Eq. 5.20 that the energy released through the breakdown path depends only on the oxide capacitance and the voltage across it. Thicker oxides lead to higher applied gate voltages at the same stress current(CCS) and more energy is therefore available, since E_{dis} increases with $\Delta V^2 \sim t_{ox}^2$, while C_{ox} decreases with t_{ox}. This electrical energy can be converted into thermal energy during breakdown leading to more hard breakdown events [36, 34]. Also increasing the capacitor area will increase the energy available for thermal breakdown, leading to more hard breakdown events. This indeed implies that soft-breakdown depends on the geometry of the sample [34, 35], however only indirectly.

In this section it will be shown for the first time that soft breakdown does not only occur in sub-5 nm oxides as is commonly assumed [33, 141, 142, 143, 144], but can also be enforced in 8 nm gate oxide thickness structures if the thermal energy during breakdown is very limited. This can be achieved by using small geometry structures with on-chip series resistors. To ensure controlled breakdown a 1 MΩ resistance was placed close to the probe tip to limit the discharge of parasitic capacitances in the wafer measurement set-up. Furthermore the stress current I_s was kept as low as possible.

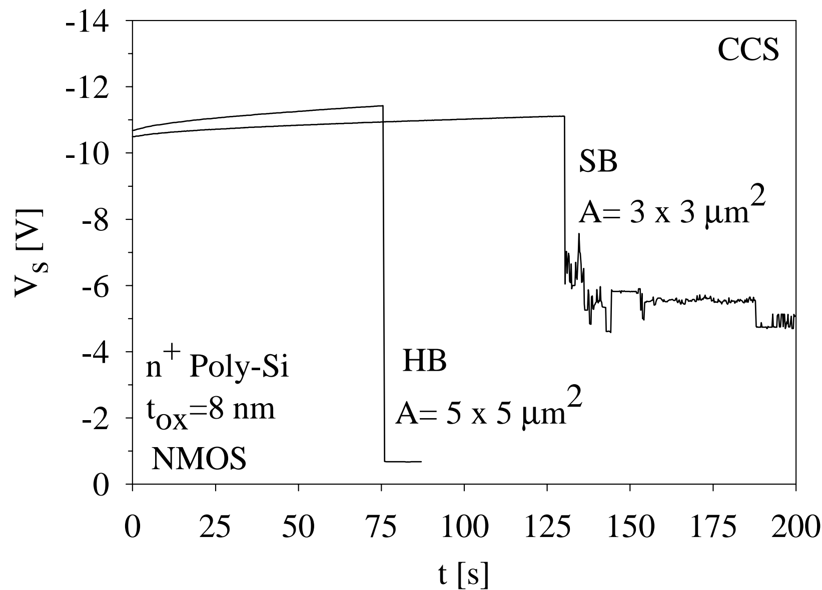

Figure 5.17: Gate voltage versus time before and after soft breakdown of n^+ poly-Si MOS capacitors on 8 nm oxide thickness. Stressing took place under CCS conditions of I_s=-5 nA. (Hard-breakdown with I_s=-0.5 μA shown as reference).

Fig. 5.17 displays the time evolution of the gate voltage V_g under CCS conditions of I_s=-5 nA of n^+ poly-Si MOS capacitors on 8 nm oxide thickness. The gate area is A=3 × 3 μm^2. It can be observed that after t=130 sec a large voltage drop of ΔV=5 V is observed, marking the point of SB. This indicates that small voltage drops are not a distinct feature of SB as is often assumed. SB is accompanied by an instability in the gate current, as can be seen in Fig. 5.17. The voltage (and current) after soft-breakdown shows a multilevel Random Telegraph Noise(RTN) behaviour which is in agreement with results found by others [145, 144, 141, 146, 147, 148].

Temperature dependence of the I-V characteristics

Fig. 5.18 displays the temperature dependence of the soft breakdown I-V characteristics. From Fig. 5.18 it can be observed that the post soft-breakdown I-V characteristics have a much weaker temperature dependence in contrast to the post hard-breakdown I-V characteristics (see Figs. 5.11 and 5.15).

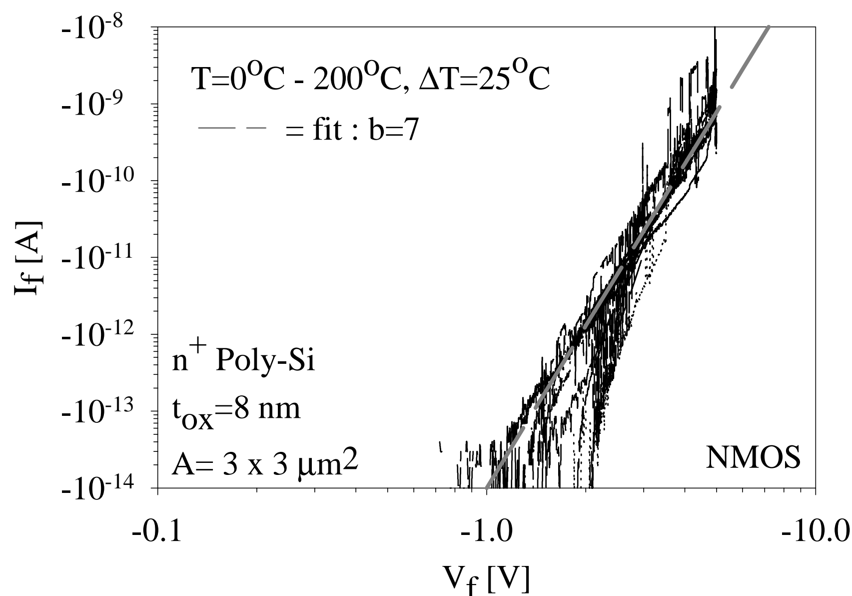

Figure 5.18: Temperature dependence of the soft breakdown I-V characteristics of n^+ poly-Si MOS capacitors on 8 nm oxide thickness. The capacitor area is A=3 $\times$ 3 μm^2.

Also it can be noted from Fig. 5.18 that the current-voltage characteristics exhibit a power law dependence (with a slope of b≈7) as was also observed by others [149, 34, 150, 151].

The I-V characteristics after SB can thus be expressed as :

$$I_g(V_g) = a \cdot V_g^b \tag{5.23}$$

Where a and b are both fit parameters.

A number of models have been proposed in literature to explain the conduction mechanism after soft breakdown. An overview of these models is given in the next section. Based on these findings a model for the conduction mechanism after low power breakdown will be proposed. It will be shown that soft breakdown and low power breakdown most likely exhibit the same conduction mechanism.

5.7.1 Summary

We demonstrated for the first time that soft-breakdown can occur even in 8 nm oxide thickness MOS capacitors, if the energy during breakdown is limited. This indicates that soft-breakdown is not an intrinsic property of sub-5 nm MOS capacitors, but depends on the amount of energy available during breakdown. It was therefore assumed that there exists an energy threshold for which if $E_{dis} < E_{th}$ a high resistance path remains intact, resulting in soft-breakdown.

5.8 Conduction mechanism after soft and low power breakdown

In this section the conduction mechanism of the I-V characteristics after soft and low power breakdown is studied. First of all the conduction mechanism after soft breakdown is investigated.

Conduction mechanism after soft breakdown

The current conduction mechanism after soft-breakdown has been investigated in detail much recently. A variety of models were proposed to explain the I-V characteristics after SB. Lee *et al.* [33] proposed a local oxide thinning model with a current conduction similar to direct-tunneling. Okada *et al.*[149, 143] proposed Variable Range Hopping(VRH) for the conduction mechanism after SB. This model can explain the temperature dependence after soft-breakdown, however they pointed out that the power law dependence of the I-V characteristics can not be explained using VRH. An alternative explanation was given by Houssa *et al.* [150, 151] which used a percolation model based on non-linear conductor theory to explain both the temperature dependence as well as the I-V characteristics after SB.

More recently, Takagi *et al.* [74] showed that in n^+ poly-Si PMOS gate devices at -V_g the I-V characteristics after soft breakdown are completely dominated by holes tunneling from the substrate to the gate. This is an important result, since all other models mentioned above are based on electron conduction being the most important conduction mechanism.

The only conflicting issue with hole tunneling from the substrate to the gate is that at -V_g their are also a lot of electrons available for tunneling in the n^+ poly-Si gate. These electrons have a much higher tunneling probability compared to holes, see chapter 2. To explain this discrepancy they proposed a tip like conductive filament for the leakage path after soft-breakdown, see Fig. 5.19.

This tip like structure increases the tunneling probability of carriers tunneling from the substrate to the gate. This means that for this type of structure at -V_g

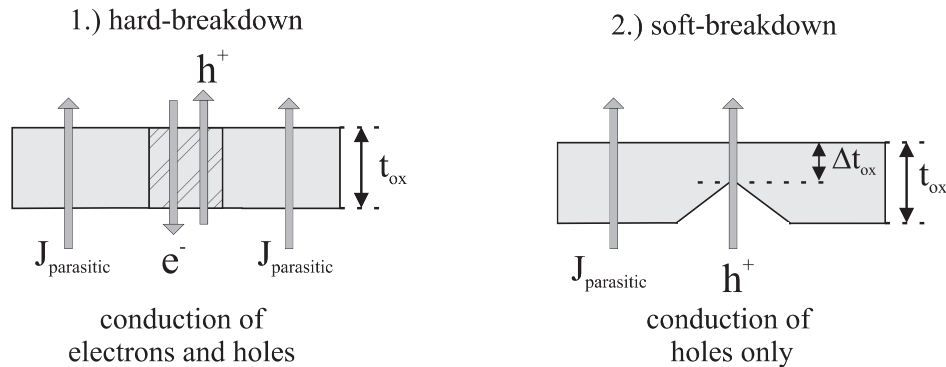

Figure 5.19: Schematic representation of the possible conduction mechanisms at -V_g after 1.) hard-breakdown and 2.) soft-breakdown.

holes tunneling from the substrate to the gate have a higher tunneling probability compared to electrons tunneling from the gate to the substrate. Note that it was already observed in chapter 2 and 3 that hole tunneling from the substrate to the gate becomes increasingly important for ultra-thin oxides at -V_g. Furthermore this hole current increases strongly with increasing electrical stress.

Conduction mechanism after low power breakdown

Next the conduction mechanism of the I-V characteristics after low power breakdown is investigated. The strong temperature dependence at low forward voltage (-V_g) observed in Fig. 5.15 indicates that the I-V characteristics of the link can not be described by direct tunneling or trap-assisted tunneling only.

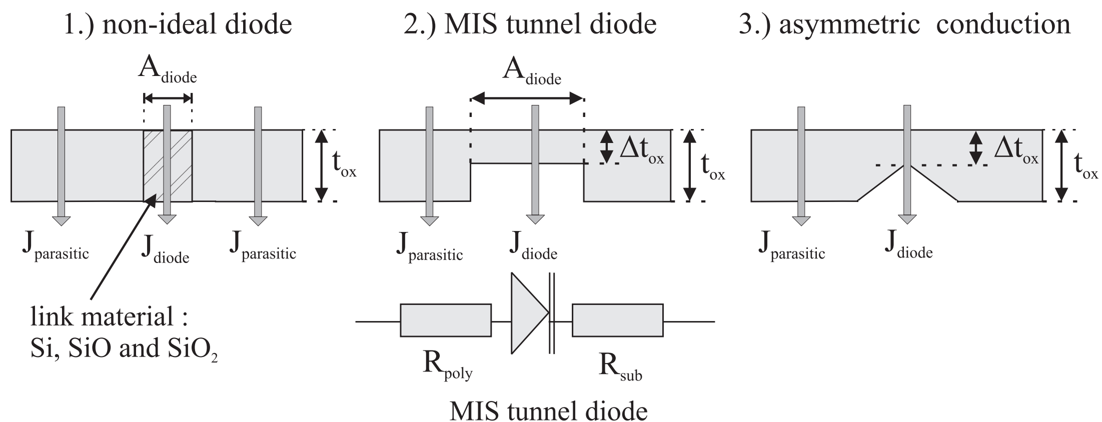

Figure 5.20: Possible conduction mechanisms for the low power post breakdown I-V characteristics. 1.) non-ideal diode 2.) MIS tunnel diode and 3.) asymmetric conduction.

Fig. 5.20 displays the possible conduction mechanisms for the I-V characteristics after low power breakdown. Since for our devices t_{ox} >4 nm, parallel conduction through the gate oxide can be neglected. The first possibility is a non-ideal nanometer-scale diode with high series resistance. For low power breakdown the forward characteristics are non-ideal since the link material may consist of a mixture of Si, SiO and SiO_2. The second option is a MIS tunnel diode with a very thin insulating layer [152, 153, 154, 155]. At high forward voltages (V_f >0.3 V) the diode current component is high and the total current is therefore limited by the tunneling probability through the insulator, which increases exponentially with decreasing insulator thickness. In this region the current is limited by the rate at which holes and electrons can tunnel from one electrode to the other. At small forward bias and moderate reverse bias, the total current is virtually independent of the insulator thickness if Δt_{ox} <3 nm. In this region the total current is limited by transport through the semiconductor substrate (diode component) rather than by tunneling through the insulator.

Although both conduction mechanisms result in a reasonable fit with measurements, they are unable to explain the origin of the higher reverse current compared to the forward current measured at elevated temperatures, see Fig. 5.16.

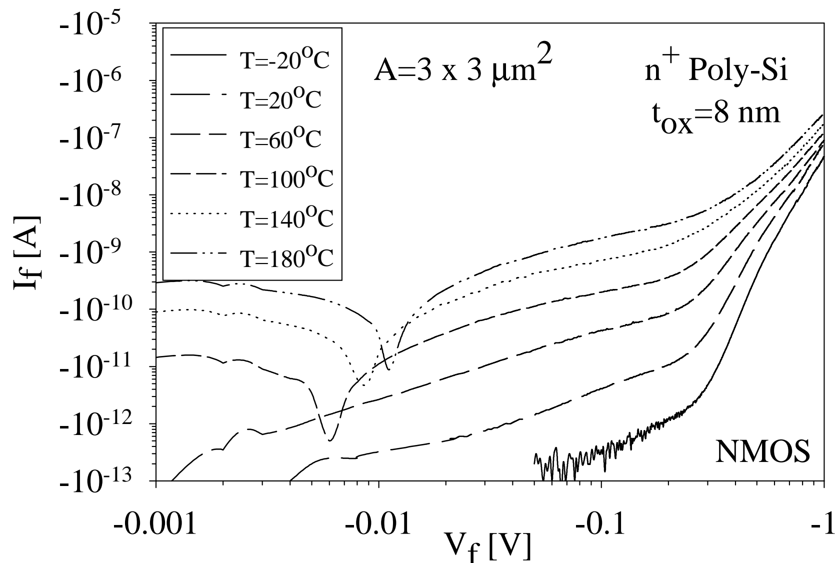

Figure 5.21: I-V characteristics after low power hard-breakdown for $-V_g$ bias conditions of n^+ poly-Si NMOS capacitors. The temperature after breakdown was varied from -20°C to 180°C, see also Fig. 5.15.

This temperature dependence strongly suggests that the conduction mechanism after low power breakdown has an asymmetric behaviour. This indicates that the conduction mechanism after low power breakdown shows much resemblance with that of soft-breakdown. It is therefore proposed that at -V_g the conduction mechanism after low power breakdown is due to holes tunneling from the substrate to the gate. For the reverse direction (+V_g) the current is dominated by electrons tunneling from the substrate to the gate. If the tunneling probability for electrons is close to unity, the reverse current is only limited by the rate at which electrons (minority carriers) can be supplied. This explains the observed temperature dependence in reverse (+V_g) direction.

However in forward direction also a strong temperature dependence is observed, in contrast to soft breakdown. To further investigate this, Fig. 5.21 displays the forward characteristics of Fig. 5.15 re-plotted on a log-log scale.

Since it is assumed that at -V_g the conduction is due to holes tunneling from the substrate to the gate, the hole concentration in the substrate needs to be evaluated as a function of the gate voltage -V_g and temperature. Fig. 5.22 displays the hole concentration in the substrate of our n^+ poly-Si MOS capacitors calculated as a function of the gate voltage under different temperatures.

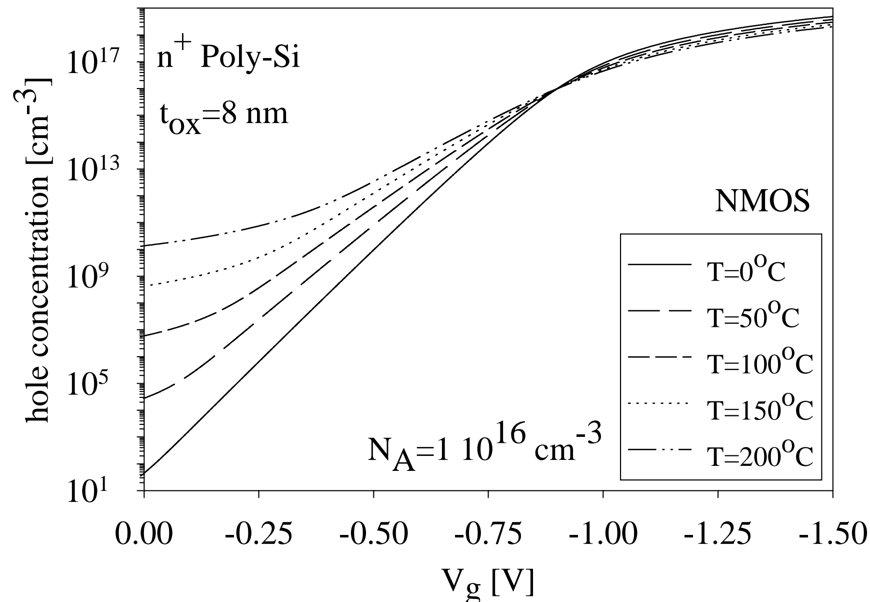

Figure 5.22: Calculated hole concentration as a function of the gate voltage -V_g for n^+ poly-Si NMOS capacitors on 8 nm oxide thickness. The temperature was varied from 0°C to 200°C.

From Fig. 5.22 it can be observed that for -V_g the hole concentration increases strongly with increasing temperature. However for V_g >-0.9 V a reduced temperature dependence is observed. The flatband voltage of our devices is approximately V_{fb} ≈-0.9 V, which means that for forward voltages higher than V_g=-0.9 V almost no temperature dependence is observed. However at lower forward voltages the temperature dependence increases with decreasing forward voltage V_g. This can also be noted from Fig. 5.21 for the forward characteristics of a low power formed gate substrate link.

5.8.1 Summary

We investigated the conduction mechanism and I-V characteristics after soft and low power breakdown. A new asymmetric conduction mechanism is proposed for the I-V characteristics after soft and low power breakdown. It is proposed that at -V_g the I-V characteristics after soft breakdown is mainly due to holes tunneling from the substrate to the gate, while at +V_g electron tunneling from the substrate (minority carriers) is the dominant conduction mechanism. This new conduction mechanism is successful in explaining the observed features, like temperature dependence and asymmetric conduction under -Vg and +V_g injection conditions.

5.9 Antifuses versus diode-antifuses

It has already been noted in section 5.4 that the post high power breakdown I-V characteristics of n^+-poly/oxide/n^+-substrate MOS capacitors closely resemble that of a programmed *antifuse* [128]. In this section the term antifuse will be explained. An antifuse is an electrically two termal device which is used in FPGAs (Field Programmable Gate Arrays) as programmable interconnections between logic devices [156]. The antifuse itself consists of a Metal-Insulator-Metal(MIM) structure where SiO_2, SiN, ONO and α-Si is used as the dielectric layer. Programming of the antifuses is achieved by forcing a high current through the dielectric layer, which eventually leads to breakdown and a permanent low ohmic connection between the logic devices is established.
Although silicon based antifuses also exists [128, 156, 157, 158], metal-to-metal antifuses clearly have a better performance, so therefore research reported in literature is mainly limited to metal-to-metal antifuses [138, 139, 159, 130, 131, 160, 133, 161].

Because of this similarity, the post high power breakdown I-V characteristics of n^+-poly/oxide/p-substrate NMOS capacitors, which resemble that of a diode we therefore call *diode-antifuses*. The diode-antifuse is an *intentionally* formed gate-substrate link in n^+-poly Si NMOS capacitors.

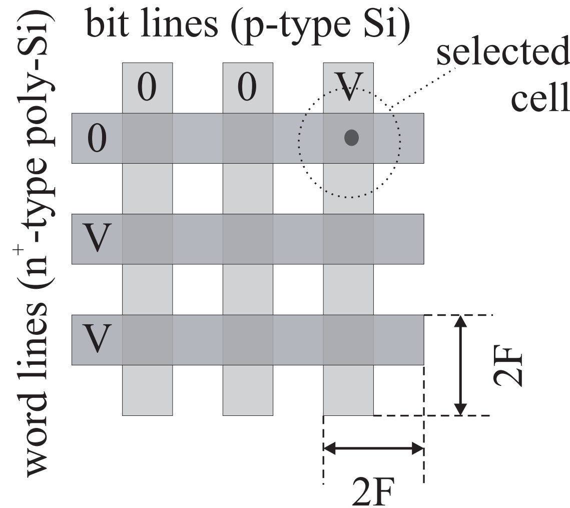

Figure 5.23: Schematic top view of the Diode Programmable Read Only Memory (DPROM) matrix. During programming, a diode-antifuse is formed at the crossing of the selected bit and word line (logical 1).

The devices are created (programmed) by controlled electrical breakdown of the gate oxide layer. The size of the conductive link after breakdown can be strongly influenced by the electrical power ($V_p \cdot I_p$) used during programming and is typically between 10 nm and 100 nm, as was already observed in Fig. 5.10. Therefore nano-scale diodes can be formed easily and they have already been exploited in low-cost Diode Programmable Read Only Memories (DPROMs) [162, 155, 163]. The Diode Programmable Read Only Memory is a stand-alone One-Time-Programmable(OPT) memory. The technology features small cell size ($4F^2$, where F is the smallest lithographic dimension in a process generation) and low mask count(7 masks for the memory array and 4 additional masks for the high-voltage NMOS and PMOS address decoder and sense amplifier transistors) [162]. A schematic representation of the DPROM matrix is depicted in Fig. 5.23. Programming of a cell is done by applying a high programming voltage V_p to the selected bit line, while grounding the selected word line. At breakdown a diode-antifuse is formed at the crossing of the selected bit and word line, resulting in a logical 1. Although the forward current of the diode-antifuse can be non-ideal due to low power oxide breakdown there is still many orders of magnitude difference in sense current between selected(forward) and unselected(reverse) cells.

5.10 Conclusions

In this chapter the electrical characteristics of n^+ poly-Si MOS capacitors after low power and high power breakdown on 8 nm and 10 nm thick oxides are studied. It was observed that dielectric hard breakdown of SiO_2 is caused by a local catastrophic runaway phenomenon and the I-V characteristics after breakdown are determined entirely by the filament cross-section formed through the dissipation of energy stored in the MOS capacitor before breakdown. Depending on gate and substrate doping polarity, different post breakdown characteristics are observed. For n^+-poly/oxide/n^+-substrate MOS capacitors the post breakdown characteristics resemble that of a resistance(*antifuses*). The value of the resistance is determined entirely by the filament cross-section of the gate substrate link. The size of the conductive link is strongly influenced by the electrical power dissipated during breakdown, which again depends strongly on the capacitor area, and is typically between 10 nm and 100 nm. An electro-thermal model was developed which is able to explain the measurements. For n^+-poly/oxide/p-substrate NMOS capacitors the I-V characteristics after high power breakdown resemble that of a nanometer size gated diode with the gate connected to the diode (*diode-antifuses*). The breakdown voltage of these diodes is high due to the gate action. Also the I_{on}/I_{off} ratio is high. The low leakage current in reverse direction and relatively high forward current indicate that the diode formed after breakdown is of good quality. Therefore nano-scale diodes can be formed easily and they have already been exploited in low-cost stand-alone Diode Programmable Read Only Memories (DPROMs). For low power breakdown the diodes become "non-ideal" and their "non-ideality" depends strongly on stress current. With increasing stress current the forward characteristics become more ideal. Furthermore, it was demonstrated that soft-breakdown can occur even in 8 nm oxide thickness, if the energy during breakdown is limited, suggesting that there exists an energy threshold for which if the energy stored on the capacitor at breakdown does not exceed the threshold energy, a high resistance path remains intact resulting in soft-breakdown. The conduction mechanism after soft and low power breakdown is still not well understood. A new asymmetric conduction mechanism was proposed for the I-V characteristics after both soft and low power breakdown. It is assumed that at $-V_g$ the I-V characteristics after soft and low power breakdown are completely determined by holes tunneling from the substrate to the gate, while at $+V_g$ electron tunneling is the main conduction mechanism. This asymmetric conduction mechanism can explain all the observed features, however further work is still required to fully understand the conduction mechanism after low power breakdown.

Chapter 6

Light emission from diode-antifuses

In this chapter results are presented of the spectrally resolved absolute measurements of the electroluminescence of silicon nanometer-scale diode-antifuses. The emission spectrum of the diode-antifuses is measured in the energy range of 1.4 - 2.8 eV at different forward and reverse currents. The dependence of the emission intensity on the current was evaluated to study the dominant emission processes. Previously proposed mechanisms for avalanche emission from conventional silicon p-n junctions are discussed in order to understand the origin of the emission. With the diode-antifuses biased in reverse breakdown, we measured (after correction for absorption and interference in the poly-Si layer) a nearly wavelength-independent emission extending from UV to IR corresponding with an average electron temperature between T_e*=5000-6000 K. This agrees with previous data of conventional avalanche p-n junctions. For the forward biased condition the spectrum reflects the silicon band structure due to emission from electron-hole recombinations. A lattice temperature at the emission site of about* T_L*=400 K was estimated. Finally, the stability of the diode-antifuses has been tested. Results indicate that the diode-antifuse is basically a high quality device. The external power efficiency has been calculated to be* $PE=2.0\cdot10^{-6}\%$ *in the energy range of 1.4 - 2.8 eV. The optical power per unit area is rather high and can reach values up to 0.1-10* W/cm^2*. Furthermore, due to its nanometer-scale dimensions, very high electrical fields and current densities are possible at low power consumption. This makes the diode-antifuse an excellent candidate for emitter elements in Si-based optical interconnect schemes and for optical sensors and actuator systems.*

6.1 Introduction

There is a strong need for an efficient Si-based on-chip light source for application in integrated optics as well as optical sensors. The integration of silicon light sources with silicon microelectronics could lead to inexpensive optical

displays and offer the potential for VLSI-compatible optical interconnect systems, enabling next generation technologies. Such light sources should be low power and small. It has already been shown that the integration of photodetectors [164, 165], waveguides [166], modulators [167], interferometers and switches with electronics in standard CMOS technology is feasible, however one of the major problems faced with Si-based optoelectronic technology is the fabrication of an efficient light source in silicon. The integration of light sources in silicon seems to be impractical since silicon has an indirect band gap making light emission due to recombination of electrons and holes a very improbable process [8]. Also the energy gap of Si ($\mathcal{E}_g$=1.12 eV) implies that emission of light is restricted to the near infrared region only.

A possible attempt to enhance recombination of electron-hole pairs in silicon is by doping Si with radiative impurity centers like Er [168, 169, 170, 171, 172] or the engineering of direct transitions in silicon, by fabricating silicon based nanostructures [168]. A very promising material in this case is porous silicon, from which intense room-temperature electroluminescence(EL) and photoluminescence(PL) in the visible and near-infrared range has been first observed by Chanham *et al.* and later by others [173, 174, 175]. Large quantum efficiencies up to 0.2% are observed, but problems related to degradation during operation, mechanical fragility, low thermal conductivity as well as the compatibility of the electrochemical treatment to fabricate the porous silicon layer with standard silicon technology still remains a point of issue.

The production of silicon or germanium nanocrystals using ion implantation in SiO_2 layers [176, 177, 178, 179] is another possibility which could overcome most of the problems encountered to obtain visible luminescence at room temperature from silicon based devices. Ion implantation of nanocrystals in SiO_2 is quite promising, since it is robust and fully compatible with the current Si planar technique.

Our work however is based on earlier observations of visible broad-band EL from reverse-biased silicon diodes brought in avalanche breakdown. It is well established that silicon p-n junctions biased in avalanche breakdown emit visible light [180, 181, 182, 183, 184]. This kind of emission originates from the transitions of hot carriers generated in the breakdown process. However, these devices require high power and light is emitted over a relatively large area or at its periphery [181, 185] and is therefore difficult to collect.

In this chapter we report spectral measurements of the electroluminescence of nanometer-scale diodes. Due to its nanometer-scale dimensions, very high electrical fields and current densities are possible at low power consumption. This makes the diode-antifuse an excellent candidate for emitter elements in Si-based optical interconnect schemes. Previously proposed mechanisms for light emission

in conventionally fabricated reverse-biased diodes are presented and discussed. It will be shown that similar processes are responsible for the emitted light in our devices.

The outline of this chapter is as follows. First in section 6.2 the experimental procedures for fabrication of the diode-antifuses are described. Also in this section the experimental setup used to record the emission spectrum of the diode-antifuses is described. Next, in section 6.3 the operation conditions of the diode-antifuses are briefly evaluated. In section 6.4 light emission measurements were performed on the diode-antifuses, with the diode-antifuses reverse biased just above the breakdown voltage V_b. Previously proposed mechanisms for avalanche emission from conventional silicon p-n junctions are discussed in order to understand the origin of the emission. In section 6.5 the measured spectra from the reverse biased diode-antifuses are fitted assuming the Bremsstrahlung mechanism for avalanche emission from our silicon junctions. An interference model is also presented to correct for the overlaying polysilicon layer. Next, in section 6.6 the emission spectrum of the forward biased diode-antifuses is evaluated. Finally in section 6.7 the long term stability of the diode-antifuses is discussed.

6.2 Experimental Procedures

n^+ poly-Si NMOS capacitors were fabricated on 0.01 Ω-cm ($N_{sub}=10^{19}$ cm^{-3}) p-type silicon substrates. A 60 nm thick field oxide was used for isolation. Next, a high quality gate oxide with 6 or 8 nm thickness (ellipsometric) was grown in diluted dry oxygen at 900°C. Undoped poly-Si layers (300 nm thick) were deposited using an LPCVD system. Gate doping was done by 50 keV, $8.0 \cdot 10^{15}$ cm^{-2} P^+ implant followed by a furnace anneal at 900°C for 30 minutes. Besides the small-area cells (10 μm × 10 μm), large-area capacitors (100 μm × 100 μm) were also fabricated in this experiment to study the defect density and the reliability of the gate oxide.
The experimental setup shown in Fig. 6.1 is used to record the emission spectra of the diode-antifuses. This setup is described in more detail by de Kort *et al.* [186]. After the light has been collected by the microscope, it is separated by a prism and focused on a photo-cathode using a lens. The projected image of the spectrum is then amplified by the photo-cathode, a multi-channel plate and projected onto a phosphor screen in front of a CCD imager chip. The spectral range of the whole system is mainly determined by the photo-cathode material (S25) and restricted to the energy range of about 1.38 eV to 3.25 eV (λ=900 - 380 nm). Furthermore, it is estimated by de Kort *et al.* [186] that with this setup it is possible to measure an absolute intensity which is accurate within a factor of 2.

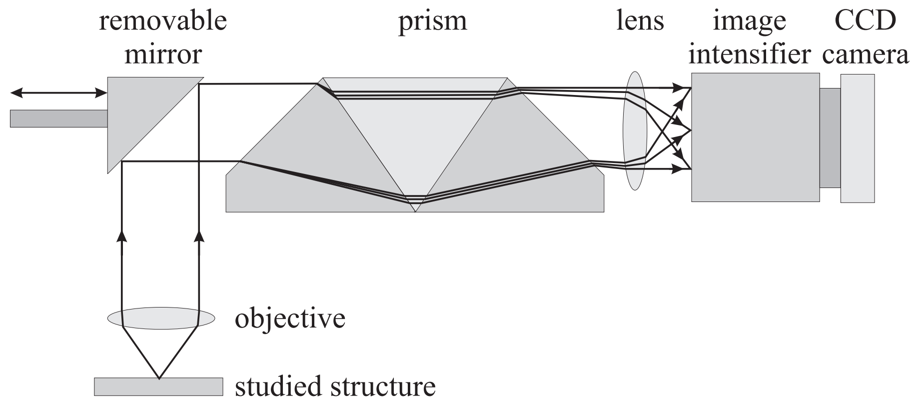

Figure 6.1: Experimental setup for the light emission spectra measurements, including microscope and removable mirror. The right side-arm contains the prism and image-intensifier for the spectral recording.

6.3 Principle of Operation

To obtain light emission in reverse-bias condition from these diodes, breakdown of the junction is needed. Fig. 6.2 shows the current-voltage characteristics of the diode-antifuses programmed at I_p=-10 mA.

The low leakage current of the diode-antifuse with a substrate doping of $N_{sub}=10^{16}$ cm^{-3} (Fig. 6.2, dashed line) shows no breakdown for voltages up to 60 V (V_b=60 V). The structure formed after breakdown resembles a gated diode with the gate and diode shorted. Because of this unique gated-diode structure, the breakdown voltage is determined by the planar junction breakdown and is therefore very high, as was already observed in chapter 5. However, to obtain light emission at low power, breakdown at a low voltage is needed. This is achieved by using a highly doped substrate $N_{sub}=10^{19}$ cm^{-3}, which lowers the breakdown voltage (V_b) down to 5.3 V as can be seen from Fig. 6.2, solid line.

From the forward characteristics it is possible to extract the junction quality factor (n=1.2 (low N_{sub}) and n=2.2 (high N_{sub})). This low value of the ideality factor reflects the good quality of the junction. Note that the relatively high leakage current and junction quality factor (n=2.2) for the highly doped substrate diode-antifuses is caused by Shockley-Read-Hall(SRH) generation and is therefore typical for highly doped p-n junctions.

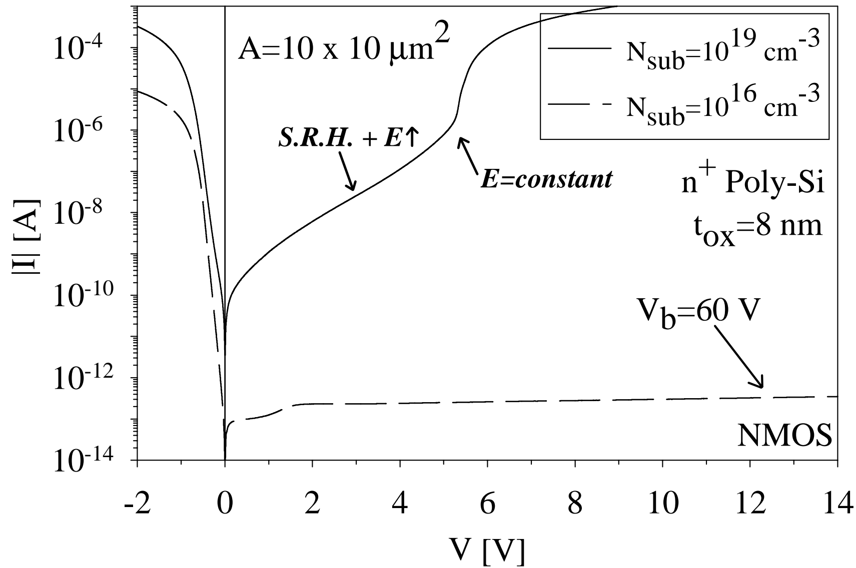

Figure 6.2: I-V characteristics of the diode-antifuses, programmed at I_p=-10 mA, for two different substrate doping $N_{sub}=10^{16}$ cm^{-3}(dashed line) and $N_{sub}=10^{19}$ cm^{-3}(solid line).

6.4 Reverse biased emission spectrum

Light emission measurements were performed on the diode-antifuses with high substrate doping($N_{sub}=10^{19}$ cm^{-3}), with the diode-antifuses reverse biased just above V_b.

The emission spectrum measured at room temperature, for different reverse currents $+I_r$ is shown in Fig. 6.3. The periodic patterns observed in the EL spectra are independent of the current and gate oxide thickness and are caused by the interference of the reflected light at the surface and the bottom of the n^+-polysilicon gate. The measured spectrum has to be corrected for this interference and the self-absorption of the poly-Si layer. This will be done in section 6.5, were this interference and the self-absorption of the poly-Si will be treated in more detail.

Several attempts have been made to understand the origin of the emitted light from reverse biased p-n junctions [187, 188, 189, 190] and up till now the most important mechanisms proposed in the literature to explain the origin of the emitted light are (see also Fig. 6.4) :

1. *direct interband transitions between hot electrons in the conduction band and hot holes in the light hole band.* [181]

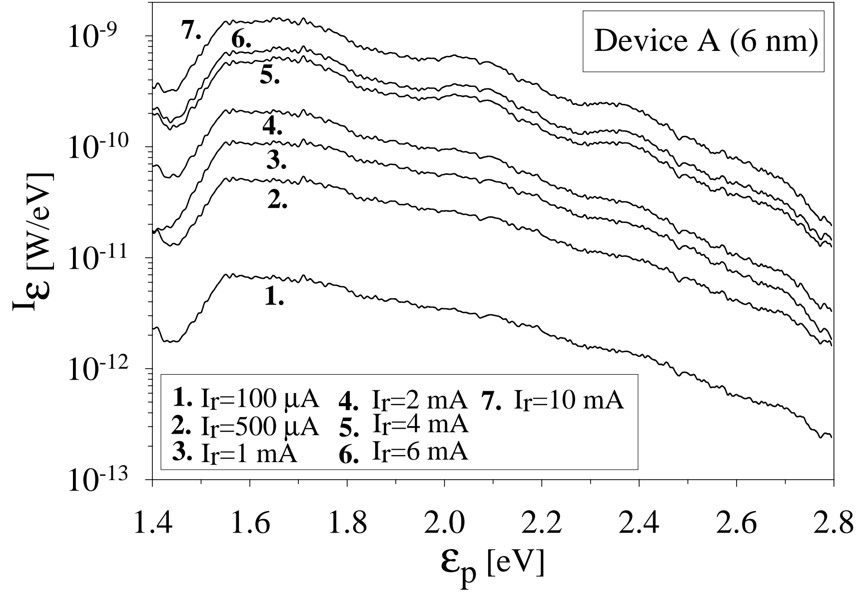

Figure 6.3: Emission spectra of the diode-antifuses, measured at room temperature with the diodes biased in breakdown at different reverse currents I_r.

2. *direct intraband transitions of hot holes between the light and heavy mass valence bands (valence-to-valence band)* . [188]

3. *indirect intraband electron transitions : Bremsstrahlung radiation due to scattering of the hot electrons by charged Coulombic centers, or phonon-assisted electron transitions (conduction-to-conduction band).* [191, 189]

4. *phonon-assisted indirect recombination of electrons and holes under high-field conditions.* [190]

These published theories and explanations typically fit at least some part of the measured spectrum, but are generally unable to explain the origin of the light emission in the whole measured spectral range.

To study the dependence of the emission intensity on the current, the emission intensity at 1.6 eV was plotted versus the reverse current I_r (here only shown on a double log scale to enable a large current-intensity range, see Fig. 6.5, Device A). This resulted in a linear current dependence, ruling out any contribution from radiative electron-hole recombinations as will be discussed below.

Since the recombination mechanism in principle requires both type of carriers, i.e. electrons and holes the transition probability is proportional to the product

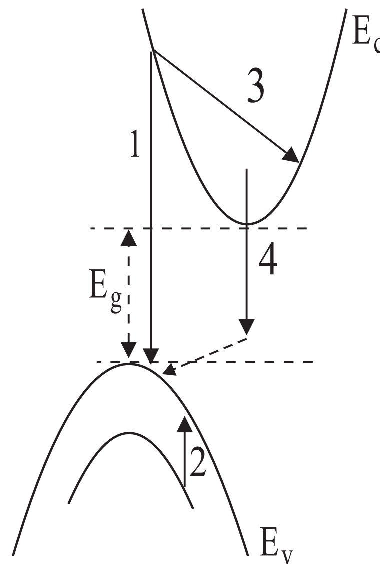

Figure 6.4: Silicon band structure model. The arrows represent: 1) direct interband recombination, 2) direct intraband hole transitions, 3) indirect intraband electron transitions (a. o. Bremsstrahlung), 4) indirect interband recombination.

of their concentrations. These carriers are generated by impact ionization within the depletion layer. As both type of carriers are generated in equal quantities (if the thermally generated reverse current is neglected) and both contribute linearly to the external current, the emission intensity should be a quadratic function of the current in contrast with our experimental results. The only recombination process with an intensity proportional to the current could be the recombination between an avalanching carrier reaching the neutral region and a minority carrier. However, since the junction is reverse biased, there is no charge storage in the neutral regions and this process can therefore not significantly contribute to the photon emission.

This indicates that only one type of carrier (in this case electrons) is responsible for the emission of photons. The recombination process can therefore be excluded as the correct emission mechanism here. Under the assumption of a constant energy distribution the Bremsstrahlung process seems to be consistent with the observed linear current dependence as it requires only one carrier type for the emission of photons. However other intraband transitions (conduction-to-conduction or valence-to-valence band) also support a linear current dependence. A clear distinction between these mechanisms can therefore not be made on the basis of our experiments.

It should be noted that recently a multi-mechanism model, combining above

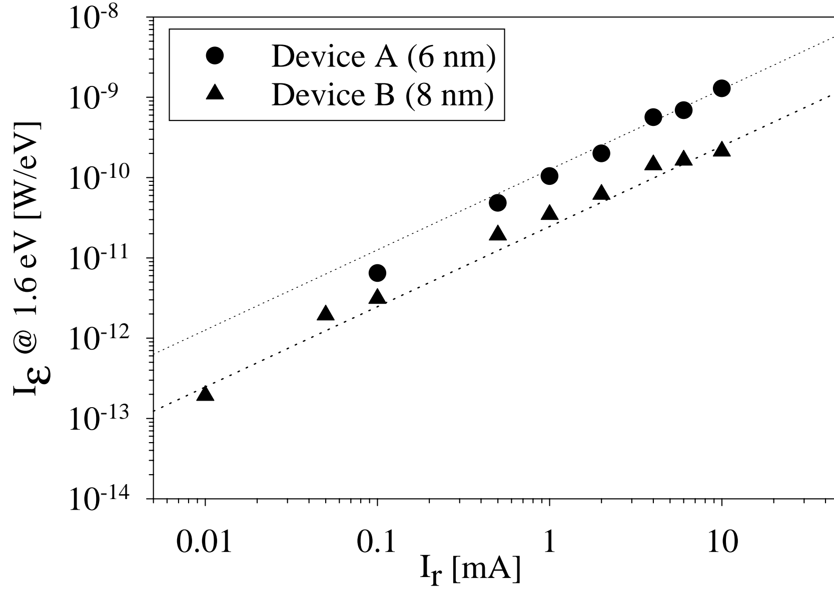

Figure 6.5: Current dependence of the intensity measured at 1.6 eV for two reverse biased diode-antifuses A & B.

mentioned mechanisms, was proposed by Akil *et al.* [192] which provides excellent agreement with measured spectra in the whole measured spectral range. This indicates that not just one but several mechanisms might be involved in the light emission of p-n junctions in avalanche breakdown.

From Fig. 6.3 the external power efficiency(PE) has been evaluated by comparing the measured optical power with the driving electrical power. This leads to a PE of approximately $2.0{\cdot}10^{-6}$%. This value seems to be low, but it should be noted that the power efficiency is only calculated for the energy range of 1.4 - 2.8 eV and only radiation lying within a cone determined by the critical angle will be able to cross the poly-Si air interface and will be detected. The measured intensity is further reduced by the numerical aperture(NA) of the detector (which is compensated for in our case), reflection at the interface and absorption. It is found [186] that due to this the detected intensity decreases but the shape of the spectra is not noticeably affected. On the other hand, the power per unit area is high due to the nanometer-scale dimensions of the diode-antifuse and is in the range of 0.1-10 W/cm^2, assuming that most of the light is generated in a small volume centered around the diode-antifuse.

6.5 Modeling of the reverse emission spectrum

In this section the emission spectra of the reverse-biased diode-antifuses are evaluated. First of all the measured spectra have to be corrected for the interference of the reflected light at the surface and the bottom of the n^+-polysilicon gate and the self-absorption of the poly-Si layer. This interference is schematically depicted in Fig. 6.6.

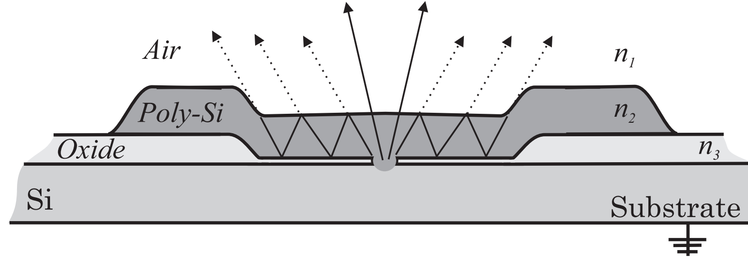

Figure 6.6: Schematic illustration of the interference of the reflected light at the surface and bottom of the n^+ poly-Si gate.

The transmission of light through an absorbing thin film for the case of normal incidence is taken from [193] and is given by Eq. 6.1 :

$$\mathcal{T}(\lambda) = \frac{16n_1n_3(n_2^2 - k_2^2)}{ab\exp(2k_2\eta) + cd\exp(-2k_2\eta) + 2e\cos(2n_2\eta) + 2f\sin(2n_2\eta)}$$

with :

$$\begin{aligned}
a &= (n_1 + n_2)^2 + k_2^2 \\
b &= (n_3 + n_4)^2 + k_2^2 \\
c &= (n_1 - n_2)^2 + k_2^2 \\
d &= (n_3 - n_4)^2 + k_2^2 \\
e &= (n_1^2 + n_3^2)(n_2^2 + k_2^2) - (n_2^2 - k_2^2)^2 - n_1^2n_3^2 + 4n_1n_3k_2^2 \\
f &= 2k_2(n_3 + n_1)(n_2^2 + k_2^2 - n_1n_3) \\
\eta &= \frac{2\pi t_{poly}}{\lambda}
\end{aligned} \tag{6.1}$$

Where n_1,n_2 and n_3 are the refractive index of resp. air, poly-Si and SiO_2, k_2 is the extinction coefficient(absorption) of Si, t_{poly} is the thickness of the polysilicon layer and λ is the wavelength of the incident light.

Since the refractive index of Si and SiO_2 and the extinction coefficient (i.e. absorption) of Si are highly dependent on the wavelength of the light, i.e. on the photon energy $\mathcal{E}_p$, they have to be calculated as a function of the photon energy $\mathcal{E}_p$ as well. This is achieved by making use of the Kramers-Kronig dispersion relation [194]. From this the refractive index of Si and SiO_2 and the extinction coefficient(absorption) of Si can be evaluated as a function of the photon energy $\mathcal{E}_p$ and the result is given in Fig. 6.7. The refractive index of air is assumed to be constant (n_1=1.0) over the whole energy range.

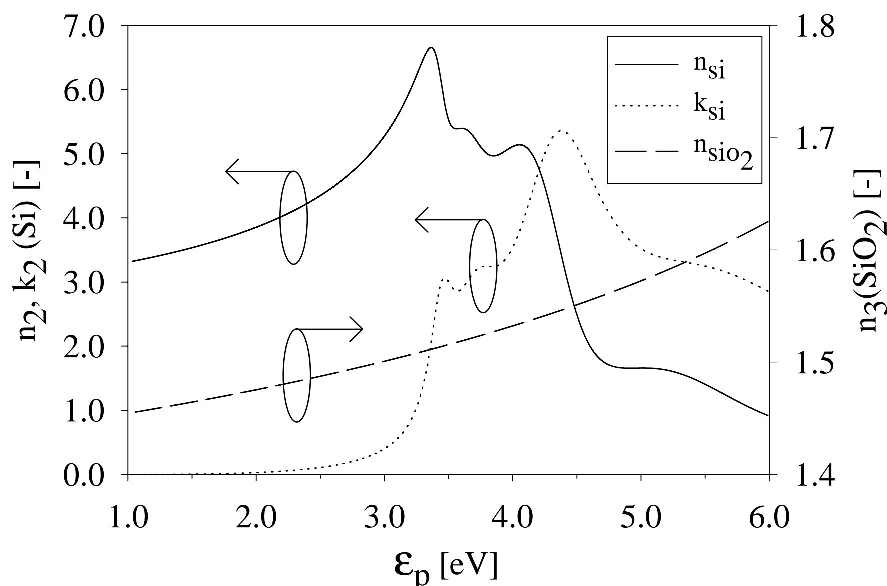

Figure 6.7: Calculated refractive index n_2 of Si, n_3 of SiO_2 and extinction coefficient k_2 of Si as a function of the photon energy. The extinction coefficient of SiO_2 is negligible in the measured energy range. Data taken from [194].

Fig. 6.8 shows the normalized spectrum at I_r=1 mA, corrected for the self-absorption of the 300 nm polysilicon layer and for the Fresnel-transmittance at the polysilicon-oxide-air interfaces. This spectrum shows a broad nearly wavelength-independent spectrum from UV to IR. The remaining oscillations in the corrected spectrum are due to the limited fitting accuracy of the model used to calculate the transmission spectrum. Refining the model would mean to include the temperature dependence of the refractive index, using the actual refractive index of poly-Si instead of assuming mono-Si and including light emission from the whole volume of the diode-antifuse rather than treating it as a point-source.

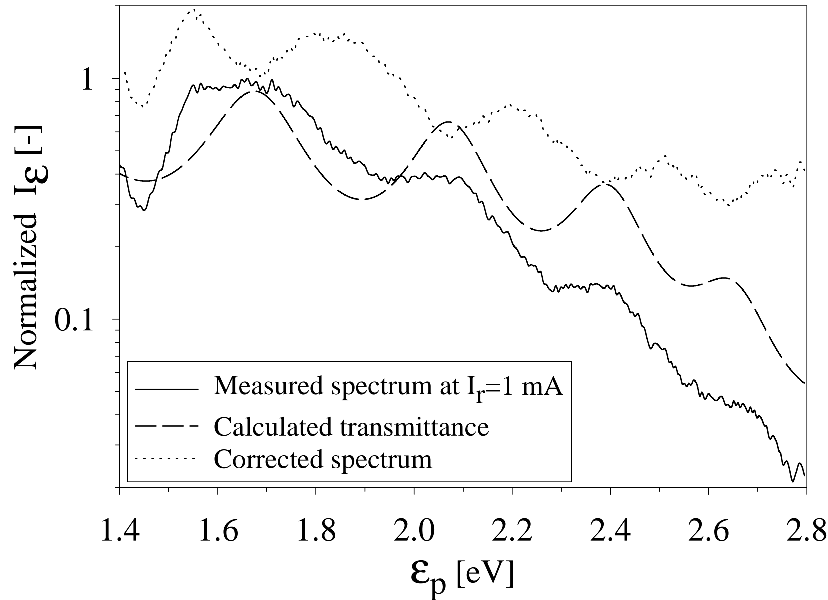

Figure 6.8: Emission spectrum measured at I_r=1 mA, corrected for the Fresnel transmittance at the oxide-polysilicon-air interfaces and for the self-absorption inside the polysilicon layer.

We can now compare the measured spectra from our diode-antifuses with that of conventional fabricated p-n junctions by using the Bremsstrahlung theory proposed by Figielsky *et al.* [191]. The Bremsstrahlung theory is adapted here since it is commonly used by others to explain their data and thus it allows use to compare our measured spectra with that of others. By assuming a Maxwellian carrier distribution ($f(\mathcal{E}) \propto \exp[-\mathcal{E}/kT_e]$), an average effective electron temperature of T_e=5000-6000 K can be derived from the slope of the corrected spectrum of Fig. 6.8. This value is close to 4000-5000 K, which is reported in literature for conventional p-n diodes [191, 195, 184]. The little higher electron temperature observed, could be the result of the high doping concentration N_{sub} used. Since the maximum electric field strength increases with increasing doping concentration [8], the maximum electric field strength which can be reached is higher than for conventionally fabricated diodes. The light-emitting mechanism is supposed to correlate strongly with the electric field strength. Nevertheless, it is also assumed that the doping profile declines by oxygen contamination and by melting processes during formation of the diode-antifuses.

From Fig. 6.3 it can also be observed that the spectrum shape does not depend

on the reverse current, since the steady-state junction electric field is always at the breakdown value $V=V_b$. This means that the carrier effective temperature T_e is expected to stay almost the same. It should however be noted that the radiating electrons have a kinetic energy well above 1 eV, so these carriers are not confined in the conduction band minima and therefore the concept of electron effective mass can not be adopted anymore. Moreover, the actual carrier distribution function is probably far from being Maxwellian (especially at high fields) so the Bremsstrahlung theory can therefore not be used to get an acceptable *quantitative* description of the spectrum [195]. Therefore this theory is only used to compare our measured spectra with that of conventional fabricated p-n junctions.

6.6 Forward biased emission spectrum

In this section the emission spectrum of the forward biased diode-antifuses is investigated. The application of a forward bias causes the mutual injection of carriers (electrons and holes) into the majority region of the opposite carrier type within the range of the characteristic diffusion length. These minority carriers recombine with the majority carriers within a mean lifetime via trap states (SRH), donor or acceptor levels or with a quantum efficiency of 10^{-4}% via the emission of a photon via photon assisted band-to-band recombination. In the latter case the principle of momentum conservation is satisfied by emission or absorption of a phonon. The emission from the forward biased diode-antifuses therefore has a uniform distribution over an area which is characterized by the diffusion length of the injected carriers.

The emission spectrum of the indirect transition will have a peak at $\mathcal{E}_p$=1.12 eV and thus will reflect the band structure of silicon. For the other mechanisms the peak will shift towards lower energies, for instance in the case of SRH, the peak will be at $\mathcal{E}_p$=0.56 eV for traps close to the centre of the bandgap, which are the most effective recombination centers. However, since the spectral range of the whole system is mainly determined by the photo cathode material (S25) and restricted to the energy range of about 1.38 eV to 3.25 eV only the outermost tail of the recombination peak can be recorded.

The emission spectra of the forward-biased diode-antifuses, measured at room temperature under different forward currents I_f is given in Fig. 6.9.

Due to the absence of a strong electric acceleration field in forward operation the carriers remain in thermal equilibrium with the lattice of the emission site. So the spectrum reflects the lattice temperature at the emission site. Different manufacturing processes of the devices are therefore of no importance [182, 184]. This means that the emission spectrum of the forward biased diode-antifuse should

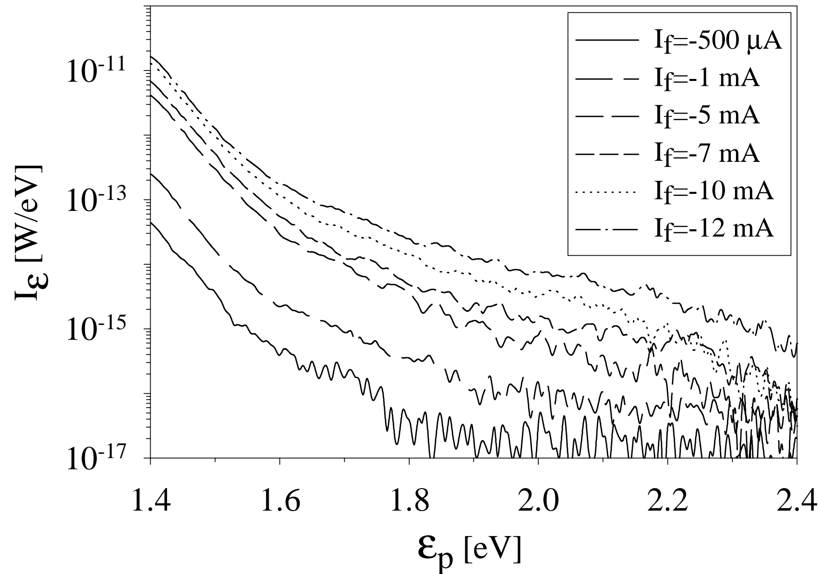

Figure 6.9: Emission spectra of the forward-biased diode-antifuses, programmed at I_p >-12 mA, measured at room temperature with different forward currents I_f.

be similar to that of conventional fabricated diodes. This is the case, as can be seen by comparing the measured spectra with that of conventional fabricated diodes [181, 182, 184]. Using Maxwell Boltzmann statistics the lattice temperature at the emission site is derived from Fig. 6.9 to be T_L=400 K, so almost no heating of the lattice takes place during measuring of the diode-antifuses under forward bias conditions.

6.7 Stability of the reverse emission spectrum

The stability of the diode-antifuses has been tested for over more than one week of continuous operation.

A constant current of $I_r=0.5\cdot|I_p|$ was passed through the diode-antifuse while the voltage across the diode-antifuse was monitored. Fig. 6.10 is a plot of the monitored voltage across the diode-antifuse as a function of the stress time. Almost no significant degradation in the electrical I-V characteristics has been observed, from which it can be concluded that the diode-antifuse is a reliable device. This is in agreement with the already known high reliability data of Si-based antifuses [128, 156, 157, 158].

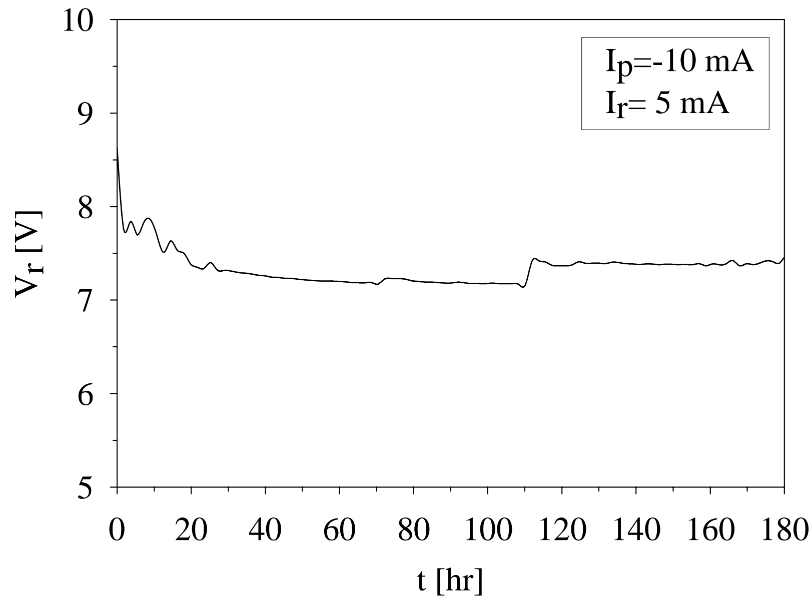

Figure 6.10: Voltage across the diode-antifuse as a function of the stress time for a reverse current of I_r=5 mA. The diode-antifuse was programmed at I_p=-10 mA.

6.8 Conclusions

We carefully measured the electroluminescence spectra of forward and reverse-biased silicon nanometer-scale diode-antifuses. The corrected emission spectrum in the reverse-biased condition shows a broad nearly wavelength-independent spectrum from UV to IR with an average effective electron temperature of about T_e=5000-6000 K. The external power efficiency has been calculated to be at least PE=$2.0 \cdot 10^{-6}$%. The power per unit area is high due to the nanometer-scale dimensions of the diodes and is in the range of 0.1-10 W/cm^2. In the forward-biased condition the emission spectrum reflects the silicon band structure, from which only the outermost tail of the spectrum can be measured. The stability of the diode-antifuses has been tested for more than one week of continuous operation. First results indicate that the diode-antifuse is a reliable device, however more data are needed. Finally, both experimental and theoretical work is still required to fully understand the emission spectrum of the diode-antifuses.

Chapter 7

Conclusions and Recommendations

"I was born not knowing
and have only had a little time to change that here and there."

Richard P. Feynman (1918-1988)

7.1 Summary

Gate oxide reliability has always been a major issue in determining the feasibility of MOS devices. The steady down-scaling of CMOS devices has lead to aggressive down-scaling of the gate oxide thickness for future MOS devices. However it is required that, among other concerns, the gate oxide can still meet requirements for reliability. Ultra-thin gate oxide reliability was studied mainly for n-doped polycrystalline Silicon (poly-Si) gate material up till now. With the down-scaling of the gate oxide thickness below 10 nm (0.5 μm CMOS), p^+ poly-Si gate electrodes have been proposed for deep sub-micron gates to replace n^+ poly-Si gates. The reliability of ultra-thin gate oxides with both n^+ and p^+ poly gate devices was the main subject of this thesis. Also the influence of polycrystalline Silicon-Germanium (poly-$Si_{0.7}Ge_{0.3}$) as a gate material on the conduction and degradation mechanisms of advanced CMOS devices was studied. P^+ poly-SiGe allows modification of the valence band edge position of the gate by varying the Ge fraction x in poly-$Si_{1-x}Ge_x$ gate devices and therefore influence the gate workfunction for p^+ gate devices.

The most important results obtained in this thesis are :

1. *The conduction mechanism (I-V) of p^+ and n^+-gates with poly-Si and poly-SiGe was studied.*

   A new model based on Minority Carrier Tunneling(MCT) from the gate was proposed for the J_g-E_{ox} characteristics of our p^+ gate devices under gate injection conditions (-V_g). For very thin oxides (t_{ox} < 4 nm) it was observed that a hole current is flowing from the source/drain to the gate in the low voltage regime.

2. *The Stress-Induced Leakage current(SILC) of ultra-thin gate oxides with both n^+ and p^+ poly-Si and poly-SiGe gates was studied.*

   For p^+-poly gate devices, asymmetric SILC (gate bias polarity) and reduced SILC for p^+ poly-$Si_{0.7}Ge_{0.3}$ was observed. It was noticed that for very thin oxides (t_{ox} <4 nm) the SILC current at -V_g and at low voltages is dominated by hole tunneling from the substrate to the gate. This current was interpreted as trap assisted hole tunneling (HTAT). An inelastic trap assisted tunneling model was developed to evaluate the SILC current for both n^+ and p^+ gate devices under FN, MCT and VBT injection conditions. This model is successful in describing the experimental I-V characteristics after SILC.

3. *Gate oxide breakdown of ultra-thin gate oxides with both n^+ and p^+ poly-Si gate devices was investigated.*

   For n^+ poly-Si gates on 2.5 nm gate oxides a decrease in t_{bd} of nearly 4 orders of magnitude was observed when the ambient temperature was increased from 25°C to 200°C. For p^+-poly Si gate devices an increase of t_{bd} with increasing active gate doping was observed. It was concluded that both the total energy release at the anode and the electron fluence are important parameters for t_{bd} of ultra-thin oxides.

4. *The post breakdown I-V characteristics of n^+ poly-Si gate devices were studied.*

   It was observed that dielectric hard breakdown of SiO_2 is caused by a local catastrophic runaway phenomenon. The I-V characteristics after breakdown are determined by the filament cross-section formed through the dissipation of energy stored in the MOS capacitor before breakdown. An electro-thermal model was developed which was able to explain the I-V characteristics after hard breakdown. When power dissipation during breakdown is limited, it was noticed that soft-breakdown can also be enforced in 8 nm gate oxide thickness structures. It was proposed that there exists an energy threshold for soft-breakdown. If the energy stored on the

capacitor at breakdown does not exceed the threshold energy, a high resistance path remains intact resulting in soft-breakdown. The I-V characteristics after low power breakdown indicate that the conduction mechanism is asymmetric with respect to gate bias polarity. However the conduction mechanism after low power breakdown is still not well understood.

5. *Light emission measurements were performed on n^+ poly-Si NMOS gate devices after breakdown.*

   Under substrate injection conditions, a nearly wavelength-independent emission extending from UV to IR corresponding with an average electron temperature between T_e=5000-6000 K was measured. For gate injection conditions, the spectrum reflected the silicon band structure due to emission from electron-hole recombinations. The stability of the structure formed after breakdown was tested. Results indicated that the device formed after breakdown is basically a high quality device.

7.2 Conclusions and Directions for further research

Based on the understanding obtained in this thesis we can draw some conclusions. However, still some aspects are not well understood and a lot of work remains to be done. Therefore recommendations for further research are given as well.

7.2.1 Conduction mechanism for p^+ gate devices

The conduction mechanism at -V_g for p^+ poly gate devices is significantly different compared to n^+ poly gate devices. It was proposed that a possible conduction mechanism for our p^+ poly gate devices at -V_g is tunneling of minority carriers (MCT), i.e. electrons from the conduction band of the gate. To investigate this, the conduction due to interface states present at the poly-Si/SiO_2 interface (IST) was neglected. However, there is a high density of interface traps present at the p^+ poly gate-SiO_2 interface from which electrons can tunnel into the oxide. Moreover, the band bending (gate depletion) at the p^+ poly gate/SiO_2 interface for -V_g increases the amount of filled interface traps. The contribution of the interface traps to the tunneling current at -V_g for our p^+ gate devices should therefore be investigated.

For very thin oxides (t_{ox} < 4 nm) it was observed that a hole current is flowing from the source/drain to the gate in the low voltage regime. Moreover this hole current increases strongly with decreasing oxide thickness and increasing electrical stress. This might have a large influence on the reliability of ultra-thin oxides

at operating conditions. The influence of this hole current on the reliability of ultra-thin oxides has not been analyzed in this thesis and remains an important aspect to be investigated.

7.2.2 Lifetime prediction of SiO_2

The reliability of ultra-thin gate oxides at operating conditions is an important issue for the feasibility of future CMOS devices. Since time-to-breakdown (t_{bd}) measurements under operating conditions are not possible, due to time constraint, all reliability studies are performed at accelerated test conditions. The main purpose of these studies is to predict oxide lifetime (t_{bd}) at operating conditions. This means that an accurate extrapolation model is needed to predict oxide lifetime at operating conditions. A fundamental understanding of the degradation mechanisms of SiO_2 is therefore needed. The three most accepted models for oxide degradation reported in literature were briefly described in chapter 1. These models will be reviewed based on our findings.

First of all it was observed in chapter 3 that for 5.6 nm gate oxide thickness the generation rate of electron traps in SiO_2 are identical for all stress fields. It was concluded that the electron flux determines the wearout of the gate oxide and that the oxide field strength merely acts as an acceleration factor for the degradation process. This indicates that the *E_{ox}-model*, which is solely based on the applied electrical field, does not hold under the stress conditions used in chapter 3 for this oxide thickness range. Because it was observed that defect generation is proportional to the stress current, which means that the electron flux plays an important role in the degradation process. This suggests that under the stress conditions used in chapter 3 the *$1/E_{ox}$ model* is better in explaining the degradation of the gate oxide.

However for sub-5 nm oxides it was proposed in literature that defect generation correlates better with applied gate voltage V_g. This was also confirmed in chapter 4 for n^+ poly-Si gate devices. A weak gate bias polarity dependence was observed with respect to time-to-breakdown if t_{bd} is plotted as a function of the gate voltage V_g. This is remarkable, since the current density under CVS was more than one order of magnitude higher for $+V_g$ compared to $-V_g$ injection conditions. This clearly demonstrates that for ultra-thin oxides one might question the validity of the *$1/E_{ox}$-model*, since the t_{bd} correlates better with V_g than $1/E_{ox}$. To test the validity of the *$1/E_{ox}$ model* for sub-5 nm oxides it is thus necessary to perform t_{bd} measurements at low voltages in order to establish if V_g and thus E_{ox} or $1/E_{ox}$ is the correct extrapolation variable.

Since direct measurements of t_{bd} at low voltages is difficult due to time constraints, indirect monitors like SILC are used at low voltages to measure defect generation. This defect generation is than correlated with breakdown to predict

t_{bd} at low voltages [7]. Also extreme high temperatures are used to measure the t_{bd} at low voltages. Stathis *et al.* [7] observed that the E_{ox}*-model* relates much better with t_{bd} at low V_g and that the $1/E_{ox}$ *model* is inconsistent with the reported thickness dependence at low V_g.

However it should be noted that in chapter 4 of this thesis an increase of t_{bd} with increasing gate anneal RTA temperature, i.e. increasing active gate doping, for p^+-poly Si gate devices was observed. This is most likely related to a decrease in tunneling current during stress at a fixed gate voltage. This indicates that both the total energy release at the anode and the electron fluence are important parameters for t_{bd} of ultra-thin oxides. So for our p^+ gate devices no unique relation between t_{bd} and V_g was found.

It can thus be assumed that for sub-5 nm oxides the results appear to confirm some form of the E_{ox}*-model* of extrapolating lifetimes to low voltages. However, the physics are different from the conventional E_{ox}*-model* which states that breakdown is field and time driven rather than controlled by electron fluence and energy. Nevertheless one should be careful with extrapolating lifetimes to low voltages assuming a linear dependence between $\log(t_{bd})$ and V_g [7], since it is still not evident that there exists a direct relation between defect generation measured from SILC and t_{bd}. This is especially true for p^+ gate devices under gate injection conditions, since for increasing active gate doping a higher t_{bd} is observed at a fixed gate voltage (CVS).

Moreover, the temperature acceleration of the t_{bd} as observed in chapter 4 is also an important issue. The effect of temperature on the t_{bd} characteristics is an important parameter since often applications require reliable operation of devices at elevated temperatures. The industry therefore specifies oxide reliability at a elevated temperature, for instance T=90 - 120 °C. A physical model which can explain the observed temperature dependence is therefore required.

Last but not least, it was observed that for sub-5 nm oxides a hole current is flowing from the source/drain to the gate in the low voltage regime, which increases strongly with decreasing oxide thickness and increasing electrical stress. This also might have a large impact on the t_{bd} of (ultra-)thin oxides at low (operating) voltages.

This indicates that a physical model including temperature dependence, trap-assisted hole tunneling etc. for defect generation in sub-5 nm oxides is therefore strongly needed to predict oxide lifetime at operating conditions.

7.2.3 Conduction mechanism after breakdown

The conduction mechanism after breakdown is still an important issue. It was observed that the post soft and low power breakdown I-V characteristics can be

well described by an asymmetric conduction mechanism. It was proposed that the I-V characteristics after soft and low power breakdown at low V_g is due to holes tunneling from the substrate to the gate. After hard breakdown electron conduction is the most important conduction mechanism.

This difference in conduction mechanism for soft and hard breakdown might question the relation of SILC and soft breakdown as precursors for hard breakdown. The difference in t_{bd} for soft and hard breakdown should therefore be investigated. Especially, since in chapter 4 time-to-breakdown was taken to be the first recorded breakdown phenomenon (soft- or hard-breakdown).

The relation between trap generation in the SILC process and the time-to-breakdown (soft and hard breakdown) for the reliability of ultra-thin oxides is an important topic. This needs further attention.

7.2.4 SiO_2 the final frontier ?

As was already briefly mentioned in chapter 1, if the scaling trend continues, SiO_2 may not be able to meet future reliability requirements. The exponentially increase in tunnel current with decreasing oxide thickness will increase the standby power and seriously degrade the gate oxide reliability at operation conditions. This poses a serious problem onto the further down-scaling of the gate oxide thickness for sub-100 nm feature-size technologies. This means that another material with higher reliability and lower direct tunneling current will be needed. To overcome this problem, the Semiconductor Industry Association (SIA) mentions high-ϵ dielectrics like Ta_2O_5 as a possible candidate to replace SiO_2 in sub-100nm feature-size technologies, which should enter production around the year 2006 (1997 version). The reason for using high-ϵ dielectrics is to obtain a larger gate capacitance per unit area, while still maintaining acceptably low gate tunneling currents. There is a variety of possible alternative high-ϵ materials which could replace SiO_2 in future generations CMOS technology. An overview of possible candidates to replace SiO_2 is depicted in Table 7.1 [196, 197, 198, 199, 200, 201].

To evaluate possible candidates a couple of properties are very important. That is the breakdown field E_{bd} and the relative dielectric constant ϵ_r, since the product of these two needs to be higher than for SiO_2. Furthermore, the bandgap and the alignment to the conduction band of the electrodes (poly-Si and mono-Si) are important, since the barrier of both the valence and conduction band need to be high enough to avoid excessive tunneling current.

However, the most challenging problem to overcome at this moment is the formation of SiO_2 at the Si substrate during high temperature anneal after deposition of the gate material. The formation of an interfacial layer of SiO_2 suppresses the

Dielectric Material	Rel. Dielectric Constant ϵ_r [-]	Eq. Oxide Thickness [nm]	Breakdown Field E_{bd} [MV/cm]	$\epsilon_r \cdot E_{bd}$ [MV/cm]	$\mathcal{E}_g$ [eV]
SiO_2	**3.9**	**1.0**	**10-13**	**39-51**	**9.0**
Si_3N_4	7.5	1.9	5-10	38-75	5.0
AlN	8.5	2.2	6-15	51-128	6.2
Al_2O_3	9-10	2.3-2.6	5.0	45-50	7-8
Ta_2O_5	22-27	5.6-6.9	3.5	77-95	4.4
TiO_2	15-40	3.8-10	1.0	15-40	3.2
ZrO_2	25	6.4	3.0	75	5.0
$(Ba,Sr)TiO_3$	200-400	51-103	-	-	-

Table 7.1: Possible candidate alternative gate materials to replace SiO_2 as a gate material in future generations CMOS technology.

advantage of high-ϵ dielectrics, since it reduces the gate capacitance per unit area.

Moreover, the reliability of these alternative gate materials has not been studied in detail yet. This creates some interesting research challenges to be solved in the near future.

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